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99 % Efficient 10 kV SiC-Based 7 kV/400 V DC-Transformer for Future Data Centers

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***Abstract*—The power supply chain of data centers from the medium voltage (MV) utility grid down to the chip level voltage consists of many series connected power conversion stages and accordingly shows a relatively low efficiency. Solid-State Transformers (SSTs) could improve the efficiency by substantially reducing the number of power conversion stages and/or directly interfacing the MV AC grid to a 400 V DC bus, from where server racks with a power consumption of several tens of kilowatts could be supplied by individual SSTs. The recent development of SiC MOSFETs with a blocking voltage of 10 kV enables the realization of a simple and hence highly reliable two-stage SST topology, consisting of an AC/DC PFC rectifier and a subsequent isolated DC/DC converter. In this context, an isolated 25 kW, 48 kHz, 7 kV to 400 V series resonant DC/DC converter based on 10 kV SiC MOSFETs is realized and tested in this paper. To achieve zero voltage switching (ZVS) of all MOSFETs, a special modulation scheme to actively control the amount of the switched magnetizing current on the MV and LV side is implemented. Furthermore, the design of all main components and especially the electrical insulation of the employed medium frequency (MF) transformer is discussed in detail. Calorimetric efficiency measurements show that a full-load efficiency of 99.0 % is achieved, while the power density reaches 3.8 kW/L (63 W/in^3).**

***Index Terms*—Medium-voltage, isolated DC/DC, soft-switching, ZVS, 10kV SiC MOSFETs, calorimetric measurement, medium-voltage transformer.**

I. Introduction

Solid-State Transformer (SST) technology is considered as an interesting concept to increase the efficiency of the power supply chain from the medium voltage (MV) utility grid down to the chip voltage level in data centers, by directly interfacing the MV AC grid to a 400 V DC power distribution bus [1]–[4]. Thereby, the number of cascaded conversion stages is substantially reduced, resulting in a lower complexity, higher reliability, higher power density, and higher efficiency of data center power supplies. For redundancy reasons, it is intended that each server rack (which can reach power demands in the range of 20 ... 40 kW, [5]–[7]) is supplied from an individual MV AC to 400 V DC SST. The power could then be distributed on MV level (e.g. 6.6 kV phase-to-phase rms, i.e. 3.8 kV rms phase-to-neutral) within the data center with the advantage of substantially lower cable cross sections and/or lower ohmic losses compared to LV distribution. Individual single-phase SSTs (single-phase for a low complexity) could then convert the MV grid voltage into 400 V DC and feed single server racks or clusters of racks, whereby the three phases of the MV utility grid could be symmetrically loaded by connecting the same number of SSTs to each phase.

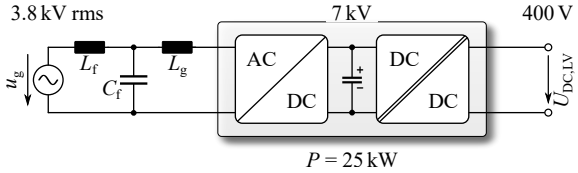

Fig. 1: Proposed single-cell two-stage realization of a MV AC to 400 V DC SST consisting of a front-end PFC AC/DC converter stage and an isolated DC/DC converter. To comply with EMI standards and to properly interface the SST to the MV grid via MV cables, an input LCL-filter is added. Given the isolated output voltage, different grounding schemes of the battery buffered DC output voltage can be implemented.

Up to the present, voltages in the 10 kV-range had to be interfaced by multi-cell converters based on ISOP, i.e. input series output parallel connected modules rated for a fraction of the total MV-side voltage, where each module is comprising an AC/DC [8]–[12] and an isolated DC/DC converter [13]–[15]. However, the recent development of 10 ... 15 kV SiC MOSFETs with their outstanding switching behavior [16]–[20] enables the construction of single-cell SSTs avoiding the series connection of several modules, and therefore resulting in a simple and reliable converter structure. Due to the reduced complexity, also a higher power density can be expected. Therefore, this paper proposes a 10 kV SiC MOSFET-based single-cell two-stage 25 kW, 3.8 kV single-phase AC to 400 V DC SST (cf. **Fig. 1**) and provides a detailed analysis and experimental verification of the isolated 7 kV to 400 V DC/DC converter stage. The associated soft-switching 3.8 kV AC to 7 kV DC PFC converter has been presented in [1] and achieves a full-load efficiency of 99.1 % and a power density of 3.28 kW/L (54 W/in^3).

As a part of the National Research Programme "Energy Turnaround" (NRP 70, cf. Acknowledgements), the efficiency goal of the SST is 98 %. Therefore, the isolated DC/DC converter has to reach an efficiency of at least 98.9 % or 99.0 % at full load considering a certain margin. Furthermore, the DC/DC converter should achieve a power density of at least 3 kW/L (50 W/in^3), comparable to the power density of the PFC rectifier stage [1]. In literature, a 15 kV SiC MOSFET-based isolated DC/DC converter with similar specifications (10 kV to 340 V, 20 kW) has been presented, achieving an extrapolated full-load efficiency of 97.3 % and a power density of roughly 1.5 kW/L (25 W/in^3) [21]. In contrast, consider-

ing the defined goals, the DC/DC converter at hand should generate only a third of the relative losses and should reach at least twice the power density.

To achieve such a compact converter, a relatively high switching frequency has to be selected, while to obtain the high efficiency, the switching losses have to be minimized by the operation of all MOSFETs under zero voltage switching (ZVS) conditions. Since the front-end AC/DC PFC stage controls the DC-link voltage, it is sufficient to realize the DC/DC converter with fixed voltage transfer ratio and galvanic isolation. For this reason, a series resonant converter (SRC) operated at resonance frequency and therefore acting as *DC transformer*, tightly coupling its input and output voltages according to the primary and secondary side turns ratio, is selected [22]. Due to the significantly different rise times of the MV and LV-side switch node voltages, a special modulation scheme has to be used for the system to achieve ZVS for all MOSFETs.

Due to the combination of the high switching frequency and the high voltage stress, dielectric losses in the transformer insulation material start playing a role. It has been shown in [23] that a thermal runaway and a destruction of the transformer could occur, if epoxy resin was selected as insulation material. The reasons are the relatively high dissipation factor and the low thermal conductivity of epoxy resins, which makes them unsuitable for the insulation of medium frequency (MF) MV transformers. Therefore, a special two component silicone compound is chosen as insulation material and the vacuum pressure potting (VPP) process used to insulate the winding package is presented in detail in this paper.

Section II describes the DC/DC converter topology and its modulation scheme to achieve ZVS conditions over the complete power range. In **Section III**, the design of all main converter components is explained in detail, with the focus on the MF transformer and its electric insulation, as well as the MV-side and LV-side power electronic interfaces. **Section IV** presents the experimental setup and measurement results including the obtained voltage and current waveforms, and the calorimetrically measured efficiency and loss distribution for different power levels. Finally, conclusions are drawn in **Section V**.

II. Topology and Modulation

For the isolated DC/DC converter stage, an LLC series resonant converter (SRC) topology is selected, mainly for the reason of clamped switch voltages, the simple operation without closed-loop control, and the possibility to achieve ZVS for all semiconductors. Hence, a high switching frequency of $48\,\mathrm{kHz}$ can be selected, which results in a high power density. Furthermore, the SRC features sinusoidal transformer currents, which are beneficial in terms of reduced high-frequency effects in the winding and the core while the currents show a low rms value, which is only $\pi/\left(2\sqrt{2}\right) = 1.11$ times higher than the corresponding DC current (magnetizing current neglected). The circuit diagram of this topology is shown in **Fig. 2(a)**. It consists of a split DC-link and a $10\,\mathrm{kV}$ SiC MOSFET-based half-bridge on the MV-side, a $52:6$ MF transformer providing the galvanic isolation, and a $1200\,\mathrm{V}$ SiC MOSFET-based full-bridge on the LV-side. The half-bridge configuration is selected

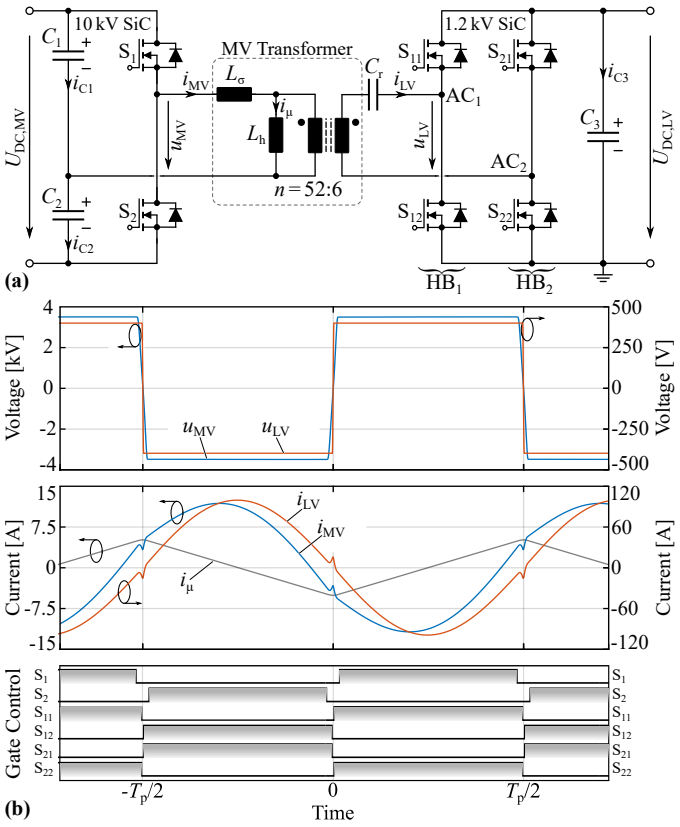

Fig. 2: **(a)** Circuit diagram of the LLC series resonant converter (SRC) consisting of a $10\,\mathrm{kV}$ SiC MOSFET half-bridge, a MF MV transformer for the galvanic isolation and the voltage step-down, a resonance capacitor C_r, and a $1200\,\mathrm{V}$ SiC MOSFET full-bridge. **(b)** Simulated voltage and current waveforms of the SRC together with the corresponding gate control signals. It can be seen that the major part of the magnetizing current i_μ is switched on the MV-side.

due to its rather simple construction and the associated voltage division by a factor of two, which is beneficial for the MF transformer design [24]. Although the LV-side DC-link voltage is only $400\,\mathrm{V}$ and therefore devices with $650\,\mathrm{V}$ or $900\,\mathrm{V}$ rating could be employed, $1200\,\mathrm{V}$, $25\,\mathrm{m\Omega}$ SiC MOSFETs are used due to their outstanding performance and to keep the flexibility to adapt the SST for $800\,\mathrm{V}$ applications by just changing the transformer turns ratio.

A. Modulation Scheme of the Dual-Active SRC

As already mentioned, the main task of the DC/DC converter is to provide the galvanic isolation and the constant $7\,\mathrm{kV}/400\,\mathrm{V}$ voltage transfer ratio, as the DC-link voltage level is controlled to a constant value by the AC/DC front end of the SST. Therefore, the SRC is operated at its resonance frequency, where it provides a quasi load-independent voltage transfer ratio and acts as a "DC transformer" [22]. Furthermore, incorporating a certain transformer magnetizing current i_μ allows the ZVS operation of all MOSFETs and hence, due to the typically low soft-switching losses (SSL), a downsizing of passive components such as the MF transformer and the DC-link capacitors is enabled by increasing the switching frequency, which is fixed to $48\,\mathrm{kHz}$.

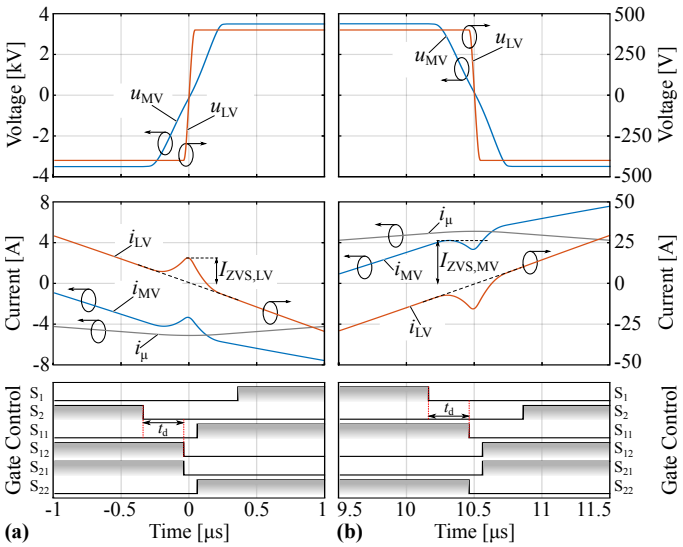

Fig. 3: Magnified view of the MV-side and LV-side voltages and currents $u_{\mathrm{MV}}, i_{\mathrm{MV}}$ and $u_{\mathrm{LV}}, i_{\mathrm{LV}}$ during **(a)** the rising and **(b)** the falling voltage edge together with the gate control signals. Due to the much larger Q_{OSS} of the MV-side MOSFETs (relative to the corresponding current), the voltage on the MV-side u_{MV} rises/falls much slower than the LV-side voltage u_{LV}. With the phase shift t_{d} between the MV and LV-side gate control signals, the switching transitions can be center-aligned, whereby the different rise/fall times create a current spike in the transformer which is utilized as ZVS current for the LV-side MOSFETs. The magnetizing current is used as ZVS current for the MV-side MOSFETs.

Fig. 2(b) shows the simulated voltage and current waveforms together with the gate signals of all MOSFETs. For the "DC transformer" operating mode of the SRC, both the MV and the LV-side MOSFET bridges apply rectangular voltages with 50 % duty cycle to the resonant tank, i.e. the transformer's leakage inductance L_σ and the resonance capacitor C_{r}, resulting in sinusoidal currents on both sides of the transformer. However, in order to achieve soft-switching, the MOSFETs must turn off a certain remaining inductive current

$$I_{\mathrm{ZVS}} = Q_{\mathrm{OSS}}/T_{\mathrm{dt}}, \tag{1}$$

which depends on the effective output charge Q_{OSS} of the switching MOSFETs and the maximum duration of the resonant switching transition, i.e. the dead time duration T_{dt}.

Since the effective output charge Q_{OSS} of the 10 kV SiC MOSFETs on the MV-side is much larger than the effective output charge of the 1200 V SiC MOSFETs on the LV-side (considering the turns ratio of the transformer and/or the corresponding current), the available transformer magnetizing current should mainly flow on the MV-side to guarantee ZVS of all MOSFETs. This can be achieved by introducing a comparably small phase shift t_{d} between the MV-side and the LV-side gate control signals. **Fig. 3** shows a magnified view of the voltages and currents during the rising and the falling voltage edge, respectively. As can be seen, the phase shift t_{d} is chosen such, that the MV-side bridge switches the major part of the magnetizing current i_μ. Furthermore, due to the phase shift t_{d}, the voltage transitions of the MV-side and the LV-side are aligned symmetrically, i.e. the much faster LV voltage transition is located in the middle of the MV voltage transition. Consequently, this leads to a certain voltage-time-area which is applied to the leakage inductance L_σ of the transformer, resulting in small current spikes on both sides of the transformer. As can be seen in **Fig. 3**, these current spikes lead to a reduction of the ZVS current on the MV-side, whereas on the LV-side the absolute value of the current i_{LV} is increased. Due to the proper selection of the phase shift t_{d}, now the LV-side switches exactly at the peak of these current spikes and hence, ZVS is also enabled for the LV-side. In practice, a compromise between the amount of magnetizing current switched on either side has to be found in dependency of the Q_{OSS} mismatch of the MV-side and the LV-side by selecting a suitable phase shift t_{d}. In the system at hand, it has been observed that this modulation works very well over the whole load range (0 kW to 25 kW) and is highly robust against changes in the switching frequency, the voltage level and even the phase shift t_{d}. For the experimental analysis $t_{\mathrm{d}} = 300\,\mathrm{ns}$ has been selected (cf. **TABLE I**).

TABLE I: Specifications and characteristics of the isolated DC/DC converter. MOSFET on-state resistances given for $T_{\mathrm{j}} = 75\,^{\circ}\mathrm{C}$ (MV-side) and $T_{\mathrm{j}} = 100\,^{\circ}\mathrm{C}$ (LV-side).

Parameter	Symbol	Value
Nominal power	P_{N}	25 kW
Switching frequency	f_{sw}	48 kHz
MV-side DC-link voltage	$U_{\mathrm{DC,MV}}$	7 kV
LV-side DC-link voltage	$U_{\mathrm{DC,LV}}$	400 V
MV-side DC-link capacitance	C_1, C_2	500 nF
LV-side DC-link capacitance	C_3	70 µF
Resonance capacitance	C_{r}	3.8 µF
Transformer leakage inductance	L_σ	195 µH
Transformer magnetizing inductance	L_{h}	4.1 mH
Transformer turns ratio	n	52 : 6
MV-side transformer rms current	$I_{\mathrm{MV,rms}}$	8.6 A
LV-side transformer rms current	$I_{\mathrm{LV,rms}}$	70.6 A
Nominal phase shift	t_{d}	300 ns
MV-side ZVS current	$I_{\mathrm{ZVS,MV}}$	4 A
LV-side ZVS current	$I_{\mathrm{ZVS,LV}}$	16 A
MV-side DC-link rms current	$I_{\mathrm{C1,C2,rms}}$	4.8 A
LV-side DC-link rms current	$I_{\mathrm{C3,rms}}$	30.9 A
MV-side switch rms current	$I_{\mathrm{S,MV,rms}}$	6.0 A
LV-side switch rms current	$I_{\mathrm{S,LV,rms}}$	50.0 A
MV-side switch resistance	$R_{\mathrm{DS,on,MV}}$	400 mΩ
LV-side switch resistance	$R_{\mathrm{DS,on,LV}}$	11.3 mΩ

III. System Design

In the following, the design of the individual main components of the DC/DC converter is described. **TABLE I** shows the specifications of the SRC, together with the values of the switched currents, and the rms current stresses of the individual components as a basis for the converter design.

A. MV-Side 10 kV SiC MOSFET-Based Half-Bridge

On the MV-side, a 10 kV SiC MOSFET-based half-bridge comprising *Wolfspeed CPM3-10000-0350* devices in combination with a split DC-link is used. For the determination of the semiconductor losses, the conduction and the switching losses are calculated in the following. With the on-state resistance and the rms current given in **TABLE I**, the total

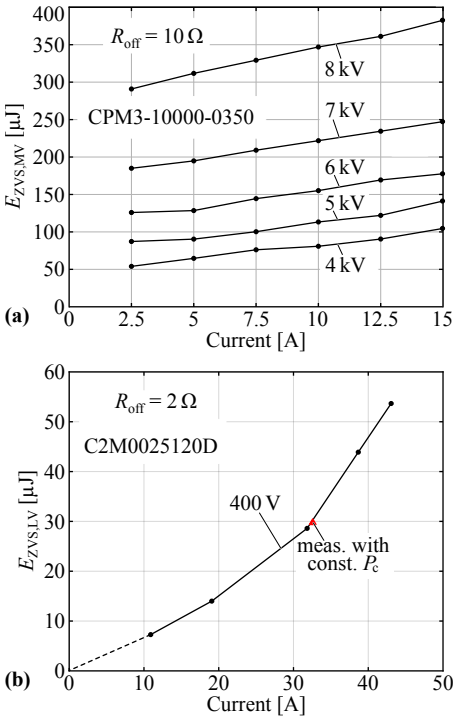

Fig. 4: **(a)** Calorimetrically measured soft-switching losses (SSL) of the 10 kV SiC MOSFETs for different DC-link voltages and currents (taken from [16]). **(b)** Calorimetrically measured SSL of one *C2M0025120D* 1200 V SiC MOSFET for different currents and a DC-link voltage of 400 V. To verify the applied calorimetric SSL measurement method, the indicated point is measured with constant conduction losses P_c and two different switching frequencies.

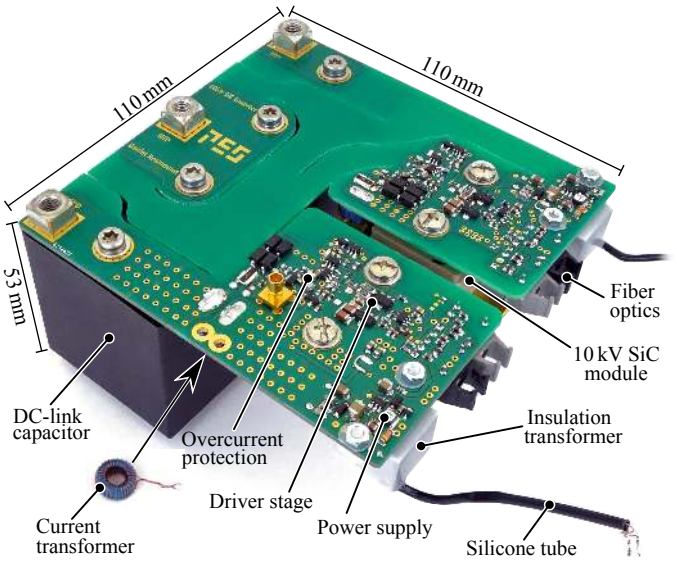

Fig. 5: 10 kV SiC MOSFET-based half-bridge with DC-link capacitors and gate driving circuitry including an ultrafast overcurrent protection, and 20 kV isolation voltage rated (and tested) gate driver power supplies.

conduction losses of both MOSFETs are $P_{c,MV} = 28.8\,W$ during full-load operation. Furthermore, although the MOSFETs are operated under ZVS, certain soft-switching losses (SSL) arise, but are not available as datasheet values. Therefore, the calorimetrically measured SSL in **Fig. 4(a)**, taken from [16], are used to determine the switching losses. For a DC-link voltage of $U_{DC,MV} = 7\,kV$ and a switched current of $I_{ZVS,MV} = 4\,A$, the energy loss per switching cycle and per MOSFET is $E_{ZVS,MV} = 191\,\mu J$. Therefore, the MV-side switching losses at a switching frequency of $f_{sw} = 48\,kHz$ are $P_{sw,MV} = 18.3\,W$ and together with the conduction losses, the total MV-side semiconductor losses are 47.1 W at full load.

For the realization of the MV-bridge, the goal is to achieve a highly compact design, despite the fact that large distances for the electrical isolation are necessary for voltages in the MV range. According to the IEC 60950-1 International Standard [25], for a sustainable operation, the required creepage distance for 7 kV is $d_{cr} = 32\,mm$, and the minimum clearance distance is $d_{cl} = 17.5\,mm$. Therefore, during the design of the PCB-based MV-bridge, possible creepage paths have to be identified and interrupted by creepage slots, which increase the breakdown voltage since $d_{cl} < d_{cr}$.

Fig. 5 shows the realized MV bridge. The PCB interconnects the DC-link capacitor with the low-side and the high-side MOSFETs, whereby busbars (not visible) are used for the connection of the drain terminals (i.e. the base plates) of the MOSFETs. Since both MOSFETs are mounted on one PCB, the full (switched) DC-link voltage of $U_{DC,MV} = 7\,kV$ occurs between the low-side and the high-side circuits on the PCB. In order to still achieve a highly compact design despite the large required creepage distances, a creepage slot separates the high-side from the low-side circuits. Furthermore, highly compact isolation transformers for the power supply of the gate drivers are on-board and feature an isolation voltage rating of 20 kV. These transformers are fed from driver circuits which are separated from the MV, whereby the required creepage distance is provided by silicone tubes that are enclosed in the insulation material of the transformer. In order to protect the 10 kV SiC MOSFETs against harmful overcurrents in case of e.g. an isolation breakdown or an operational fault, the gate drivers are equipped with an ultrafast overcurrent protection circuit (based on monitoring the source current with an air-gapped current transformer), which reacts within 22 ns and safely turns off all MOSFETs, even in case of a flashover. More details on the gate driver isolation transformers and the overcurrent protection circuit is given in [26].

The 10 kV SiC modules are directly mounted on separate heat sinks without any electrical insulation. However, since the base plates of the modules are non-isolated (i.e. the base plates act as drain terminals), the heat sinks (not shown) are floating on the respective drain potential such that the fans have to be separated from them by a clearance distance of at least $d_{cl} = 17.5\,mm$, as similarly done in [1]. Although a certain part of the air flow is bypassing the heat sinks, a thermal resistance of $R_{th,MV} = 0.125\,K/W$ per heat sink is achieved and the expected heat sink temperature increase is less than 5 K, which is beneficial in terms of a low $R_{DS,on}$ and consequently low conduction losses of the 10 kV SiC MOSFETs.

B. LV-Side 1200 V SiC MOSFET-Based Full-Bridge

The LV-side of the isolated DC/DC converter is realized with 1200 V, 25 mΩ SiC MOSFETs *C2M0025120D* from *Wolfspeed*, since they offer a low on-state resistance and a

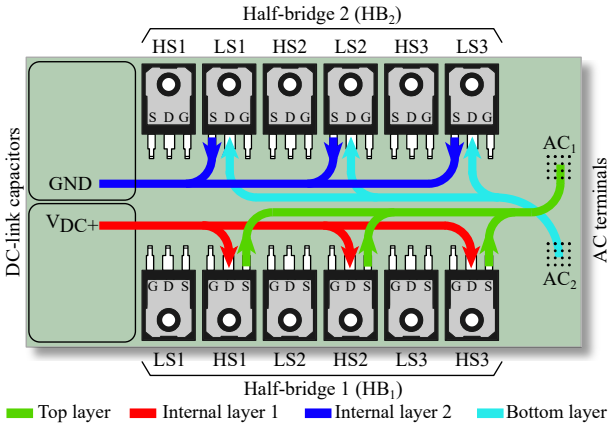

Fig. 6: Bottom-view of the full-bridge layout for symmetrical current path lengths through the individual MOSFETs in the parallel connection. PCB current path only indicated for high-side MOSFETs of half-bridge 1 (HB_1), cf. S_{11} in Fig. 2(a), and low-side MOSFETs of half-bridge 2 (HB_2), i.e. S_{22} in Fig. 2(a). Each switch is composed of three parallel-connected TO247 devices.

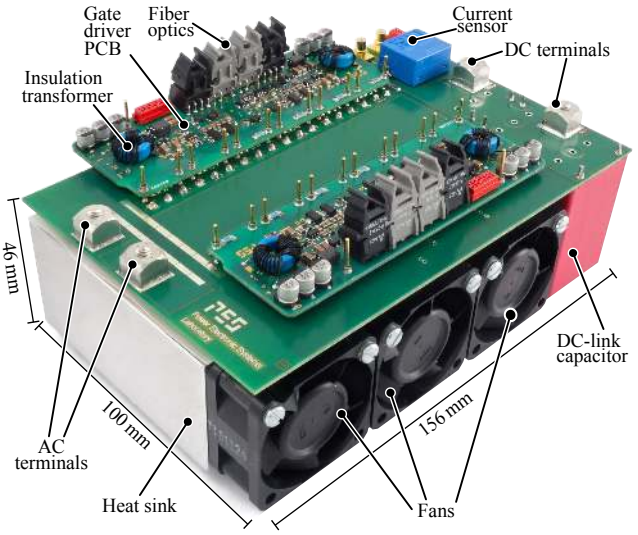

Fig. 7: Picture of the LV-side 1200 V SiC-based full-bridge with three parallel *C2M0025120D* MOSFETs per switch.

certain flexibility for future, e.g. 800 V, applications. However, in order to handle the high current on the LV-side and to reduce the conduction losses, each switch of the LV-side full-bridge consists of three parallel *C2M0025120D* MOSFETs. With the intention of a symmetric current distribution among the three parallel MOSFETs per switch, the current path from the DC-link capacitor through the bridge-legs to the AC-terminals must be symmetric for all MOSFETs. **Fig. 6** shows the realized layout of the full-bridge. The MOSFETs of each half-bridge are lined up between the DC-link capacitors on the left side and the AC terminals on the right side. This ensures an equal current path length through all MOSFETs and guarantees a symmetric current distribution. Furthermore, the high-side MOSFETs (HS1...HS3) and the low-side MOSFETs (LS1...LS3) in each half-bridge are placed alternately in order to minimize the commutation loop inductance. Inductive switching tests show that currents of up to 100 A can be switched without oscillations or an asymmetric current distribution, as the homogeneous temperature distribution observed on thermal images of the MOSFET cooling pads prove.

For an estimation of the LV-side semiconductor losses, the conduction and the switching losses of the LV-side full bridge are calculated. With the LV-side MOSFET rms current $I_{\mathrm{S,LV,rms}}$ and the equivalent on-state resistance $R_{\mathrm{DS,on,LV}}$ of the parallel connection of three *C2M0025120D* MOSFETs given in **TABLE I** (specified for $T_{\mathrm{j}} = 100\,^{\circ}\mathrm{C}$), the conduction losses are $P_{\mathrm{c,LV}} = 113\,\mathrm{W}$.

1) LV-Side Soft-Switching Loss (SSL) Measurements: Similar to the MV-side MOSFETs, also the SSL of the 1200 V SiC MOSFETs are not given in the datasheet. Therefore, calorimetric SSL measurements with *C2M0025120D* MOSFETs are carried out for a drain-source voltage of 400 V and different switched currents. Thereby, an inductor is connected to the AC terminals of the full-bridge, which is soft-switched with a duty cycle of 50 %, leading to symmetrical triangular current in the inductor. The switched current can be varied via the switching frequency or the inductance value, where the MOSFETs always turn off the peak value of the triangular current under ZVS conditions [16], [18]. Besides the conduction losses during the on-state of the MOSFETs, each turn-off event generates a certain amount of SSL in the MOSFETs. The total LV-side semiconductor losses are measured via the temperature increase of the heat sink and its thermal resistance R_{th} (similar as shown in [1]), which is known from calibration measurements with constant DC power. In order extract the SSL out of the total losses, at the same time the conduction losses are determined by measuring the current and the on-state voltage of the MOSFETs with a special on-state voltage measurement circuit (OVMC) [27] during operation. For these SSL measurements, the full-bridge is equipped with only one *C2M0025120D* MOSFET per switch. **Fig. 4(b)** shows the resulting SSL per switching cycle for a DC-link voltage of 400 V and different switched currents, measured with a turn-off gate resistor of $R_{\mathrm{off}} = 2\,\Omega$. As can be seen, the SSL increase approximately linearly with the current for low currents and start increasing disproportionately for currents beyond 20 A.

To verify the measured SSL, a different measurement method is applied. Thereby, the intention is to keep the conduction losses P_{c} constant (by keeping the peak of the triangular current and therewith the switched current I_{sw} constant) and to measure the total semiconductor losses P_{semi1} and P_{semi2} (again thermally via the temperature increase and the R_{th} of the heat sink) at different switching frequencies f_{sw1} and f_{sw2} [28]. Consequently, to keep the peak current constant when the switching frequency is changed, the inductance value has to be adapted accordingly. By taking the difference between the two measured loss values, the conduction losses cancel out and the SSL for the switched current I_{sw} can be calculated as

$$E_{\mathrm{ZVS,LV}}\left(I_{\mathrm{sw}}\right) = \frac{P_{\mathrm{semi2}} - P_{\mathrm{semi1}}}{f_{\mathrm{sw2}} - f_{\mathrm{sw1}}}. \qquad (2)$$

This method has been applied for a switched current of $I_{\mathrm{sw}} = 32.5\,\mathrm{A}$ and as can be seen in **Fig. 4(b)**, the obtained SSL

match very well with the curve obtained with the OVMC, which proves a high accuracy of the measurement method.

With the measured SSL of the LV-side MOSFETs, the SSL during operation of the DC/DC converter can now be determined. Assuming a symmetric current distribution among the three parallel MOSFETs per switch of the full-bridge and a ZVS current of $I_{\mathrm{ZVS,LV}} = 16\,\mathrm{A}$ (cf. **TABLE I**), each MOSFET turns off a current of $I_{\mathrm{ZVS,LV}}/3 = 5.33\,\mathrm{A}$. Consequently, the total LV-side switching losses of the four power switches each consisting of 3 parallel MOSFETs are

$$P_{\mathrm{sw,LV}} = 4 f_{\mathrm{sw}} \cdot 3 E_{\mathrm{ZVS}}\left(I_{\mathrm{ZVS,LV}}/3\right) = 1.56\,\mathrm{W}, \qquad (3)$$

whereby the the switching loss curve in **Fig. 4(b)** is extrapolated towards lower currents in order to obtain the SSL value for a switched current of $5.33\,\mathrm{A}$. As can be noted, the SSL of the LV-side are very small, considering the system power rating of $25\,\mathrm{kW}$. However, in e.g. a phase shifted dual-active bridge topology, where the MOSFETs would be turned off at the peak of the current [29], [30], the SSL would become significant.

2) LV-side Full-Bridge Hardware: **Fig. 7** shows a picture of the realized $1200\,\mathrm{V}$ SiC-based LV-side full-bridge. It consists of a 4-layer power PCB ($140\,\mu\mathrm{m}$ outer and $105\,\mu\mathrm{m}$ inner copper thickness), which holds the MOSFETs, the DC-link capacitors, the heat sink as well as the fans, and two gate drive PCBs with isolated auxiliary supplies, each driving one half-bridge. The gate signals are received via optical fibers from a central DSP-board. Furthermore, current and voltage measurement circuits are implemented for control and monitoring purposes. As can be seen, the bridge is highly compact with dimensions of only $156 \times 100 \times 46\,\mathrm{mm}$.

C. Resonance Capacitor

As shown in **Fig. 2(a)**, the resonance capacitor C_{r} is connected in series to the LV-side winding of the transformer and it not only acts as resonance capacitor but also as DC-blocking capacitor in case the voltage applied from the LV-side full-bridge contains a small DC offset, e.g. due to incorrect switching times resulting from discretization errors in the DSP. Further reasons not to place the resonance capacitor on the MV-side are the split DC-link on the MV-side, which already takes care of the DC-blocking, and the fact that no MV-insulation of the resonance capacitor is required on the LV-side. The capacitance of C_{r} can be calculated via the leakage inductance of the transformer (as well as the additional stray inductance of the busbars) and the desired resonance frequency, which is equal to the switching frequency f_{sw} and results in $C_{\mathrm{r}} = 3.8\,\mu\mathrm{F}$. Care must be taken when the DC-link capacitors are comparably small and start influencing the resonance [31]. Due to the high transformer LV-side current of $70.6\,\mathrm{A}$ (cf. **TABLE I**), which also flows through the resonance capacitor C_{r}, a low-loss capacitor with a high current rating is required. Therefore, and with the purpose of offering a high flexibility regarding the value of C_{r}, a parallel connection of 38 *C0G* ceramic capacitors in a 2220 package ($5.7\times5.0\times2.8\,\mathrm{mm}$) with $100\,\mathrm{nF}$ each and a voltage rating of $450\,\mathrm{V}$ is selected. With the dissipation factor of $\tan\delta = 0.05\,\%$, the capacitor losses can be determined as $P_{\mathrm{Cr}} = 2.17\,\mathrm{W}$ at full-load operation. The capacitor array is soldered between two copper plates for the connection to the transformer and the PCB terminal. At full-load operation of the converter, the capacitor temperature under natural convection is only $45\,^{\circ}\mathrm{C}$, which means that no additional cooling is required.

D. MF MV Transformer

One of the key components of the isolated DC/DC converter at hand is the MF MV transformer, which is responsible for the voltage step-down and the galvanic isolation between the MV-side and the LV-side. Although it is well known in power electronics how to design MF transformers (for voltages below $1\,\mathrm{kV}$) and it is well known from power systems how to design the electrical insulation of MV or even high-voltage $50/60\,\mathrm{Hz}$ transformers, the combination of MF and MV in a transformer is very challenging in many aspects. Only the recent development of SiC MOSFETs with blocking voltages of $10\ldots15\,\mathrm{kV}$ and their outstanding soft-switching capabilities allow for the combination of switching frequencies around $50\,\mathrm{kHz}$ and switched voltages in the $5\ldots10\,\mathrm{kV}$ range. With these conditions and the aim for a highly compact design (which directly excludes oil as insulation and cooling medium for this power level due to the required oil-expansion tank and dehydration breather), two major problems arise. Due to the MV, the insulation material layer, which encapsulates the MV winding and isolates it from the LV-winding and the core, has to be chosen rather thick. However, the losses of the MV winding have to be extracted by heat conduction through the insulation material, which typically features only a very low thermal conductivity. Furthermore, in a highly compact transformer, the surface area for the heat extraction is small and consequently, the cooling of the MV-winding is very challenging. Secondly, due to the combination of the high switching frequency and the high switched voltage, dielectric losses inside the insulation material can lead to local hotspots, to thermal degradation and even to a thermal runaway [23]. Consequently, it is important to select a suitable insulation material and to consider the dielectric losses during the design process of the MF MV transformer.

1) Transformer Pareto Optimization: With the purpose of achieving a highly compact and efficient transformer, it is optimized with respect to power density and losses. For the high targeted efficiency and power density, only ferrite core material, litz wire and shell-type windings are considered. While the magnetizing inductance, the core material (BFM8) and the isolation distances are fixed, a sweep over the following parameters is carried out and the winding, the core, and the dielectric losses within the transformer operated at nominal power are determined by coupled FEM simulations:

- operating frequency;
- core shape (U-core or E-core);
- core dimensions;
- number of layers and chambers on the MV-side;
- number of turns on the MV and the LV-side;
- litz wire diameter and number of strands;
- strand diameter.

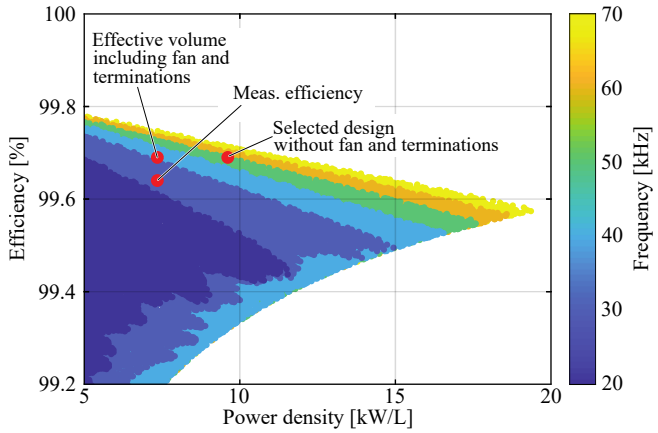

Fig. 8: Volume/loss Pareto optimization of the MF MV transformer for different operating frequencies (color-coded). The optimization does not include the volume of the fan and the terminations. Therefore, these volumes are added separately and the effective volume is indicated in the figure. Additionally, the measured efficiency, which is slightly lower than the simulated efficiency (99.64 % compared to 99.69 %, i.e. 0.05 % difference), is shown.

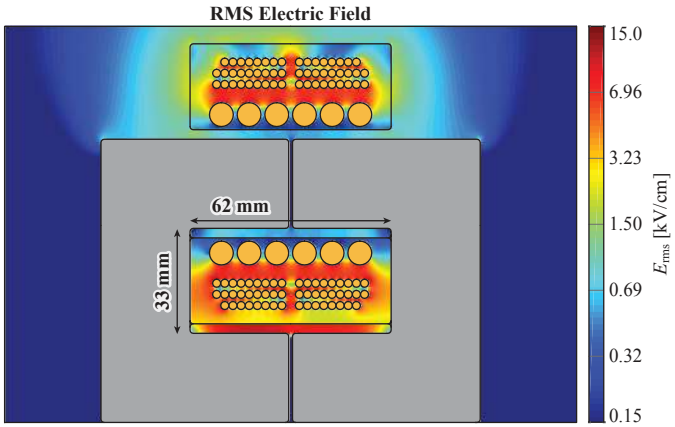

Fig. 9: FEM simulation of the electric field distribution (rms values) of the transformer for a $\pm 3.5\,\mathrm{kV}/400\,\mathrm{V}$ excitation.

TABLE II: Key parameters of the realized MF MV transformer.

Parameter	**Value**
Nominal power	25 kW
Operating frequency	48 kHz
Terminal voltages	$\pm 3.5\,\mathrm{kV}/\pm 400\,\mathrm{V}$
Winding	52:6 turns, litz wire, shell-type
MV litz winding	$630 \times 71\,\mu\mathrm{m}$, three layers, two chambers
LV litz winding	$2500 \times 100\,\mu\mathrm{m}$, single layer
Core type	U-core, BFM8 ferrite, $2500\,\mathrm{mm}^2$
Air gap	$2 \times 1.1\,\mathrm{mm}$
Insulation	4.0 mm thickness, designed for 15 kV

The simulations include high-frequency effects in the litz wire [32]–[34], the fringing field of the air gap [35], and the effects of the non-sinusoidal magnetic flux by calculating the core losses via iGSE [36]. During the simulation, transformer designs which exceed a certain current density in the windings, a certain core loss density, or a certain dielectric loss density in the insulation material, are discarded in order to avoid designs which would cause a thermal runaway of the transformer. **Fig. 8** shows the results of the Pareto optimization of the transformer for different operating frequencies. As can be seen, there is a trend towards higher possible efficiencies and power densities for an increasing operating frequency. However, the efficiency gain between 50 kHz and 70 kHz is rather insignificant and a selection of a high switching frequency would also lead to an increase of the soft-switching losses and hence to a decrease of the total converter efficiency. In order to reach the DC/DC converter's full-load efficiency goal of 99.0 %, the maximum allowed transformer losses are 75 W, given the fact that the MV-side and the LV-side bridges, the resonance capacitor, the auxiliary supplies, and the fans together generate around 175 W of losses. Therefore, a design with a calculated efficiency of 99.69 % and an operating frequency of 48 kHz is selected. The chosen transformer is a U-core design, which features a larger exposed area of the winding package for the forced convective cooling and an easier construction of the litz wire terminations compared to E-core designs. The chosen transformer is pointed out in **Fig. 8** and as indicated, if the volumes of the fan and the litz wire terminations are included, the power density slightly decreases. Furthermore, the design point of the realized transformer with its calorimetrically measured efficiency (cf. Section III-D5) is shown in the Pareto plot and as can be noted, the simulated and the measured efficiencies (99.69 % and 99.64 %, respectively) are very close, which indicates an accurate simulation as well as an accurate measurement of the transformer losses.

TABLE II lists the key parameters of the realized transformer design and as can be noted, a two-chamber winding is selected on the MV-side in order to reduce the electric field stress between the three layers of the MV-winding, which increases the reliability of the electric insulation. For a deeper analysis of the electric field strength inside the transformer winding package and the surrounding air, the result of a 2D FEM simulation is shown in **Fig. 9**, whereby the insulation material has been modeled with its permittivity given in **TABLE III**. As can be seen, the maximum rms electric field is $15\,\mathrm{kV/cm}$ and the peak value is more than 10 times below the electric breakdown field strength of the utilized insulation material. It has to be noted that a higher electric field would lead to quadratically higher dielectric losses

$$P_{\mathrm{ins}} \propto E^2 \cdot f_{\mathrm{sw}} \cdot \tan\delta, \tag{4}$$

and possibly to partial discharges, which both would enhance the material's ageing process due to local hot spots and degradation. As will be shown by calorimetric measurements in Section III-D5, the dielectric losses account for a significant part of the total transformer losses and cannot be neglected as in case of MF LV transformers.

2) Construction of the Transformer Windings: Due to their different electric potentials, the MV and LV windings have to be isolated from each other by an electric insulation material. In order to guarantee that the insulation material thickness between the MV and the LV-winding is constant at a value of 4.0 mm, the MV and the LV-winding are wound on individual 3D-printed coil formers (material: polycarbonate) and assembled concentrically, as shown in **Fig. 10**. With this

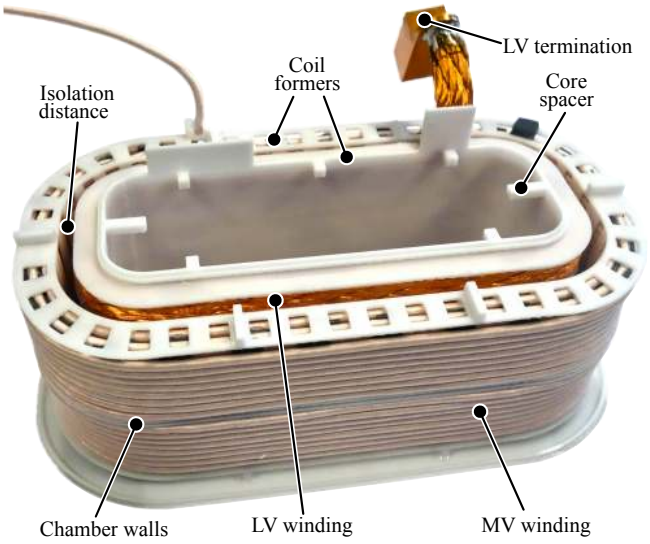

Fig. 10: Picture of the MV and LV transformer windings on their 3D-printed coil formers. The isolation distance between the MV and the LV windings, as well as the chamber walls separating the two MV winding chambers can be seen.

arrangement, the LV-winding acts as an electric field shield between the MV-winding and the core and therefore, no MV-insulation is required on the surface of the LV-winding which faces the core. For the cooling of the windings, the LV coil former is equipped with core spacers (cf. **Fig. 10**), which separate the core from the winding package by a certain distance and allow an air flow to pass in between. Furthermore, polypropylene spacers are used between the three layers of the MV winding in order to keep a distance of $0.8\,\mathrm{mm}$ between the individual layers, such that the insulation material can flow into the interspaces during the subsequent potting process. Additionally, for the monitoring of the winding temperature, several NTC temperature sensors are placed close to the LV-windings. Once the windings are assembled, the HF litz wires are soldered into the intended copper terminations to guarantee a low contact resistance.

3) Vacuum Pressure Potting of the Transformer Windings: For the potting of the windings, the coil formers are closed with another 3D-printed part, resulting in a sealed winding package which is then filled up with the insulation material. As already mentioned, standard insulation materials such as Epoxy resins are unsuitable for MF MV applications due to their typically low thermal conductivity and/or high dielectric losses. Therefore, a two-component silicone compound (containing thermally conductive particles) of type *TC-4605 HLV* from Dow Corning is used. The properties of this material are listed in **TABLE III**. An additional advantage compared to

TABLE III: Properties of the utilized silicone *Dow Corning TC-4605 HLV*.

Property	Value
Dielectric strength	$24\,\mathrm{kV/mm}$
Dielectric constant ε_r	< 4.1 for $f > 50\,\mathrm{kHz}$
Dissipation factor $\tan\delta$	$< 0.8\,\%$ for $f > 50\,\mathrm{kHz}$
Thermal conductivity	$1\,\mathrm{W/(m\,K)}$

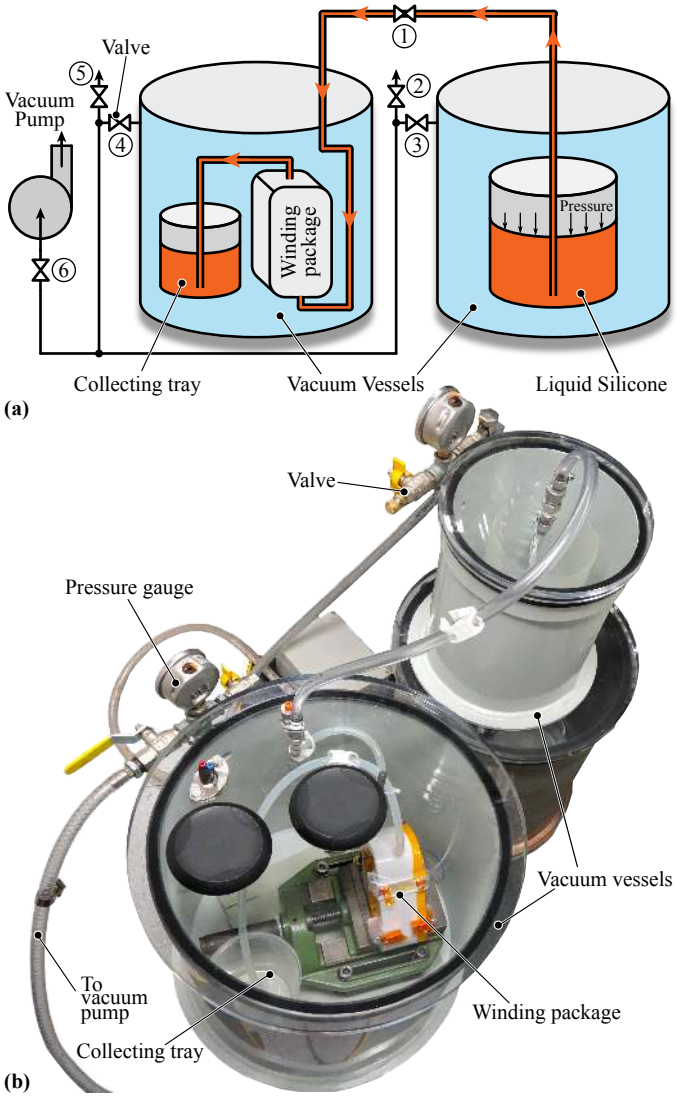

Fig. 11: **(a)** Schematic drawing and **(b)** picture of the silicone vacuum pressure potting (VPP) process of the transformer winding package. Both vessels are evacuated ($30\,\mathrm{mbar}$) to devolatilize the liquid silicone. Then, the pressure in the right vessel is increased, pressing the silicone through the tubes into the sealed winding package, from where the excessive silicone flows into a collecting tray. After the filling process, the pressure is increased to atomspheric pressure again, in order to compress possible vacuum cavities. Finally, the silicone is cured at $120\,^\circ\mathrm{C}$.

epoxy resin is the mechanical flexibility of the silicone, which prevents it from cracking during the curing.

The utilized silicone shows outstanding dielectric and thermal properties but reacts highly sensitively to amines, amides, nitriles, and alcohols etc. during the curing process. These substances might be contained e.g. in adhesives used for the mechanical fixing of the turns during the construction of the windings. When the still liquid silicone comes in contact with one of these substances, it might not cure properly, preventing it from developing its dielectric properties [37]. Therefore, the compatibility of the silicone to any adhesives or in general to any materials contained in the winding package has to be verified. It has been found that e.g. cyanoacrylate-based instant adhesives and UV adhesives are unsuitable, whereas two-component instant adhesives, such as *LOCTITE 3090*, for

example, have been used successfully.

To guarantee a high reliability of the MV-insulation, the insulation material must be free of cavities or other imperfections, which can lead to partial discharges. To achieve this, a vacuum pressure potting (VPP) process, as shown in **Fig. 11(a)**, is used. Thereby, the already mixed liquid two-component silicone and the winding package are placed in two separate vessels. With a vacuum pump, both vessels are evacuated down to a pressure of $30\,\mathrm{mbar}$ while valves ①, ③, ④ and ⑥ are open. Since there is no silicone yet in the collecting tray, the tubings and the sealed winding package are evacuated as well. After a certain time, when the liquid silicone is devolatilized, valves ④ and ⑥ are closed. The pressure in the right vessel is then slightly increased by shortly opening valve ②, which presses the liquid silicone into the tubings and from bottom to top through the winding package. To remove possible cavities inside the winding package, this process is not stopped before approximately $300\,\mathrm{mL}$ of the liquid silicone have flown through the winding package into the collecting tray. For the further steps, it is important that both ends of the tubings are located below the surface of the liquid silicone, such that no air can enter. Now, valve ① is closed and both vessels are pressurized again to atmospheric pressure, compressing possible vacuum cavities inside the winding package. Finally, the tubes entering and leaving the winding package are clamped to avoid any further flow of the silicone and the winding package is cured for several hours at a temperature of $120\,^{\circ}\mathrm{C}$ in order to activate the adhesion of the silicone to other materials. The best results regarding adhesion are achieved when the temperature is applied directly after the VPP process, although the curing itself does not require an increased temperature. However, if the temperature is only applied after the curing at room temperature, the silicone might detach from the coil former, leading to undesired vacuum or air cavities between the coil former and the silicone. **Fig. 11(b)** shows a picture of the VPP setup with the two vacuum vessels and the sealed winding package. The covers of the vacuum vessels are made out of acrylic glass and each vessel is equipped with a pressure gauge to enable the monitoring of the process by eye.

4) Transformer Prototype: The assembled transformer consisting of the winding package and the ferrite cores is shown in **Fig. 12**. As can be seen, the core spacers of the winding package separate it from the core by a certain distance, forming an air channel for the forced convective cooling of both, the core and the windings. However, since the insulation between the LV-winding and the inner wall of the winding package is not designed for MV but only for LV (cf. **Fig. 9**) and the core spacers represent a direct creepage path between the winding package and the cores, the cores must be tied to ground potential. For this reason, a grounding bar is attached to the ferrite cores with the help of a conductive silver adhesive.

For the verification of the electrical insulation of the transformer, a DC voltage of $20\,\mathrm{kV}$ has been successfully applied to the MV-winding for one hour.

In operation, the transformer is cooled by a fan (not shown), which provides an air flow onto the cores, the winding package and through the air channel in between. The dimensions of the

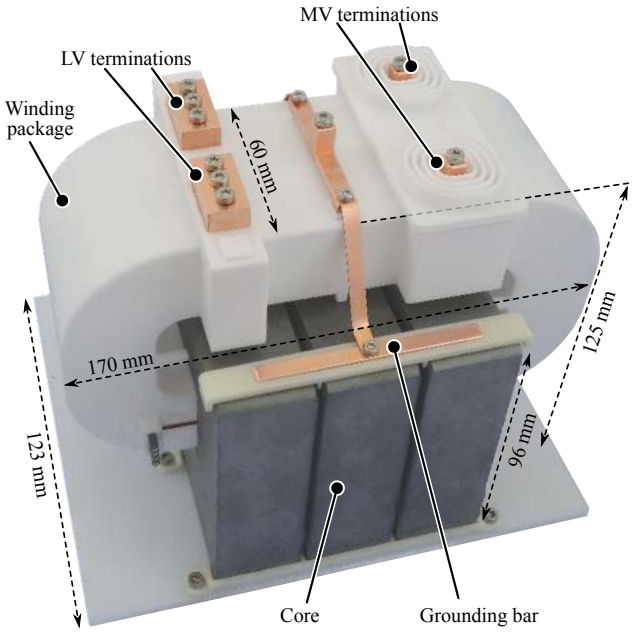

Fig. 12: Picture of the realized $25\,\mathrm{kW}$ MF transformer consisting of three BFM8-ferrite U-core sets and the winding package with the mounted MV-side and LV-side terminations.

transformer are indicated in **Fig. 12** and the boxed volume of the transformer itself is $2.6\,\mathrm{L}$ and the volume is $3.4\,\mathrm{L}$ when also the terminations and the fan are included. Therefore, the $25\,\mathrm{kW}$ MF MV transformer achieves a power density of $7.35\,\mathrm{kW/L}$ (including the fan and the terminations).

5) Transformer Measurements: To characterize the efficiency of the transformer as one of the key components of the isolated DC/DC converter at hand, electrical or calorimetric measurement methods can be applied. However, literature has shown that electrical efficiency measurements of highly efficient systems (either converters or individual power components) are inaccurate, even in case the input and output voltages and currents are DC or $50\,\mathrm{Hz}$ AC [1]. Consequently, even larger measurement errors can be expected in case of an electric efficiency measurement of an MF MV transformer operated with switched voltages due to skews between the voltage and current measurements and the limited bandwidth of the measurement devices. Therefore, instead of electrically measuring the input and output power of the transformer to determine its efficiency, its losses are directly measured calorimetrically. With the aim of not only determining the total losses of the transformer but also the loss distribution among the windings, the core, and the insulation material, these loss components are measured independently in a highly accurate two-chamber calorimeter [38].

Fig. 13(a) shows the measurement setup for the determination of the winding losses. For this purpose, the LV-winding of the transformer is shorted, and since the currents during the operation of the DC/DC converter are quasi-sinusoidal, a sinusoidal current with a frequency of $48\,\mathrm{kHz}$ (which is the operation frequency of the DC/DC converter) is impressed into the MV-winding. Due to the short-circuit on the LV-side, the magnetic flux in the core is nearly zero and no core

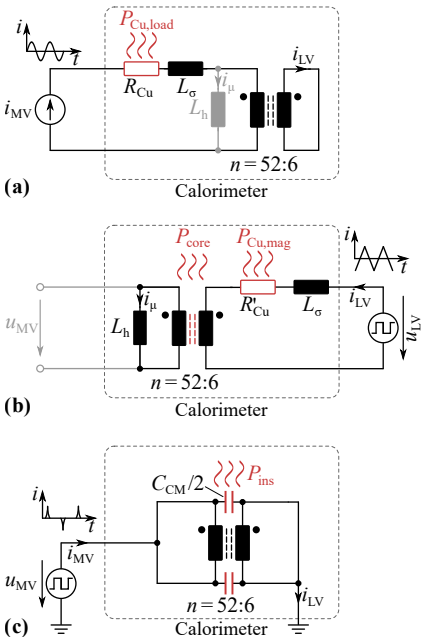

Fig. 13: Calorimetric measurement setups for **(a)** the winding losses, **(b)** the core losses, and **(c)** the dielectric losses P_{ins} in the insulation material of the transformer.

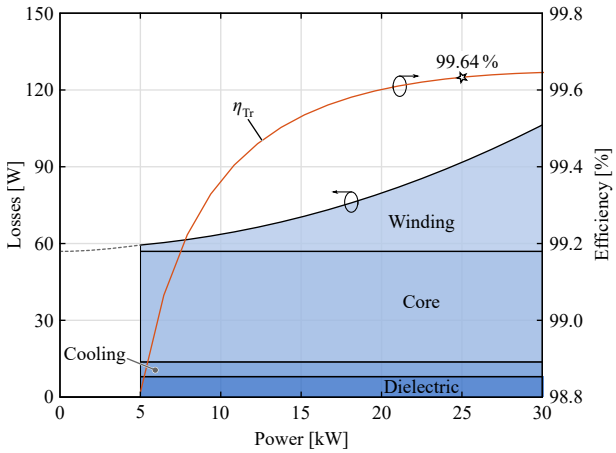

Fig. 14: Calorimetrically measured distribution of the transformer losses together with the transformer efficiency curve. At the rated converter power of 25 kW, the transformer efficiency reaches 99.64 %.

losses but only the winding losses $P_{\mathrm{Cu,load}}$ in the equivalent resistance R_{Cu} of both windings caused by the sinusoidal load current occur and can be measured calorimetrically for different amplitudes (i.e. different loads).

Furthermore, the circuit for the measurement of the core losses is shown in **Fig. 13(b)**. Thereby, the MV-side of the transformer is left open, while a rectangular voltage is applied to the LV-winding, creating a triangular magnetizing current and magnetic flux with equal values as during real operation of the DC/DC converter. Besides the actual core losses P_{core}, also the small part of the ohmic and air-gap fringing-field-related winding losses $P_{\mathrm{Cu,mag}}$ generated by the magnetizing current during DC/DC operation is measured, but together with the losses from the winding loss measurement with the sinusoidal load current (cf. **Fig. 13(a)**) adds up to the correct total winding losses, i.e. $P_{\mathrm{Cu}} = P_{\mathrm{Cu,load}} + P_{\mathrm{Cu,mag}}$. Furthermore, in this arrangement, the dielectric losses in the insulation material are present as well. However, the dielectric losses are measured individually (as shown below) to separate them from the core losses.

Since the losses of ferrite material is typically strongly temperature dependent, the core temperature during the core loss measurement must be equal to the core temperature during the operation of the DC/DC converter. Due to the air-channel between the winding package and the ferrite cores of the transformer, their thermal coupling is extremely low. Accordingly, the core temperature and hence the core losses are not significantly influenced by the winding temperature during the converter operation. For this reason, the core temperature and therewith the core losses can be assumed as constant over the whole power range, since always the same voltage time area is applied to the transformer independently of the transferred power.

As already mentioned, due to the combination of the high voltage and the high frequency, dielectric losses occur in the insulation material. To determine these losses by measurement, the circuit in **Fig. 13(c)** is used. As can be seen, the transformer is shorted on both sides and grounded on the LV-side. The MV-side is excited by a rectangular voltage generated by the MV-side bridge-leg (cf. Section III-A) with the same frequency (48 kHz), rise time (600 ns), and amplitude (±3.5 kV) as during real converter operation. Thereby, the parasitic common-mode (CM) capacitances C_{CM} between the MV and the LV-winding are charged and discharged, which in combination with a certain dissipation factor $\tan\delta$ causes dielectric losses that are measured calorimetrically. As can be noticed, with this pure CM excitation, only the CM-component of the dielectric losses are included. However, in converter operation, there is also a differential-mode (DM) voltage across the MV-winding, which causes dielectric losses in the inter-layer insulation as well. To also include these losses, the electric field FEM simulation (cf. **Fig. 9**) is calibrated in such a way that the pure CM insulation losses match with the measurement, before the simulation is extended to also include the DM losses.

The distribution of the calorimetrically measured transformer losses is shown in **Fig. 14** together with the efficiency curve over the load range from 5 kW to 30 kW. Besides the winding, core and dielectric losses, the losses caused by the fan for the cooling of the transformer are also included. As can be seen, at full load (25 kW), the measured efficiency reaches 99.64 %. Furthermore, with a loss distribution of $P_{\mathrm{Cu}} = 34.8\,\mathrm{W}$ (winding losses), $P_{\mathrm{core}} = 43.2\,\mathrm{W}$ (core losses), $P_{\mathrm{ins}} = 8.0\,\mathrm{W}$ (dielectric losses), and $P_{\mathrm{cooling}} = 5.8\,\mathrm{W}$ (cooling losses), it can be noted that the dielectric losses account for 9 % of the total transformer losses and indeed have to be considered in MF MV transformer designs, especially regarding a possible thermal runaway.

If for the calorimetric transformer loss measurement the following measurement errors are assumed (core losses 25 % (due to the strong temperature dependency), winding losses 20 %, dielectric losses 40 % (since only the CM part is measured and the DM part is determined by a re-calibrated simulation),

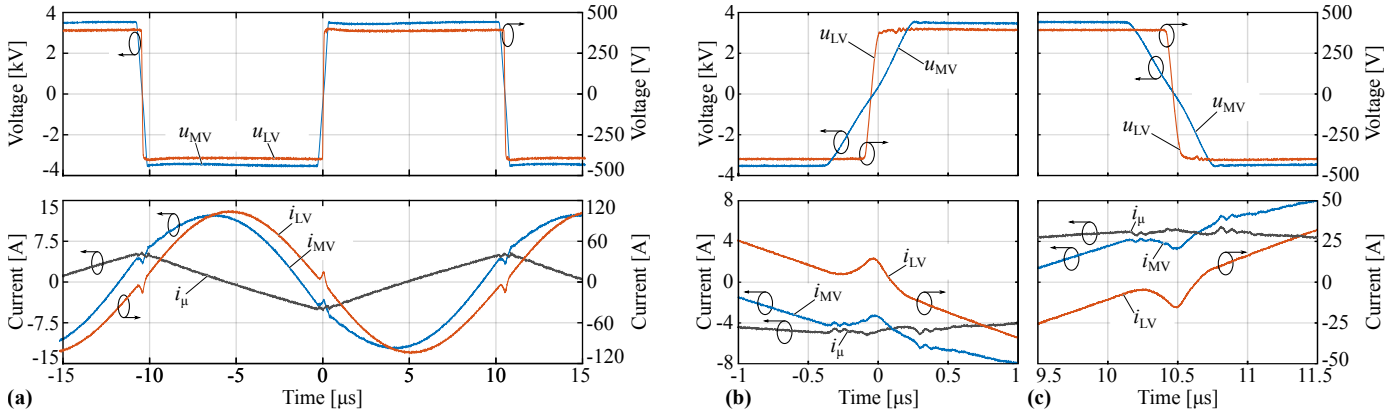

Fig. 15: **(a)** Measured voltage and current waveforms during 25 kW operation of the converter. The magnetizing current i_μ is determined as the difference between the MV-side current i_{MV} and the transformed LV-side current i_{LV}. **(b) & (c)** Magnified views of the voltages and currents during the rising and falling voltage transition, respectively. Practically the total magnetizing current i_μ is available for ZVS on the MV-side, whereas the current spikes are utilized for achieving ZVS on the LV-side.

and cooling power 2 %), a total efficiency measurement error of $\pm 0.08\,\%$ results for the transformer, i.e. its efficiency is in the range of $99.64\,\% \pm 0.08\,\% = (99.56\,\% \ldots 99.72\,\%)$.

IV. Experimental Setup and Results

For the experimental verification and the efficiency evaluation of the realized DC/DC converter, an appropriate test setup is required. Due to its bidirectionality, the converter can either be supplied from the LV-side or the MV-side, whereby the transferred power is dissipated in a variable load resistor in order to be able to operate the converter at different power levels. In this case, the converter is supplied from the 400 V-side by two paralleled 0...500 V, 0...40 A power supplies (*Regatron TopCon Quadro TC.P.16.500.400.S*). During converter operation, the voltages and currents at the transformer terminals are measured especially in order to see whether or not the converter is operated under ZVS conditions on both sides. For this purpose, a *LeCroy HDO4054A* oscilloscope in combination with *Pearson* current transformers and differential voltage probes (*LeCroy HVD3605*) is used.

For the measurement of the complete system efficiency, the losses of all main power components have to be measured. As already mentioned, calorimetric measurement methods achieve a much higher accuracy compared to electrical measurement methods. Since the efficiency curve of the transformer is already characterized calorimetrically (cf. **Fig. 14**), the remaining main sources of losses are the 10 kV SiC MOSFETs on the MV-side and the 1200 V SiC MOSFETs on the LV-side. The power demand of the auxiliary supplies for the gate drivers and the cooling system can easily be measured electrically, whereby the relatively small losses of the resonance capacitor C_{r} are taken from the calculation in Section III-C.

For the accurate measurement of the semiconductor losses, the steady state temperature increase of their heat sinks is measured and together with the thermal resistances of the heat sinks, which are known from calibration measurements with constant power, the semiconductor losses can be determined accurately [1]. While high precision NTCs are used for the measurement of the heat sink temperature on the LV-side, a fiber-optic measurement system (*Optocon FOTEMPMK-19*), which measures the temperature at the tips of up to 10 non-conductive optical fibers, is used to determine the temperature of the floating heat sinks on the MV-side. Due to the relatively small temperature increase of the MV-side heat sinks of $\Delta\vartheta_{\mathrm{ss}} = 4\,\mathrm{K}$ at full-load and a resolution of 0.2 K of the fiber optic temperature measurement, the measurement error is 10 %. Together with an assumed deviation of the thermal resistance of 5 %, the maximum expected error (for the full-load operating point) is $e_{\mathrm{HS,MV}} = 15\,\%$ (with the propagation of uncertainty theory, i.e. the geometric sum of the errors, the total error would only be 11.2 %). On the LV-side, however, the resolution of the NTCs used for the temperature measurement is 0.1 K and leads together with a steady state temperature increase of 16.5 K at full-load to a measurement error of 1.2 %. With an assumed deviation of the thermal resistance of 5 %, the worst case error of the LV-side semiconductor loss measurement is $e_{\mathrm{HS,LV}} = 6.2\,\%$ (or 5.1 % when the propagation of uncertainty theory is considered).

A. Measured Waveforms

Fig. 15(a) shows the measured voltage and current waveforms at the MV-side and the LV-side transformer terminals during full-load operation (25 kW) of the DC/DC converter, together with the magnetizing current obtained by taking the difference between the MV-side and the transformed LV-side current. As can be seen, the waveforms are smooth and are free of any oscillations, which verifies the careful design of the converter. In **Fig. 15(b) & (c)**, a magnified view of the waveforms in the vicinity of the rising and falling voltage transitions is shown. It can be seen that the MV-side switches almost the entire magnetizing current, whereby the LV-side switches the current peak generated by the different rise/fall times of the MV-side and the LV-side voltage transitions. This means that both, the MV and the LV-side are operated under ZVS conditions and since the magnetizing current is load-independent, ZVS is achieved over the complete load range without the need for adjusting any parameters such as e.g. the phase shift or the switching frequency. During the

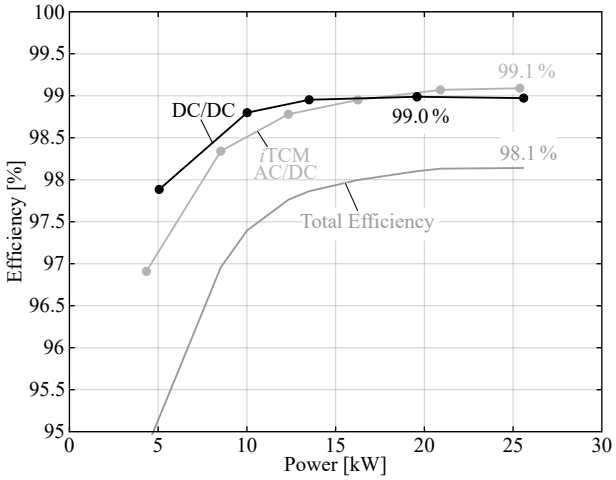

Fig. 16: Calorimetrically measured efficiency of the realized DC/DC converter. An efficiency of 99.0 % is achieved above 13 kW. Together with the *i*TCM AC/DC converter presented in [1], a full-load efficiency of the complete SST-system (cf. **Fig. 1**) of 98.1 % is reached.

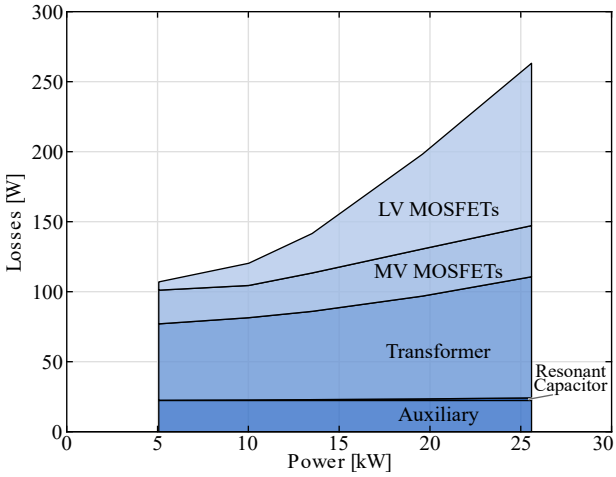

Fig. 17: Measured loss distribution of the DC/DC converter's main components over the power range from 5 kW to 25.6 kW.

measurements at different power levels, the robustness of the SRC against small changes in the switching frequency and the phase shift has been tested, especially regarding whether or not all semiconductors operate under ZVS conditions. Thereby, it has been found that the modulation is extremely robust and that ZVS is maintained even for changes in these parameters of up to ±10 %. Comparing the measured waveforms in **Fig. 15** to the simulated waveforms in **Figs. 2 & 3**, an almost perfect matching can be noticed.

B. Efficiency Measurements

One of the most important key features of a power electronic converter is its efficiency, since the related energy losses are closely coupled to the operating costs of the converter during its lifetime. Therefore, the efficiency of the DC/DC converter is characterized for different loads between 5 kW and 25.6 kW. The calorimetrically measured efficiency curve is shown in **Fig. 16**. As can be seen, an efficiency of 99.0 % in the power range between 13 kW and 25 kW is achieved. This means that, in contrast to similar converters [21], [39], [40], the realized DC/DC converter not only achieves three times less (relative) full-load losses, but is also well suited for partial load operation, e.g. in a redundant system, where two converters in parallel supply a critical load and are therefore operated at 50 % of their rated power [41]. Furthermore, in **Fig. 16**, also the efficiency curves of the *i*TCM PFC AC/DC converter described in [1] and of the complete SST are shown. Together with the full-load efficiency of 99.1 % of the AC/DC converter, the full-load efficiency of the 3.8 kV AC to 400 V DC SST reaches a value of 98.1 %. With the given accuracy of the individual calorimetric measurements, the accuracy of the total DC/DC efficiency is ±0.08 %, i.e. the efficiency is between 98.92 % and 99.08 %.

For a deeper analysis of the individual loss components of the DC/DC converter, **Fig. 17** shows the calorimetrically measured loss distribution. As can be seen, the LV-side MOSFETs and the transformer are responsible for the largest share of the losses, whereby the MV-side MOSFETs, the auxiliary supply power, and the resonance capacitor losses account for only a minor loss contribution. Whereas the transformer losses cannot be improved significantly any more (due to the given material properties), the LV-side MOSFET losses of 116 W (which match very well with the calculated losses of 113.8 W) could easily be decreased by a factor of two by replacing the 2nd generation 1200 V, 25 mΩ SiC MOSFETs with the latest 3rd generation 900 V, 11.5 mΩ SiC MOSFETs. However, even then the LV-side MOSFET conduction losses would still be significantly higher compared to the MV-side MOSFET conduction losses. To obtain equal conduction losses in both, the MV and the LV-side MOSFETs, the following conditions would have to be fulfilled, whereby the factor of two arises from the half-bridge/full-bridge configuration (magnetizing current neglected):

$$2R_{\mathrm{DS,on,LV}} \cdot \left(\frac{P}{U_{\mathrm{DC,LV}}}\right)^2 = R_{\mathrm{DS,on,MV}} \cdot \left(\frac{2P}{U_{\mathrm{DC,MV}}}\right)^2, \quad (5)$$

$$R_{\mathrm{DS,on,LV}} = 2R_{\mathrm{DS,on,MV}} \cdot \left(\frac{U_{\mathrm{DC,LV}}}{U_{\mathrm{DC,MV}}}\right)^2 = \frac{R_{\mathrm{DS,on,MV}}}{153}. \quad (6)$$

Consequently, based on an MV-side on-state resistance of $R_{\mathrm{DS,on,MV}} = 400\,\mathrm{m\Omega}$, the LV-side on-state resistance would have to be $R_{\mathrm{DS,on,LV}} = 2.6\,\mathrm{m\Omega}$ according to (6) for equal MV and LV-side conduction losses. Such a low on-state resistance could be achieved by using e.g. 5 parallel 900 V, 11.5 mΩ SiC MOSFETs per switch. However the total SiC chip area on the LV-side would be 4.8 times higher than the total SiC chip area on the MV-side in this case. This underpins the extremely good performance of the 10 kV SiC MOSFET technology, or in other words, as long as the $R_{\mathrm{DS,on}}$ does not scale better than quadratically with the blocking voltage for the same chip area (cf. (6)), the MV-MOSFETs will always outperform the LV-MOSFETs. This can be explained by the fact that the SiC MOSFET channel resistance becomes much less significant compared to the SiC bulk resistance with increasing blocking voltage, therefore the total $R_{\mathrm{DS,on}}$ is closer to its theoretical limit for MOSFETs with higher breakdown voltage [42].

Furthermore, comparing the measured full-load MV-side MOSFET losses of $36.5\,\mathrm{W}$ to the calculated losses of $47.1\,\mathrm{W}$, a significant difference can be noticed. This can be explained by the antiparallel SiC JBS diode chip (*CPW3-10000-Z020B*) contained in the $10\,\mathrm{kV}$ modules. With a forward voltage threshold of $1\,\mathrm{V}$ and a differential resistance of $300\,\mathrm{m\Omega}$, circuit simulations show that the JBS diode conducts a significant part of the load current during full-load converter operation with a power flow from the LV-side to the MV-side. This results in an equivalent $R_{\mathrm{DS,on}}$ of $232\,\mathrm{m\Omega}$ and total MV-side conduction losses of $16.7\,\mathrm{W}$ instead of $28.8\,\mathrm{W}$ calculated with the $R_{\mathrm{DS,on,MV}}$ of $400\,\mathrm{m\Omega}$ of the MOSFET chip itself. Thus, together with the MV-side switching losses of $P_{\mathrm{sw,MV}} = 18.3\,\mathrm{W}$, the total MV-side semiconductor losses sum up to $35\,\mathrm{W}$, which is very close to the measured value. For a power flow from the MV-side to the LV-side, where the antiparallel JBS diodes do not conduct any current, conduction losses of $28.8\,\mathrm{W}$ would appear and would lead to a slight decrease ($< 0.05\,\%$) of the converter efficiency compared to a power flow from the LV-side to the MV-side.

V. Conclusion

In this paper, a bidirectional isolated $25\,\mathrm{kW}$, $48\,\mathrm{kHz}$, $7\,\mathrm{kV}$ to $400\,\mathrm{V}$ DC/DC converter employing $10\,\mathrm{kV}$ SiC MOSFETs on the MV-side is presented. Due to its tight coupling of the input and output voltages and the ability to achieve zero voltage switching (ZVS) in all semiconductors, a series resonant converter (SRC) topology operated at resonance frequency and therefore implementing a "DC transformer" is selected. Due to the significantly higher parasitic output capacitances C_{OSS} of the $10\,\mathrm{kV}$ MV-side SiC MOSFETs and the consequently much slower voltage transitions compared to the LV-side, a special modulation scheme is required. A small phase shift between the MV-side and the LV-side gate control signals is introduced, which allows an active sharing of the magnetizing current between the MV and the LV-side and therefore enables ZVS on both sides.

The design of all main power components of the DC/DC converter is presented in detail with a focus on the MF MV transformer and its electrical insulation. It is highlighted that the proper selection of the insulation material is extremely important, since a material with a low dissipation factor and a high thermal conductivity is required to not cause a thermal runaway and hence the destruction of the transformer insulation material. Therefore, a thermally highly conductive silicone compound is chosen and the vacuum potting process (VPP) of the winding package is described in detail. For a deeper analysis, the distribution of the transformer losses among the core, the winding, and the insulation material is measured calorimetrically and it is found that the dielectric losses account for $9\,\%$ of the total transformer losses and have to be considered in MF MV transformer designs. The transformer reaches a measured efficiency of $99.64\,\%$ at $25\,\mathrm{kW}$ transferred power.

Measurements at different power levels show that all switches are operated under ZVS and that the modulation scheme is highly robust against changes in e.g. the switching frequency and/or the phase shift. Finally, the converter efficiency is measured calorimetrically in the power range between $5\,\mathrm{kW}$ and $25.6\,\mathrm{kW}$, achieving an efficiency of $99.0\,\%$ between $13\,\mathrm{kW}$ and $25.6\,\mathrm{kW}$, at a power density of $3.8\,\mathrm{kW/L}$ ($63\,\mathrm{W/in^3}$, referenced to $25\,\mathrm{kW}$). Due to the extremely flat efficiency curve, the realized DC/DC converter is also well suited for partial load operation. Furthermore, from the calorimetrically measured loss distribution, it can be seen that the LV-side conduction losses account for the largest part of the converter losses. Accordingly, by simply replacing the $1200\,\mathrm{V}$ LV-side SiC MOSFETs with latest generation $900\,\mathrm{V}$ SiC MOSFETs, the LV-side conduction losses could be decreased by a factor of two, resulting in a total DC/DC efficiency beyond $99.2\,\%$.

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