A 0.1–5 GHz Cryogenic SiGe MMIC LNA

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***Abstract*—In this letter, the design and measurement of the first SiGe integrated-circuit LNA specifically designed for operation at cryogenic temperatures is presented. At room temperature, the circuit provides greater than 25.8 dB of gain with an average noise temperature (T_e) of 76 K $(NF = 1\ \mathrm{dB})$ and S_{11} of -9 dB for frequencies in the 0.1–5 GHz band. At 15 K, the amplifier has greater than 29.6 dB of gain with an average T_e of 4.3 K and S_{11} of -14.6 dB for frequencies in the 0.1–5 GHz range. To the authors' knowledge, this is the lowest noise ever reported for a silicon integrated circuit operating in the low microwave range and the first matched wideband cryogenic integrated circuit LNA that covers frequencies as low as 0.1 GHz.**

***Index Terms*—BiCMOS, cryogenic, heterojunction bipolar transistors (HBT), integrated circuit (IC), low-noise amplifier (LNA), low temperature, noise, SiGe.**

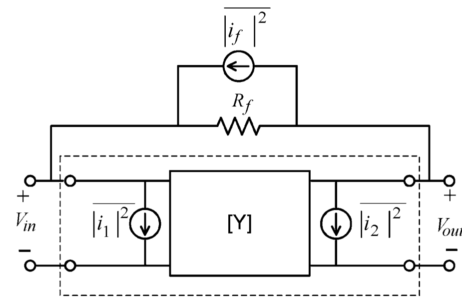

Fig. 1. Generic two-port network with shunt resistive feedback applied. The two-port network is represented in terms of Y-parameters and the noise is represented by an equivalent input and output current source. The feedback network is located outside the dotted line.

I. Introduction

THE sensitivity of a receiving system is limited by its system noise temperature, which is a combination of the input-referred receiver noise and the background noise. For terrestrial communication systems, where the background noise is on the order of 300 K, reducing the noise of the LNA below 77 K, or a 1 dB noise figure, provides diminishing returns as the dominant source of noise is actually the background noise. However, for some applications, such as radio astronomy, deep-space communications, and low-temperature physics research, the background noise is just a few Kelvin. For these applications, the noise requirements are quite stringent and it has become common practice to cryogenically cool the receiver front-end in order to reduce the system noise to within a factor of two of the background noise. Since the early eighties, the amplifiers used in such cryogenic receiver systems have been designed almost exclusively using III-V FET devices [1], which historically speaking, have had much better RF performance than their silicon-based counterparts.

However, as industry has invested billions of dollars into silicon based technologies, the RF performance of devices fabricated in standard CMOS and BiCMOS processes has finally become competitive with III-V FET devices. As discussed at length in [2], the low GHz range noise performance of state-of-the-art SiGe devices having current-gain cutoff frequencies in the low hundreds of GHz is primarily determined by the dc current gain (β) of the device, which sets the ratio of input current noise power to device transconductance.[1]

It has been known for quite some time that band-edge effects occurring due to the introduction of Ge in the base of a SiGe HBT lead to an exponential enhancement of β with cooling [3]. Thus, SiGe HBTs are an excellent candidate for extremely low-noise cryogenically cooled LNAs operating at frequencies up to 10 GHz. However, despite their strong promise, very limited work has been published on the cryogenic noise properties of SiGe HBTs (noise parameters have been measured at 78 K [4] and at 85 K [5]). To the authors' knowledge, no work has been reported on SiGe integrated-circuit LNAs specifically designed for cryogenic operation.

As a first step towards the design of cryogenic SiGe LNAs, the dc characteristics of a large device were measured at 15 K and a simple discrete-transistor cryogenic amplifier which achieved better than 4 K noise temperature from 0.6–3 GHz was designed using the dc data in conjunction with foundry-supplied room temperature capacitance values [2]. Following this result, a device was modeled as a function of bias in terms of noise performance and small-signal model parameters at several temperatures from 15–300 K [6]. Finally, in the work reported here, the small-signal models have been applied to the design of a very broadband matched cryogenic LNA. The organization of this letter is as follows:

1) A theoretical look into the effect of lossy feedback at cryogenic temperatures.
2) A discussion of the amplifier design procedure.
3) The presentation of measurement results.

II. Effect of Lossy Feedback at Cryogenic Temperatures

It is well known that one can achieve an input match through the use of resistive feedback. However, at room temperature,

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[1]In the low frequency limit, $T_{min} \approx (T_a n_c/\sqrt{\beta})$, where T_a is the ambient temperature and n_c is the collector current ideality factor $(n_c = I_C * q/kT_a g_m)$.

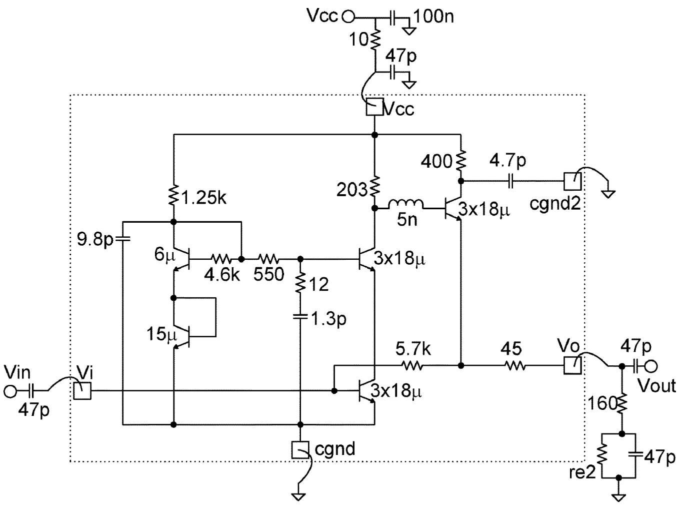

Fig. 2. Schematic diagram including external components. Dotted lines indicate the chip boundary.

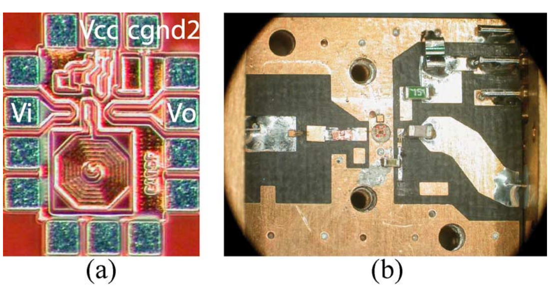

Fig. 3. (a) Fabricated amplifier die photograph. All unlabeled pads are tied to cgnd. The die area is $0.5 \times 0.6\ \mathrm{mm}^2$. (b) Packaged amplifier.

resistive feedback is generally considered to be an unreasonable option for use in very low noise applications as the thermal noise from the feedback resistor contributes an unacceptable amount of noise. However, as the feedback resistor is cooled from 300 K to 15 K, its thermal noise reduces by a factor of 20. Thus, it makes sense to look into the feasibility of using a feedback resistor to provide impedance match without destroying the noise performance of the amplifier. A noise model of a generic network with external lossy feedback appears in Fig. 1. In this work, the network is represented in terms of Y-parameters and has external current noise generators[2] $\overline{|i_1|^2}$ and $\overline{|i_2|^2}$. The feedback network consists of a resistor with a thermal current noise source. It can be shown that at frequencies well below the unity-current-gain cutoff frequency (f_t) of the two-port, its minimum noise and optimum source resistance including the effect of feedback can be approximated as[3]

$$T_{min} \approx \frac{1}{2k}\sqrt{\frac{\overline{|i_1'|^2}\ \overline{|i_2|^2}}{|Y_{21} - g_f|^2}} \tag{1}$$

[2]The internal network is noiseless and the noise parameters are completely described by the two external current generators and their complex correlation coefficient, $\overline{i_1 i_2^*}/|i_1||i_2|$.

[3]It has been assumed in the following that $1/Y_{11} \gg R_S$, $\overline{|i_1|^2} \ll \overline{|i_2|^2}$, and $\overline{|i_1|^2}\ \overline{|i_2|^2} \gg (4kT_a g_f)^2$. These assumptions are valid for SiGe HBTs with high β so long as R_f is much larger than the generator resistance.

and

$$R_{OPT} \approx \frac{2kT_{min}}{\overline{|i_1'|^2}} \tag{2}$$

where k is Boltzman's constant, $g_f = 1/R_f$ is the feedback conductance, and the quantity $\overline{|i_1'|^2} = \overline{|i_1|^2} + 4kT_a g_f$ represents a temperature-dependent equivalent increase in the input current noise power spectral density due to the addition of the feedback resistor to the circuit. Furthermore, if the input transistor is an HBT, it can be shown that $\overline{|i_1'|^2} \approx 2qI_{C1}/\beta_1 + 4kT_a g_f$, where I_{C1} and β_1 are the dc collector current and current gain of the input transistor. Thus, three important effects occurring as a result of the resistive feedback can be highlighted:

1) The minimum noise of the amplifier is multiplied, due to g_f, by a factor of approximately $\gamma = \sqrt{1 + 2\beta_1 kT_a g_f / qI_{C1}} = \sqrt{1 + 2\beta_1 g_f / g_{m,ideal}}$. For a fixed current density, it has been experimentally observed in SiGe HBTs that β rises as roughly $1/T_a$ and T_{min} decreases nearly proportionally with T_a [6].[4] Thus, to first order, γ is independent of temperature and the noise added by the lossy feedback will decrease proportionally to T_a. Finally, in order to avoid degradation of the noise, it is necessary that $\beta g_f \ll g_{m,ideal}/2$.
2) The optimum source resistance of the amplifier decreases by a factor approximately equal to γ.
3) The input resistance becomes $R_{in} \approx R_f/(1 + A_{V,OL})$, where $A_{V,OL}$ is the open loop voltage gain.

Thus it can be seen that by connecting the feedback resistor to a point with high $A_{V,OL}$, its value can be made large (i.e. g_f small) and the desired R_{in} can be obtained with a degradation factor (γ) close to unity.

III. Design Procedure

A schematic diagram of the circuit appears in Fig. 2. The amplifier consists of a cascode stage driving an emitter follower with resistive feedback used to provide input match and is designed such that it can operate from 300 K down to 15 K by changing the value of external resistor $re2$. As the foundry does not provide models to predict performance at cryogenic temperatures, the circuit was designed using a combination of commercial and custom models. To facilitate the cryogenic design, a transistor from the IBM BiCMOS8HP process was first characterized and modeled as a function of both temperature and bias [6]. Using the small-signal models developed for operation at 15 K physical temperature, the amplifier was then designed in AWR's Microwave Office (MWO). Next, simulation was carried out at 300 K in Cadence Virtuoso using foundry supplied models. After verifying that the simulation results at 15 K and 300 K agreed, a layout was generated and parasitic capacitances were extracted. Finally, the parasitic capacitances were back-annotated into the MWO simulation environment and the circuit was compensated for the wiring capacitances. Extracted resistance values were not included in the cryogenic simulations as the conductance of metals increases significantly at cryogenic temperatures.

[4]In [6], the data were presented in terms of $T_{CAS,min}$, which simplifies to T_{min} at low frequencies.

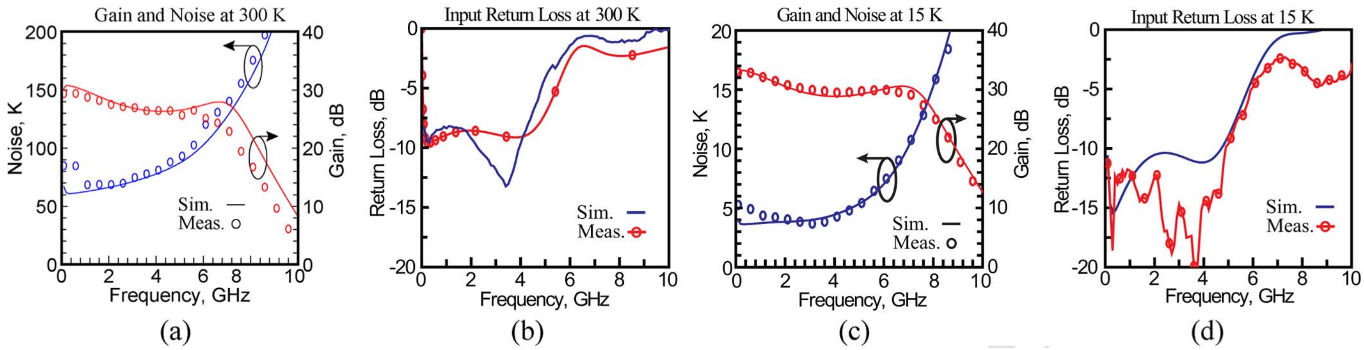

Fig. 4. Gain and noise measured at (a) 300 K and (c) 15 K physical temperature. (b) Return loss measured at 300 K and (d) 15 K. The 15 K noise measurement setup has been calibrated to ±1 K accuracy. To account for packaging effects in the simulation, an input loss of 0.27 dB was assumed at 300 K and the inductance values of bondwires connecting to the amplifier were tuned as the length of each bondwire was not accurately known. The bondwire inductances were assumed to be independent of temperature and were tuned in both the 15 and 300 K simulations simultaneously.

TABLE I
MEASURED PERFORMANCE

Temp. K	Freq. range GHz	T_e@1.5 GHz/3 GHz K	S_{21}@1.5 GHz/3 GHz dB	S_{11}@1.5 GHz/3 GHz dB	S_{22}@1.5 GHz/3 GHz dB	OP1dB dBm	OIP2 dBm	OIP3 dBm	Pdiss mW
15	0.1-5	4.3/3.7	31.7/29.9	-14.1/-14.7	-17.3/-18.2	-10.5	30.5	5.9	20
300	0.1-5	67/75	28.3/27.0	-8.4/-11.8	-16.0/-15.5	-	-	-	76

IV. MEASUREMENTS

The circuit was fabricated in the 0.12 μm IBM BiCMOS8HP process and a die photograph appears in Fig. 3(a). For testing, the amplifier was mounted in an inexpensive package shown in Fig. 3(b) and consisting of a PC board sandwiched in between two gold plated brass carriers [7] with the IC mounted in a VIA hole to minimize bondwire lengths.

Measurements were made at both 15 K and 300 K. Room temperature gain and noise are plotted along with simulation results in Fig. 4(a) and the return loss is plotted in Fig. 4(b). At 300 K, the packaged amplifier has a T_e of less than 92 K (1.2 dB NF) out to 5 GHz with an average gain and T_e of 27.6 dB and 76 K (1.0 dB NF) over the 0.1–5 GHz range. In addition, inspection of Fig. 4(a) and (b) reveals very good agreement between simulation and measurement. The slight discrepancy in the gain can be explained by the failure to account for wiring resistances in the simulation.

Following room temperature measurements, cryogenic gain and noise measurements were carried out using the cold attenuator method described in [8] and the results are plotted in Fig. 4(c). The amplifier achieves a T_e of better than 5.4 K out to 5 GHz with an average value of T_e and gain of 4.3 K and 30.8 dB over the operating band. Following noise and gain measurements, the amplifier was cooled without an attenuator on the input and its S_{11} and linearity were measured and the results appear in Fig. 4(d) and Table I. At 15 K, S_{11}, S_{21}, and T_e were all found to be in excellent agreement with the modeled result. The ripple in the return loss measurement is believed to be due to changes in the stainless steel cable connecting the amplifier to input of the dewar occurring with cooling as calibration of the VNA was done at 300 K.

V. CONCLUSION

In this letter, the design procedure for a matched cryogenic LNA has been presented including a discussion of the impact of a feedback resistor on the noise. The fabricated circuit results agree well with modeling, both at 15 and 300 K physical temperatures. To the authors' knowledge, the amplifier has the lowest reported value of T_e for a silicon integrated circuit and is the only input-matched integrated-circuit cryogenic LNA spanning this frequency range that has been reported to date.

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