A 0.114-mW Dual-Conduction Class-C CMOS VCO with 0.2-V Power Supply

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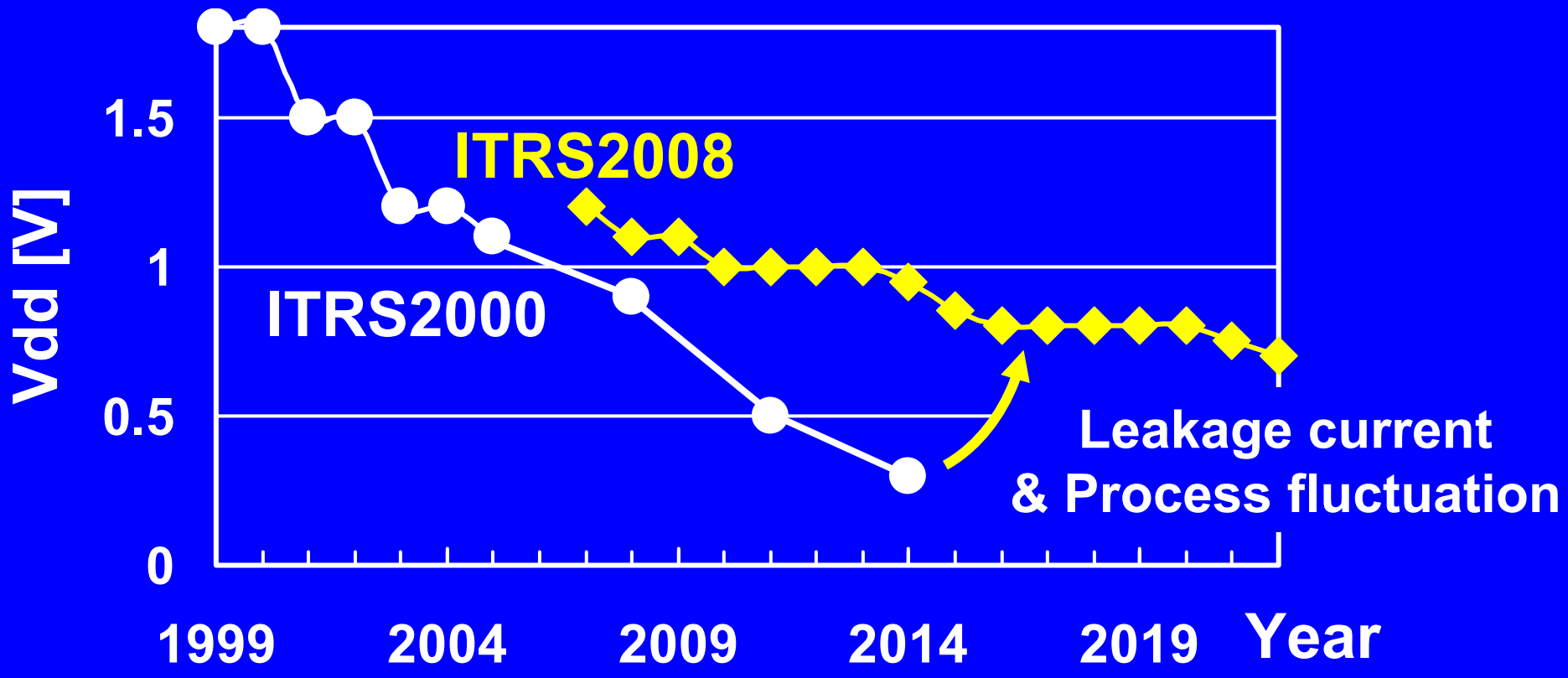
Outline of Presentation

- Motivation
  - Supply voltage scaling
  - Jitter degradation
- Low-voltage VCO's issues
- The proposed Dual-Conduction topology
  - Low-power and Low-phase noise with a very low supply voltage
- Measurement results
- Conclusions

Supply Voltage Roadmap



The voltage scaling is required again.
Low-voltage circuit design is challenging.

Phase Noise Comparison

LC-VCO [A.Mazzanti, et al., JSSC 2008]

$$\frac{\omega_0^2}{\omega_{\text{offset}}^2} \cdot \frac{kT}{V_{\text{DD}} I_{\text{bias}}} \cdot \frac{1+\gamma_n}{Q^2}$$

+30dB worse

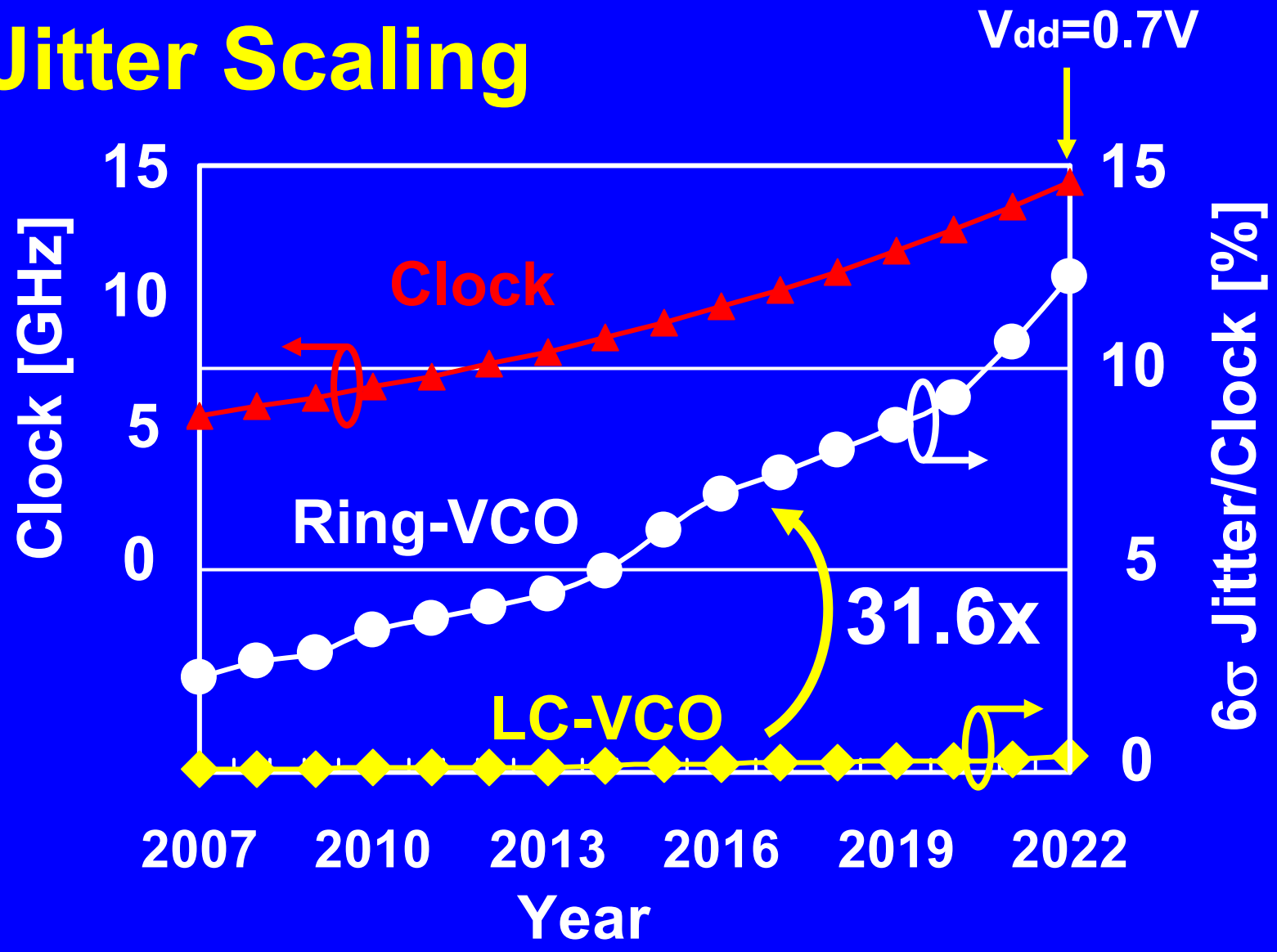
Ring-VCO [A.Abidi, JSSC 2006]

$$\frac{\omega_0^2}{\omega_{\text{offset}}^2} \cdot \frac{kT}{V_{\text{DD}} I_{\text{bias}}} \cdot 2M \left\{ \frac{V_{\text{DD}}}{V_{\text{DD}} - V_{\text{TH}}} (\gamma_n + \gamma_p) + 1 \right\}$$

M: #stages

$$V_{\text{TH}} = \frac{V_{\text{DD}}}{4},\ \gamma_n = \gamma_p = \frac{2}{3},\ M = 3,\ Q = 10$$

Jitter Scaling



With the same power consumption, LC-VCO has much smaller jitter performance.

Clock Generation with Low Vdd

- Lowering of supply voltage is required to realize high-speed and low-active-power circuits.
- Jitter will become larger according to the voltage scaling.
- Ring-VCO become infeasible due to too large jitter or too large power consumption.
- To reduce the power consumption of the clock generator, use of LC-VCOs is an unavoidable way in such the low-voltage condition.

Low-Voltage LC-VCO

- Transformer-Feedback VCO can operate with a low supply voltage.
- 0.5V and 0.35V VCOs are reported.

[1] K. Kwok, and H. C. Luong, JSSC 2005

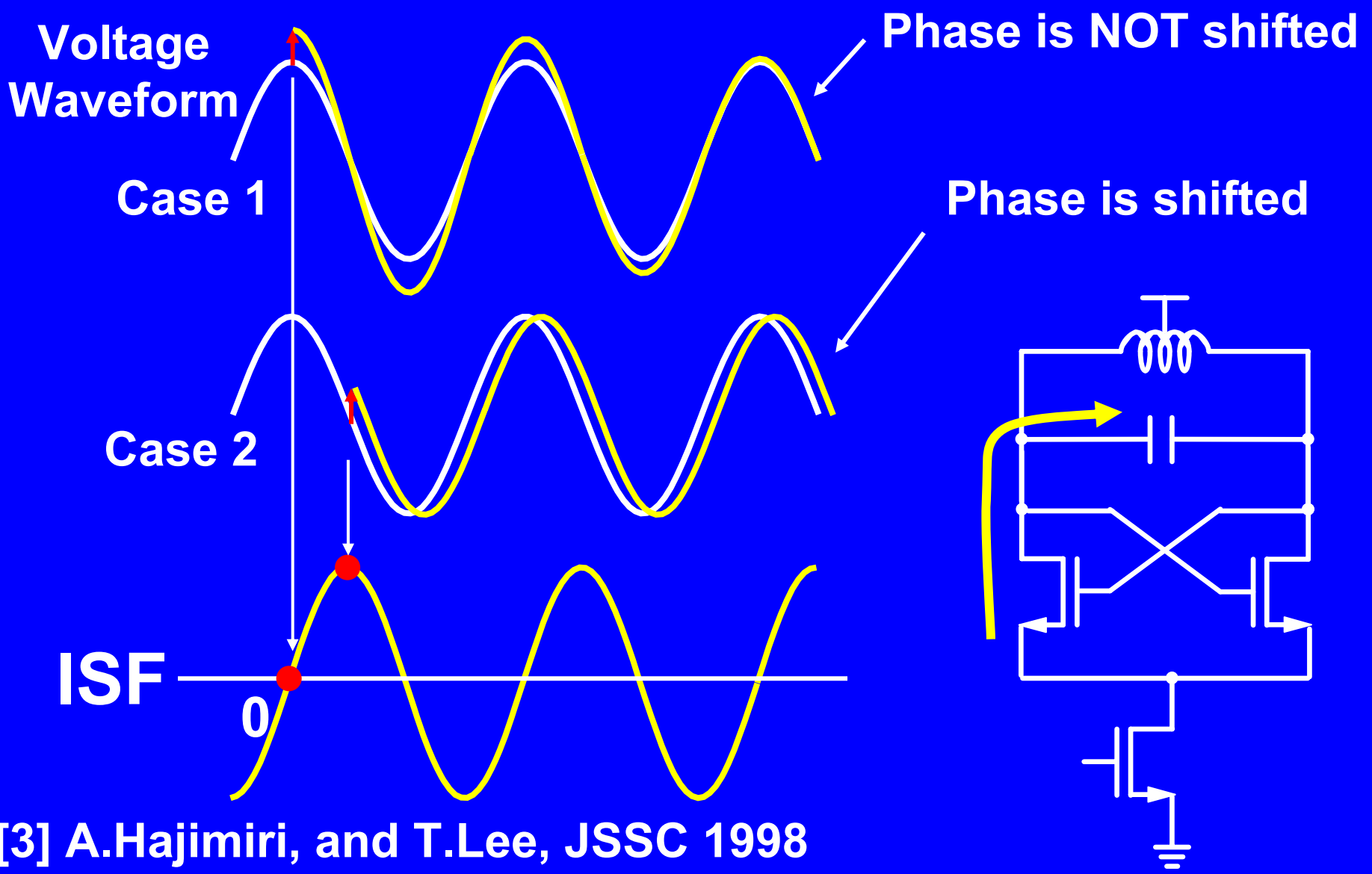
- Class-C VCO archives 196dBc/Hz of FoM.
- Startup is an issue of Class-C VCO under the low-voltage condition.

[2] A. Mazzanti, and P. Andreani, JSSC 2008

Summary of This Work

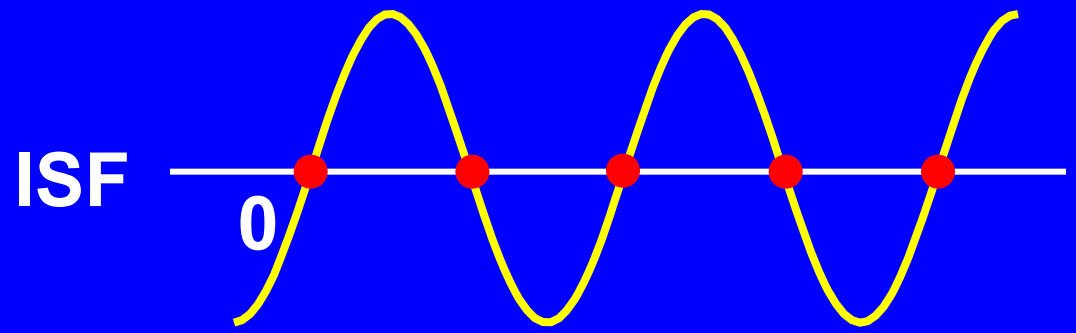
- Sub-0.5V LSI
- A Dual-Conduction topology is proposed for Class-C VCO in this work.
- It is modified to work with a very low supply voltage.
- 0.2V VCO is realized by using a 0.18μm CMOS process with 114μW of power consumption.

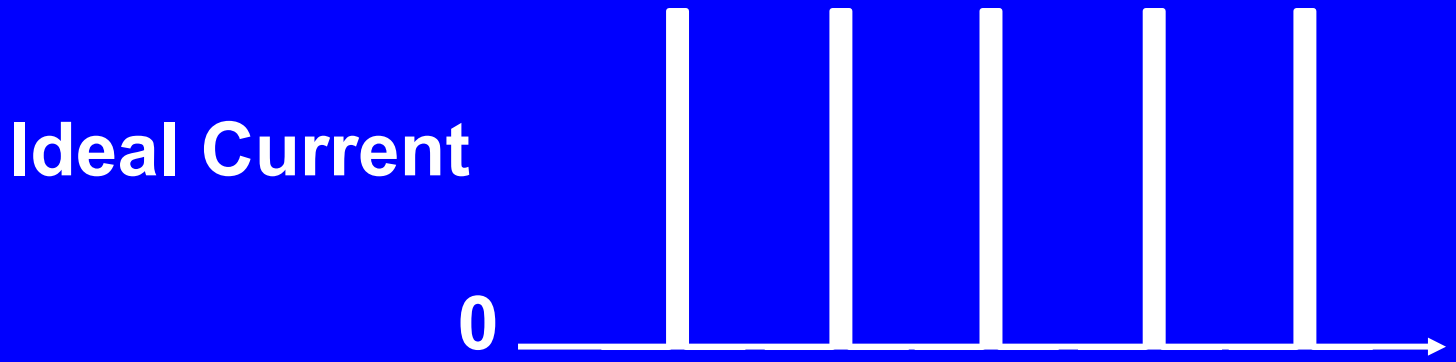
Impulse Sensitivity Function (ISF)

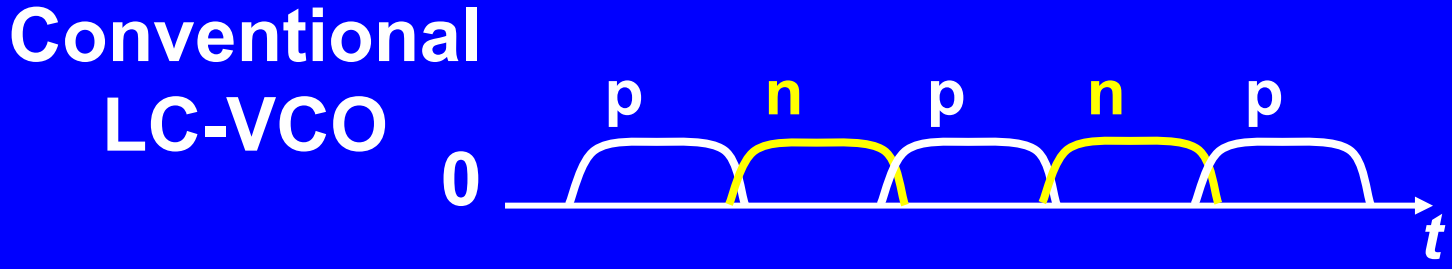


[3] A.Hajimiri, and T.Lee, JSSC 1998

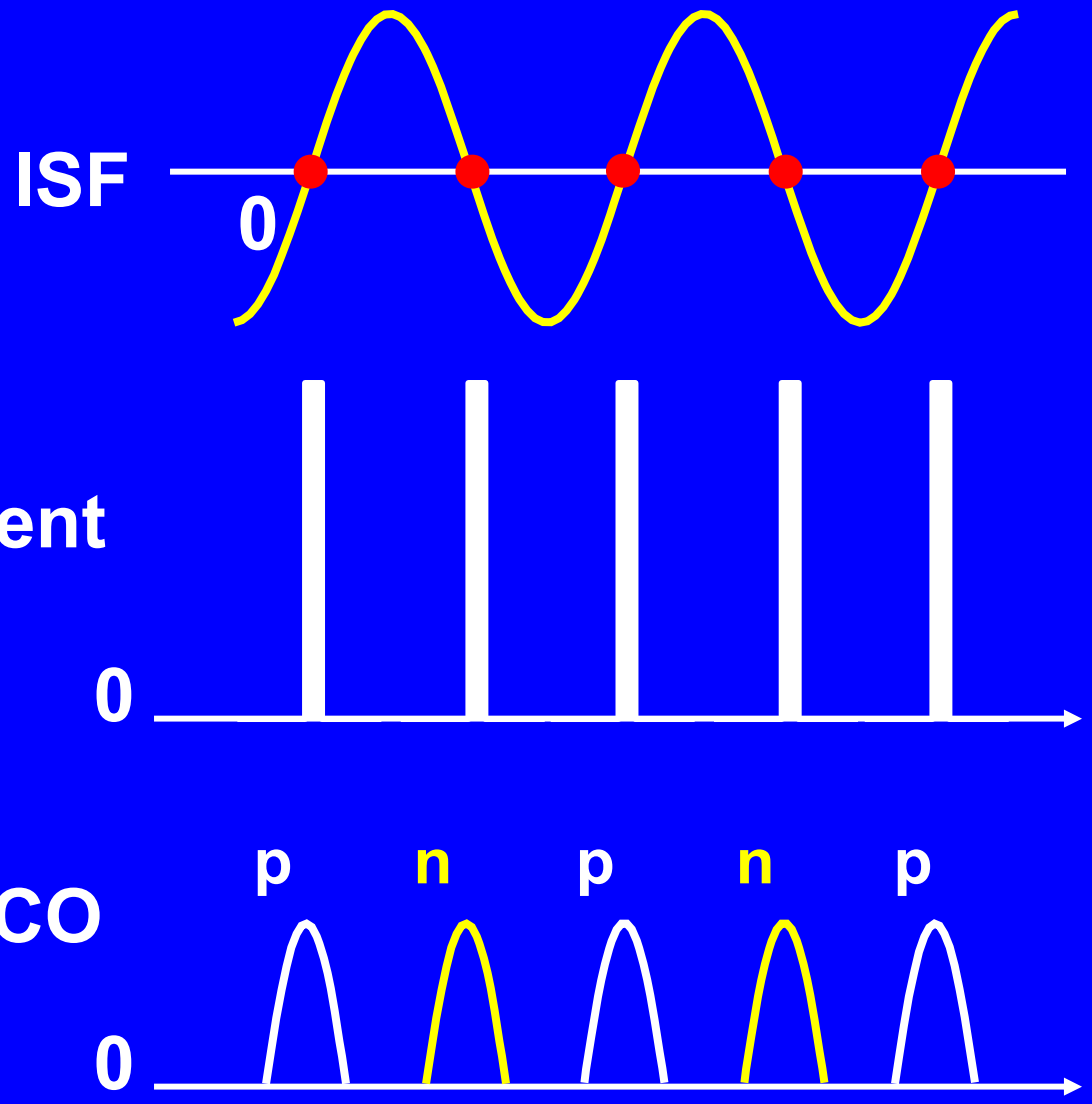
Ideal Current Conduction



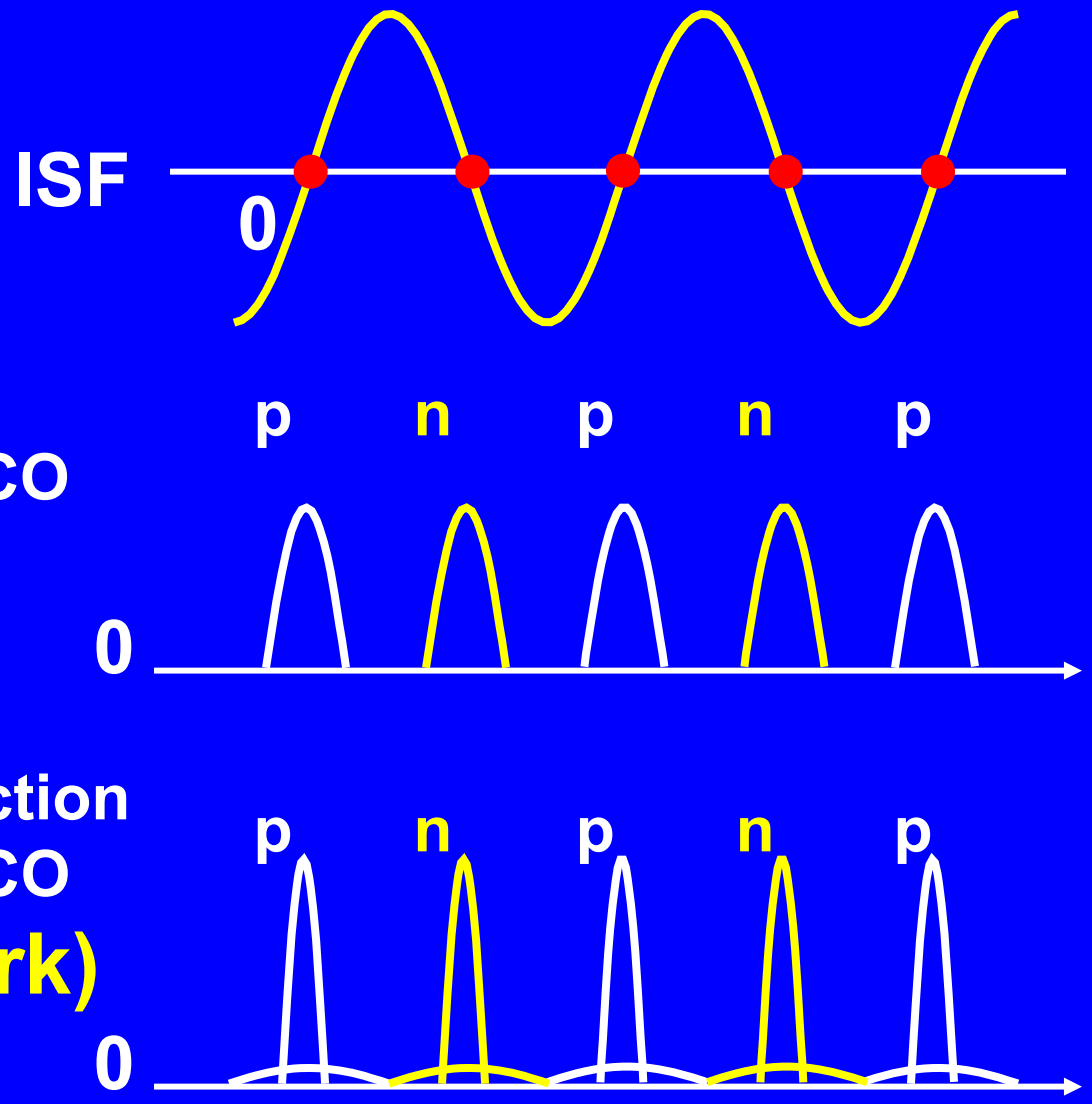




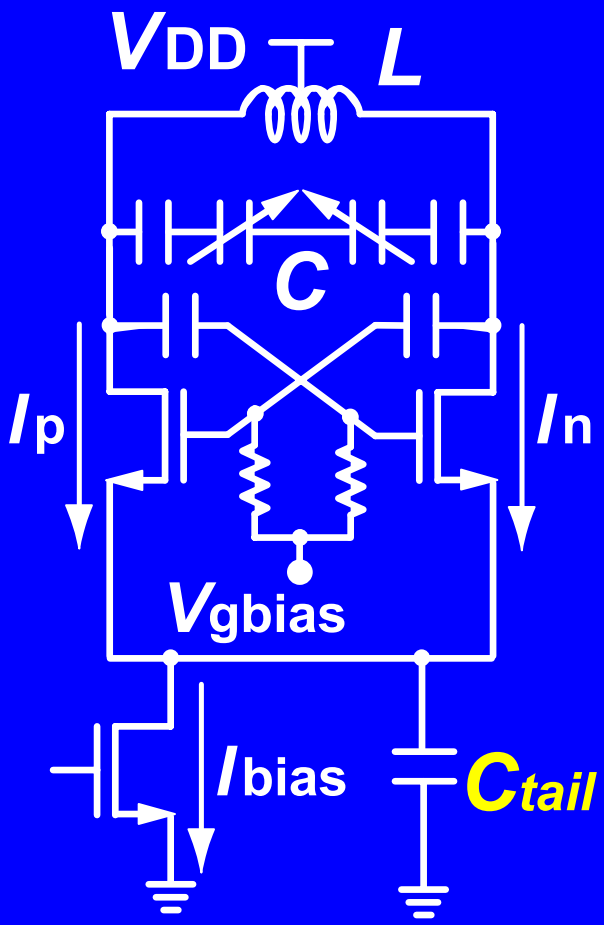
Current Conduction of Class-C VCOs

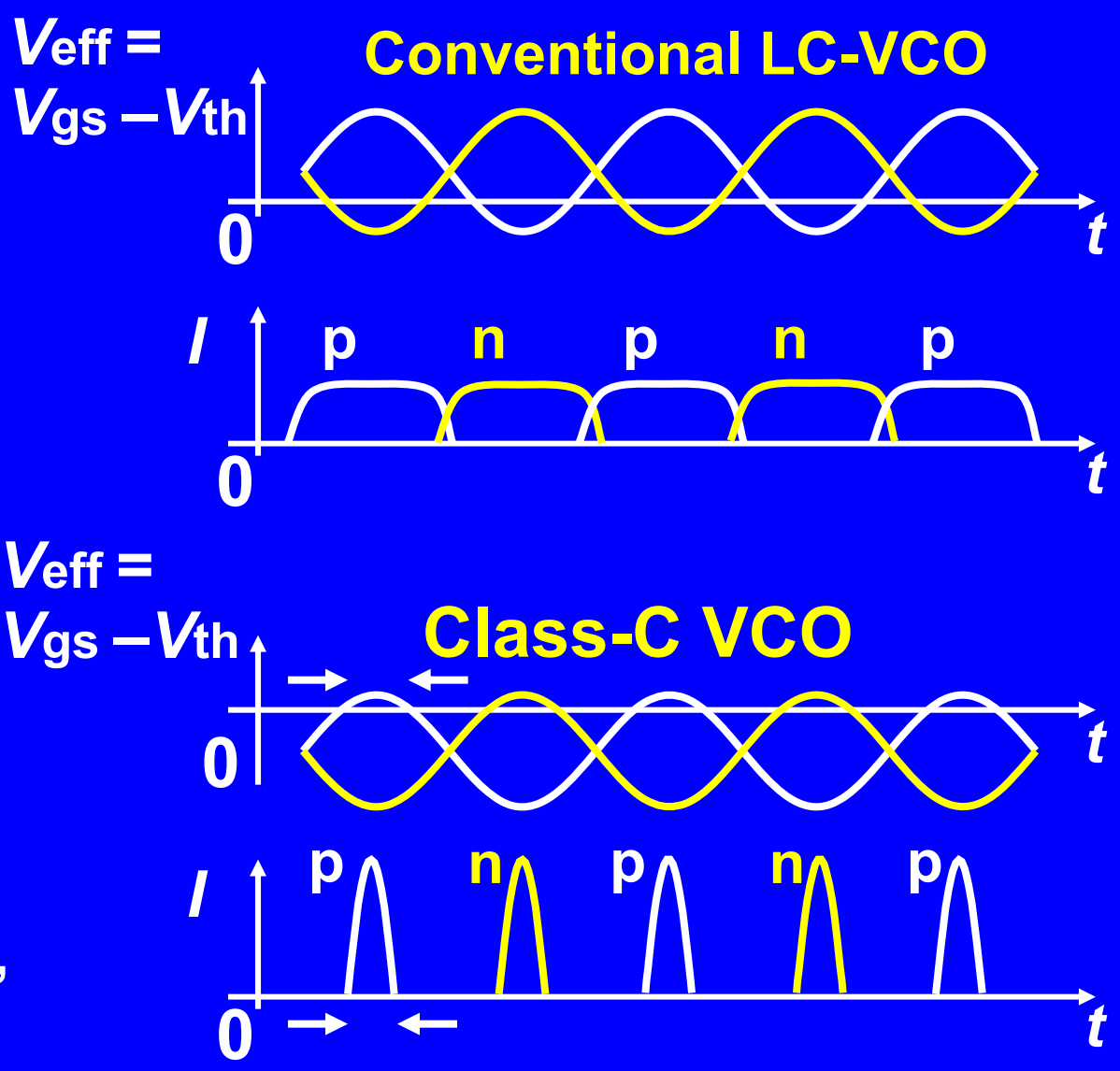


Current Conduction of Class-C VCOs



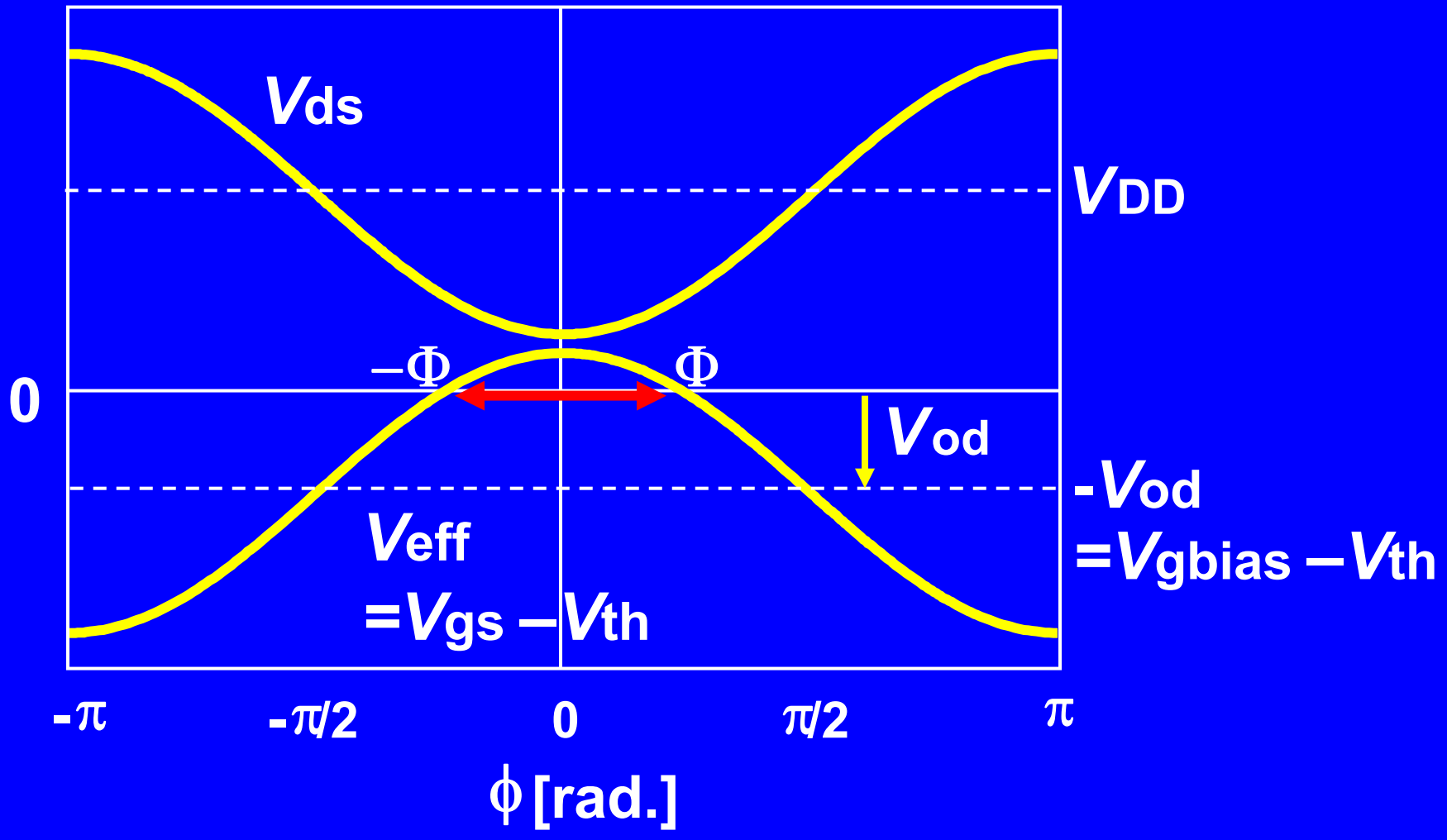
Class-C VCO[2]





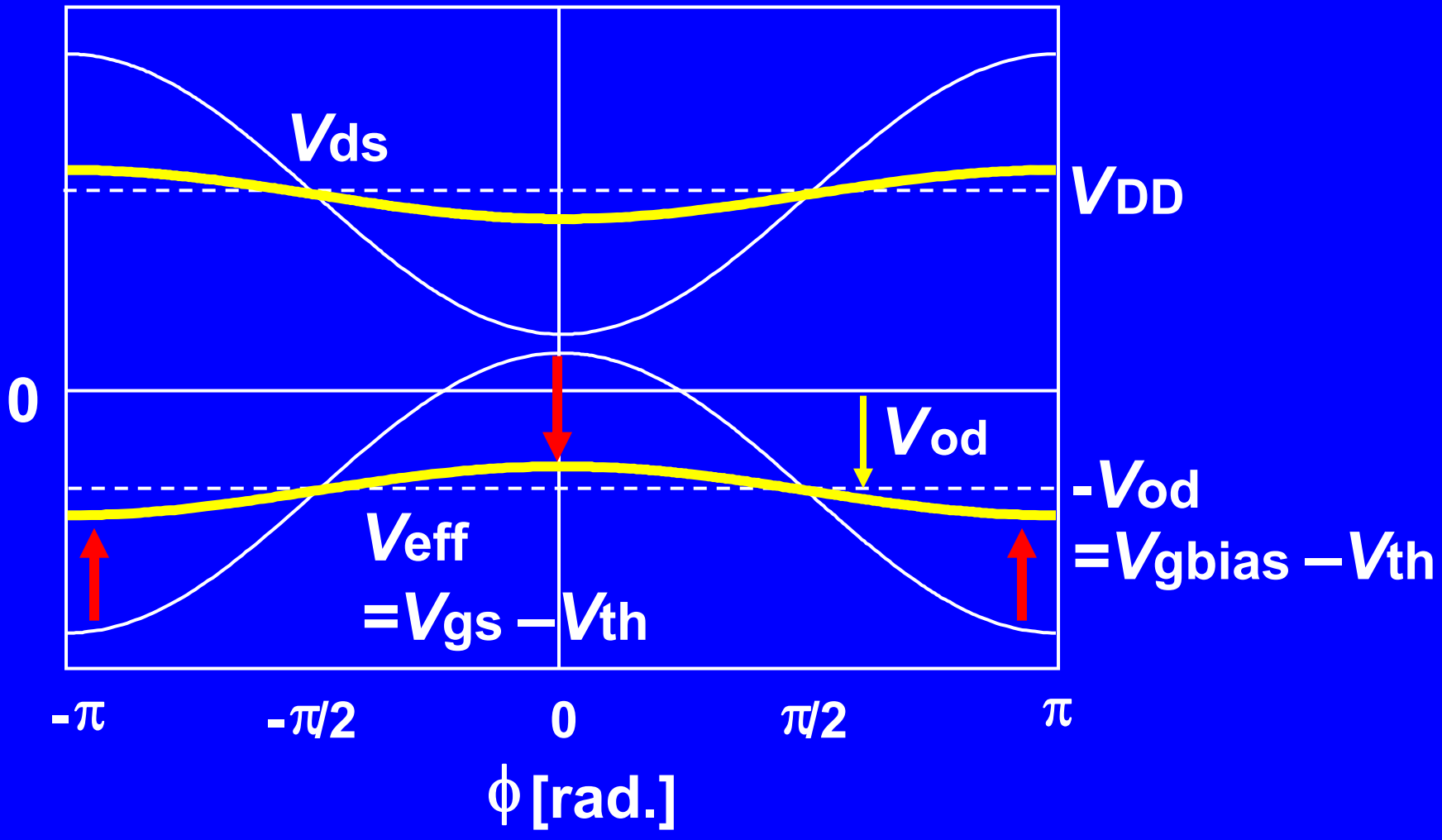
[2] A. Mazzanti, *et al.*, JSSC 2008

Condition for Class-C Operation



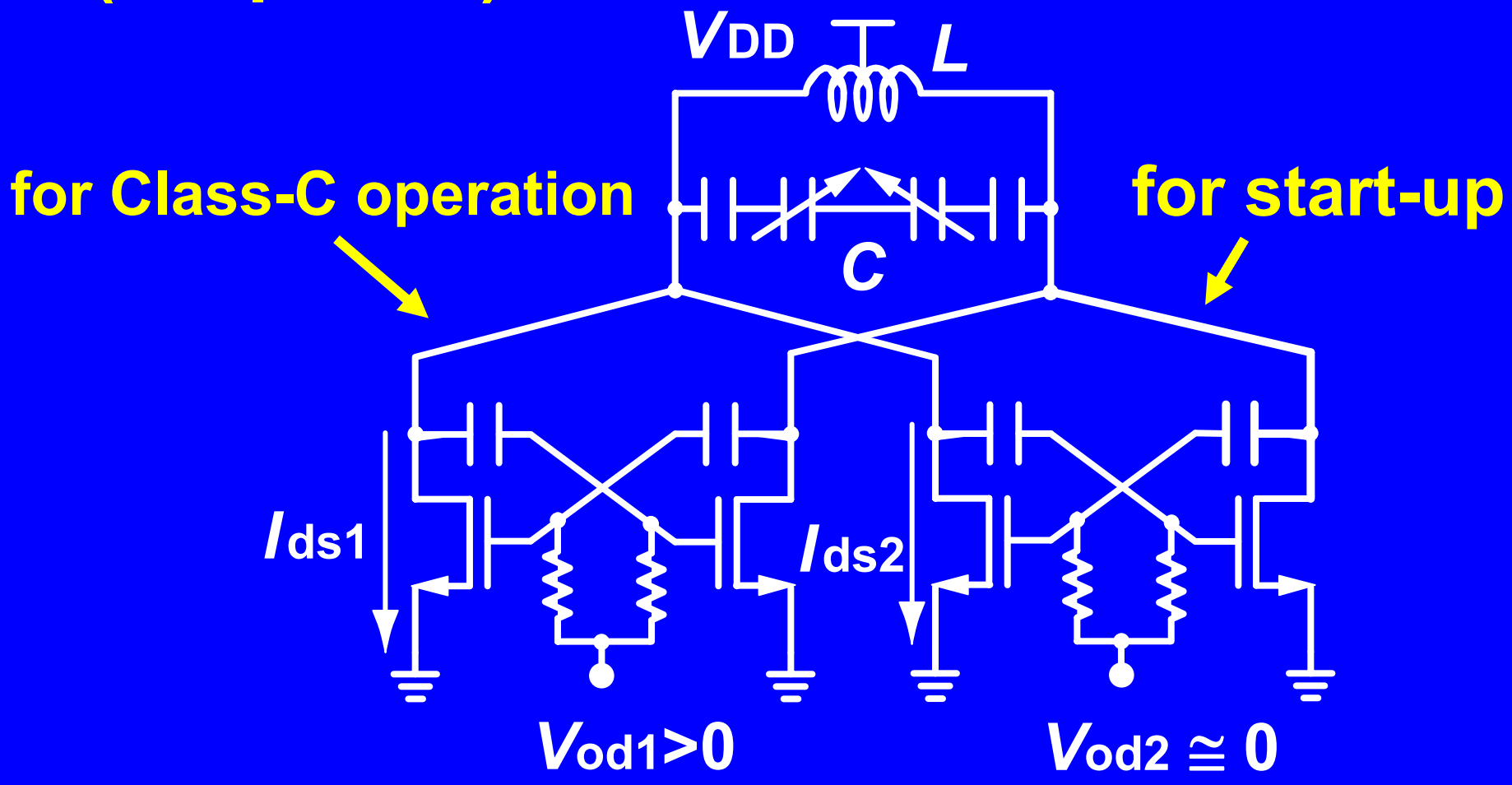
Active region: $V_{ds} > V_{eff}$

Issue of Class-C VCO for Low Vdd

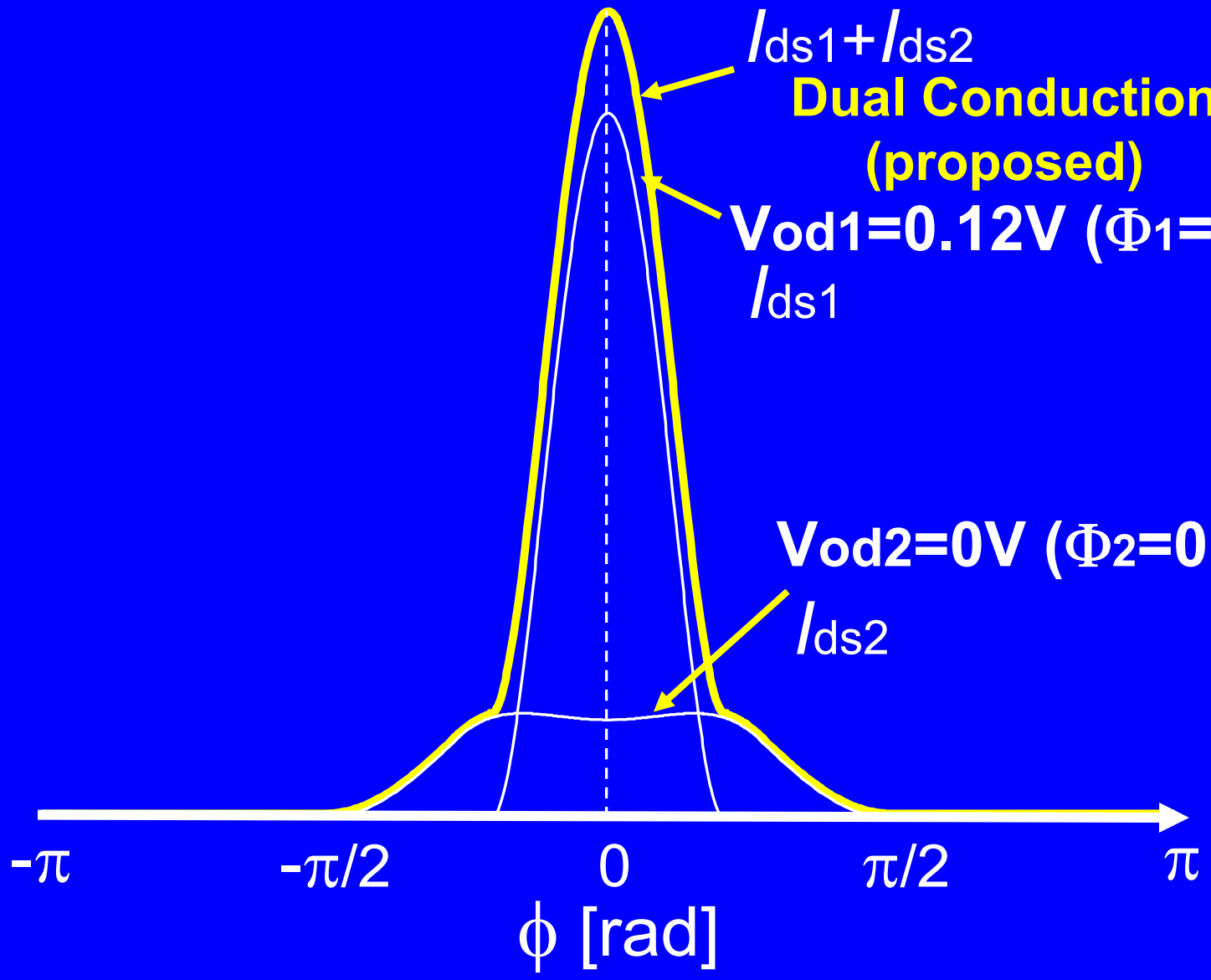


Vod has to be small due to the start-up problem, so conduction angle cannot be reduced.

Dual-Conduction Class-C VCO (Proposed)

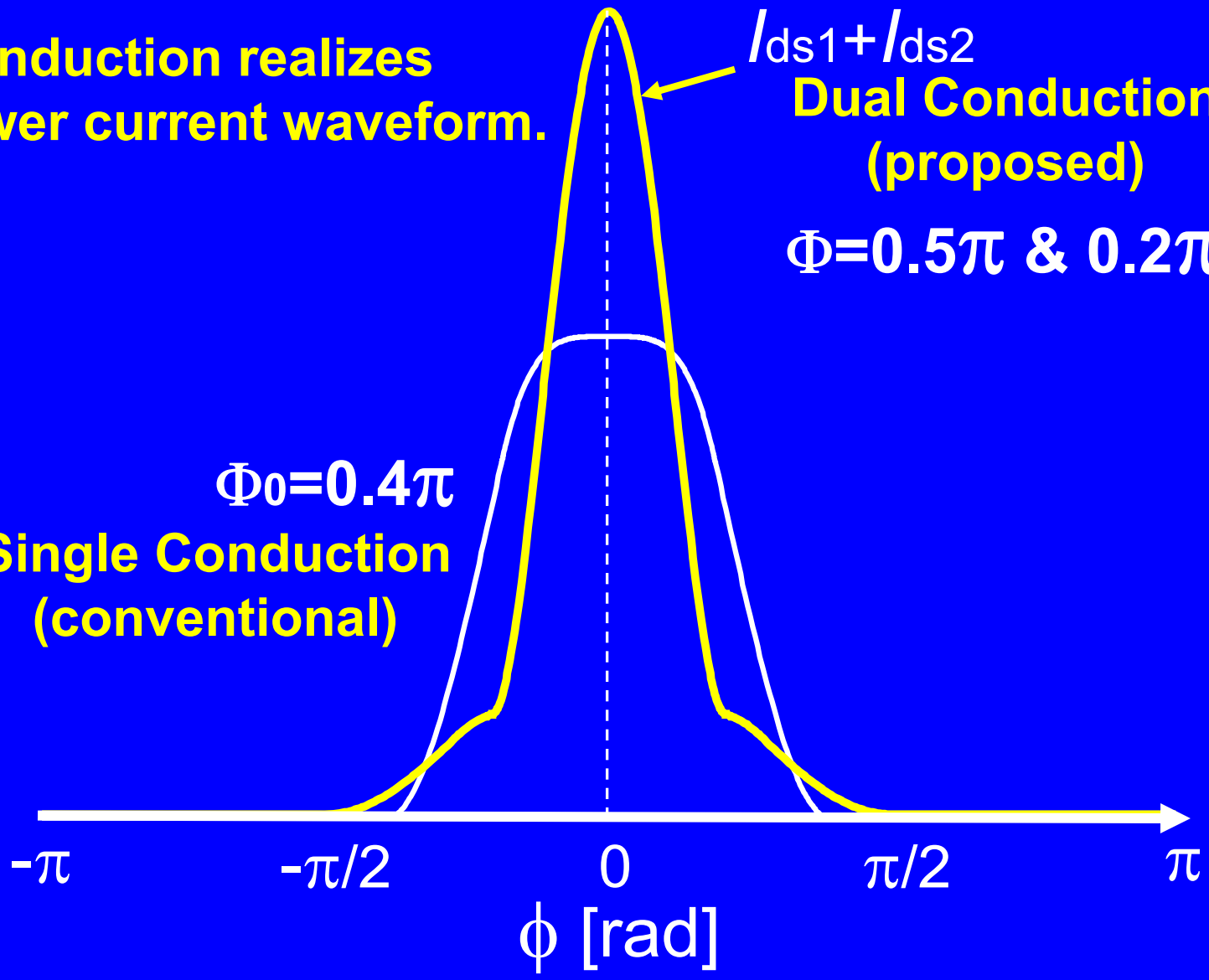


Dual-Conduction Current Waveform



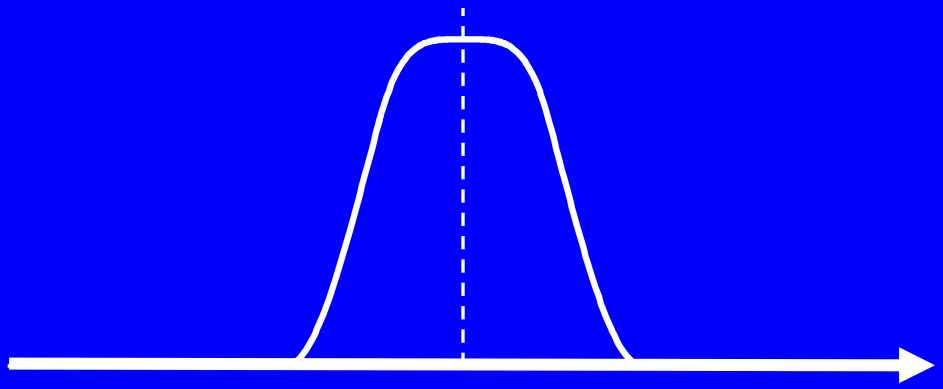
Comparison of Current Waveforms

Dual Conduction realizes a narrower current waveform.



Analytical Comparison

Single Conduction (conventional)



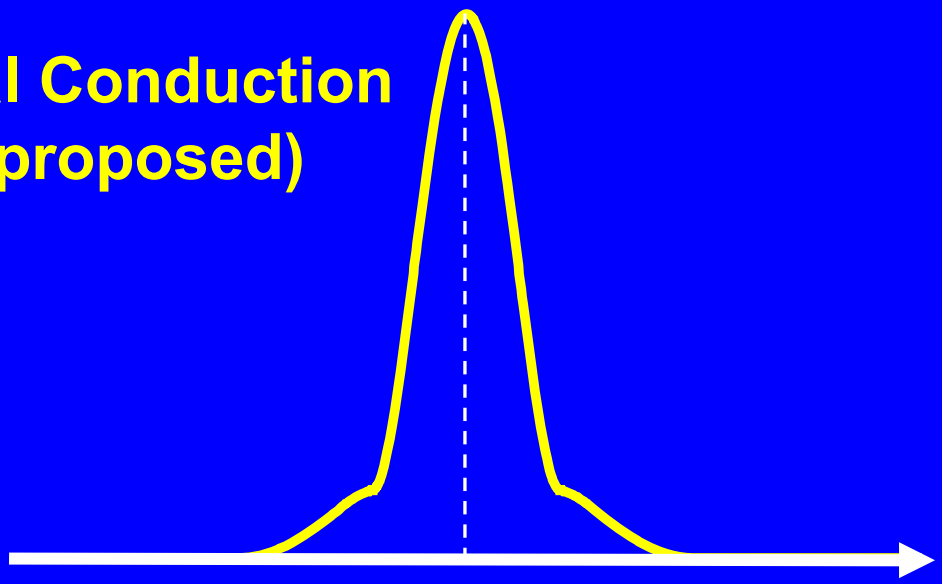
V_{od}=0.05V (Φ_0=0.4π)

PN: -106dBc/Hz-1MHz

P_{dc}: 168μW

FoM: 188dBc/Hz

Dual Conduction (proposed)



V_{od1}=0.12V (Φ_1=0.2π)

V_{od2}=0V (Φ_2=0.5π)

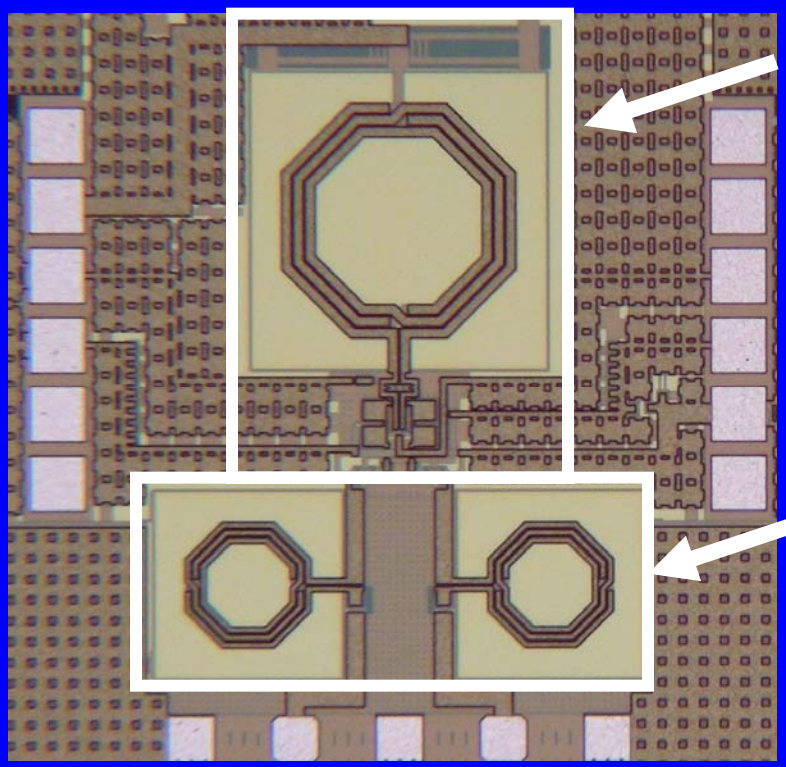
PN: -109dBc/Hz-1MHz

P_{dc}: 162μW

FoM: 191dBc/Hz

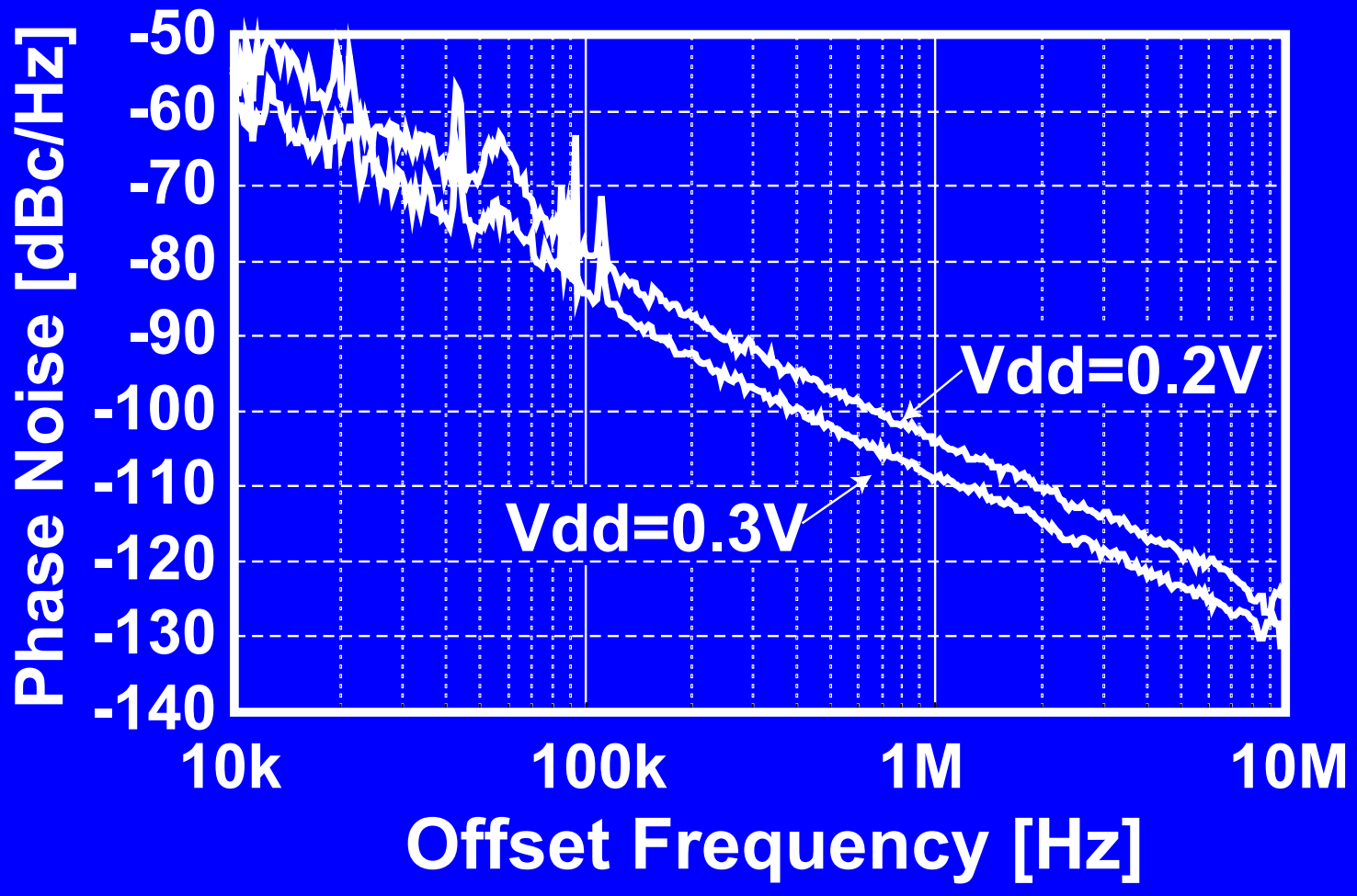
(*) V_{dd}=0.2V, A=0.15V, V_{th}=0.5V, f_0=5GHz, Q=10

Chip Micrograph



- 0.18μm CMOS process
- 670μm x 440μm for core area

Phase Noise Measurement



V_{gbias1}=0.45, V_{gbias2}=0.55

f_0=4.5GHz

-104dBc/Hz@1MHz for 0.2V

-109dBc/Hz@1MHz for 0.3V

Performance Comparison

	[2]	[1]		This work	
Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	
Vdd [V]	1.0	0.5	0.35	0.3	0.2
P_{DC} [mW]	1.3	0.57	1.46	0.159	0.114
f_0 [GHz]	4.9	3.8	1.4	4.5	4.5
Phase noise [dBc/Hz]	-130 @3MHz	-119 @1MHz	-129 @1MHz	-109 @1MHz	-104 @1MHz
FoM [dBc/Hz]	196	193	190	190	187
Topology	Class-C (single)	Transformer feedback		Class-C (dual)	

[1] K. Kwok, *et al*., JSSC 2005 [2] A. Mazzanti, *et al*., JSSC 2008

Conclusion

- A 0.2V LC-VCO is realized by using a dual-conduction Class-C topology, which has a smaller conduction angle than the conventional Class-C VCO under the low supply voltage condition.
- The significance of this work is improvement of FoM for the low-voltage oscillators.
- A low-jitter and low-power clock generator can be realized.
- Bias generation is a remaining issue.