IEEE Asian Solid-State Circuits Conference
November 12-14, 2007 / Jeju, Korea

# A 0.13µm Hardware-Efficient Probabilistic-Based Noise-Tolerant Circuit Design and Implementation with 24.5dB Noise-Immunity Improvement

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**Abstract**

As the size of CMOS devices is scaled down to the nanoscale level, noise interferences start to significantly affect the VLSI circuit performance. Because the noise is random and dynamic in nature, a probabilistic-based approach is more suitable to handle signal errors than the conventional deterministic circuit designs. However, probabilistic-based designs cost larger hardware area. In this paper, we design and implement a hardware-efficient probabilistic-based noise-tolerant circuit, an 8-bit Markov Random Field carry lookahead adder (MRF_CLA), in 0.13µm CMOS process technology. The measurement results show that the proposed MRF_CLA can provide 24.5dB of noise-immunity enhancement as compared with its conventional CMOS design. Moreover, the transistor count can be saved 42% as compared to the state-of-art MRF design [1].

## I. Introduction

With the progress of VLSI process technology, the design complexity and the transistor density in SoC systems increase rapidly, which leads to the power consumption and power density in SoC designs also increase rapidly. Future electronic devices are expected to operate at much lower power supply to save power, especially portable electronics and biomedical implanting devices. However, one of the major challenges in ultra-low power and nano-circuit design is noise fluctuation. As we move into the nanoscale CMOS designs, signal errors, which directly account for thermal noise, become significantly and start to affect the VLSI circuit performance. Because the faults are random and dynamic in nature, a probabilistic approach is more suitable to handle these random injected noises.

In [1], a *probabilistic noise-tolerant* circuit design was proposed and implemented based on the theory of Markov Random Field (MRF) [2]. The MRF provides a formal probabilistic framework so that computation can be directly embedded in a network with immunity to both device and signal failures. By computing the logic states in a probabilistic way, the MRF-based noise-tolerant circuits can bring the circuit to operate with better noise-immunity. However, the area overhead of MRF circuits in [1] is about 10 times larger than the conventional CMOS circuits. Therefore, in this paper, we propose a *hardware-efficient probabilistic-based noise-tolerant circuit* through MRF network simplification. The proposed design can provide nearly the same noise-tolerant performance but with lower hardware overhead. We implement an 8-bit MRF_CLA in 0.13µm CMOS process technology. The measurement results show that the proposed MRF_CLA can provide 24.5dB of noise-immunity enhancement as compared with the conventional CMOS CLA. Moreover, the transistor count can be saved 42% as compared to the state-of-art MRF design [1].

## II. Hardware-Efficient MRF Noise-Tolerant Circuit Design

The MRF provides a formal probabilistic framework, which has been commonly used in pattern recognition and communications. The main reason for selecting the Markov random network as the basis for our design is that its operation does not depend on perfect devices or perfect input signals. The basic idea of MRF design is as follows: under the probabilistic framework, we cannot expect logic values in a circuit at a particular time to be correct. We can only expect the probability distribution of the values to have the highest likelihood in a correct logic state. The appropriate mathematical framework for this type of analysis is the MRF, which was developed [2] to support the optimization of the values of a large set of random variables so that their overall joint probability has a global maximum.

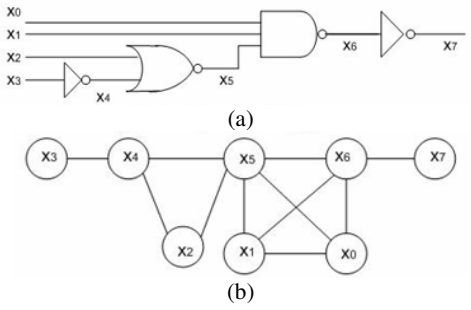



Fig. 1: A logic circuit & its MRF graph (a) A sample circuit; (b) its MRF graph [3].

In [1], the first working silicon chip was fabricated to prove the design concept of the noise-tolerant MRF circuits. Its solution is to map the circuit onto MRF graph, and then implement the MRF network by minterm generators. We take the M3 module of the ISCAS-85 C432 interrupt controller [4] shown in Fig. 1(a) as an example circuit. The M3 circuit can be mapped onto an MRF graph as shown in Fig. 1(b). To implement the MRF

noise-tolerant circuit follow [1], the hardware complexity will be exponential in the number of MRF network nodes. As illustrated in Fig. 2, the valid function of the M3 circuit is determined by nodes X1 to X7; therefore, the hardware complexity will be proportional to $2^7$.

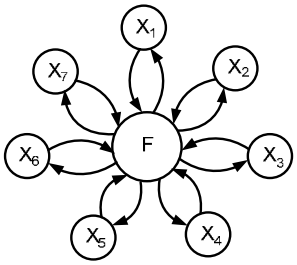
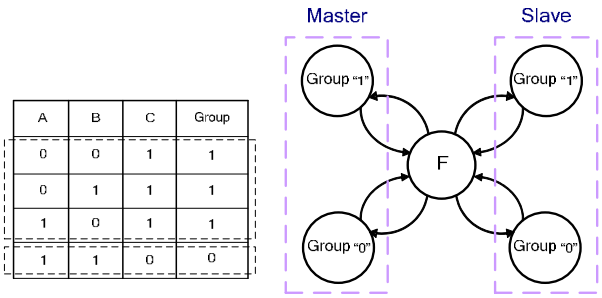



Fig. 2: The output function of M3 circuit is determined by its MRF nodes.




| A | B | C | Group |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

(a) (b)

Fig. 3: The proposed hardware-efficient MRF mapping method. (a) The truth table is separated into two groups; (b) the output function is determined by master and slave MRF networks.

To reduce the hardware complexity, we propose and implement a hardware efficient MRF circuit in this paper. Instead of directly implementing all valid states in MRF network, we separate the truth table into two groups according its output logic states and implement it by master and slave MRF networks. As illustrated in Fig. 3(a), all output states in logic "1" are collected in group "1", while logic "0" are collected in group "0". First, we implement minterms in the group "1" and group "0", respectively. These two groups will compete for determining the output function states. Therefore, we call this part as master MRF network. To achieve a reliable decision, we connect the output signals feedback to strengthen the reliability of master MRF network. This part is called as slave MRF network.

Finally, the joint distribution of random logic levels in the circuit can be made to converge to the correct logic operation with the higher probability. As illustrated in Fig. 3(b), the output function of the MRF circuit is determined by master and slave MRF networks; therefore, the hardware complexity will be proportional to 2*2. By this way, the design overhead will not increase exponentially and the noise-tolerance performance can be preserved.

Fig. 4 shows the proposed hardware-efficient MRF NAND implementation. The master MRF NAND network is constructed by a AND gate and an OR gate. The slave MRF NAND network is connected as a RS latch. In a logic circuit, the correct state is determined by

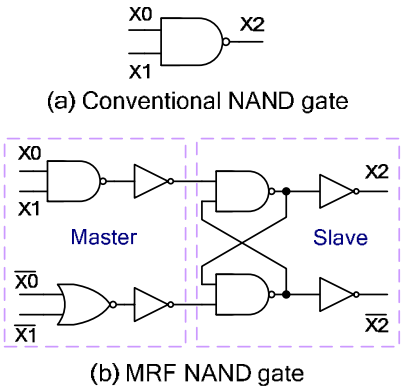



Fig. 4: The schematic of a NAND logic (a) A CMOS NAND gate & (b) its MRF NAND logic.

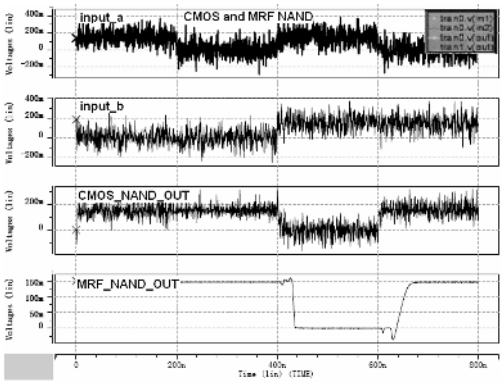



Fig 5: Simulation results of the inputs/ouputs of CMOS and MRF NAND.

the group with higher probability. The propagation of logic states through the network is such that the distribution of each network node has a local maximum probability in order to have the correct logic values. The noise-tolerant capability is achieved because the MRF network is updated by iteratively changing the state of nodes and propagating these changes through the network. Ultimately the network converges to a stable set of state probabilities corresponding to the correct logic states. Successful operation only requires that the energy of correct states is lower than the energy of errors.

The corresponding SPICE simulation of a NAND gate by using the 70nm CMOS library from Berkeley [5] is shown in Fig. 5. The top two curves are the input signals, which are generated by adding the Gaussian noise with zero mean to logic '1' and to logic '0'. The noise on the inputs causes the standard CMOS NAND gate to switch between correct and incorrect output values as shown in the second curve above the bottom in Fig 5. The MRF outputs remain robust as shown in the bottom curve. We can see that the MRF design has much better noise-tolerance capability.

### III. Chip Implementation and Measurement

To demonstrate the noise-tolerance capability of the MRF circuits, we utilize an 8-bit MRF_CLA as a proof-of-concept design for performance comparison. The architecture of the proposed 8-bit MRF CLA is illustrated

in Fig. 6. To construct a MRF CLA, we divide the whole CLA into many basic cells and map the MRF circuit on these basic cells. By this way, the design overhead will not increase rapidly and the noise-tolerance performance can be maintained.

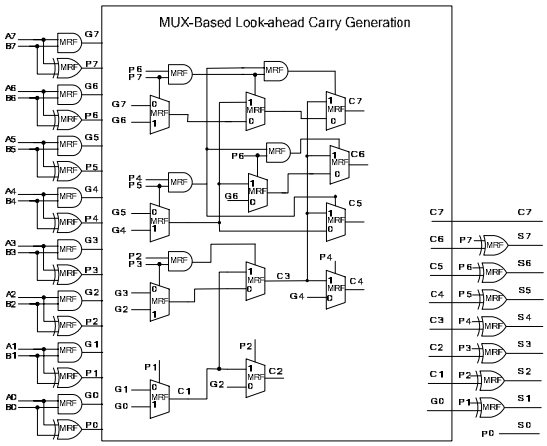



Fig 6: Architecture of the proposed 8-bit MRF CLA.

The 8-bit hardware-efficient probabilistic-based MRF_CLA is implemented in TSMC 0.13μm CMOS process. The MRF_CLA chip die photo is shown in Fig. 7. The performance summary is collected in Table 1. As a comparison, the transistors count in the proposed MRF design needs 2940 transistors, which can save 42% transistor count, while the transistor count is 5040 in [1]. As compared to the conventional CMOS design, the noise tolerance ability of MRF design can be improved about $10^2$~$10^4$ times under various AWGN noise interference. With superior noise-tolerant ability, the operation voltage in the MRF design can be significantly reduced to operate under the sub-threshold region for power savings. The conventional CMOS design simply cannot operate under such low power environment. In extremely noisy nanoscale computing system, the improvement of noise-tolerance ability and energy consumption outweigh what we compromise in the design complexity. Moreover, by using nanofabrication technology, we expect nanoelectronics to compensate the drawbacks of MRF. Noise interference is certainly going to get much worse in nanoelectronic circuits, and conventional CMOS circuit technique simply cannot deal with the problems.

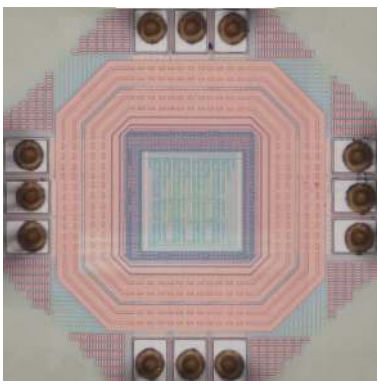
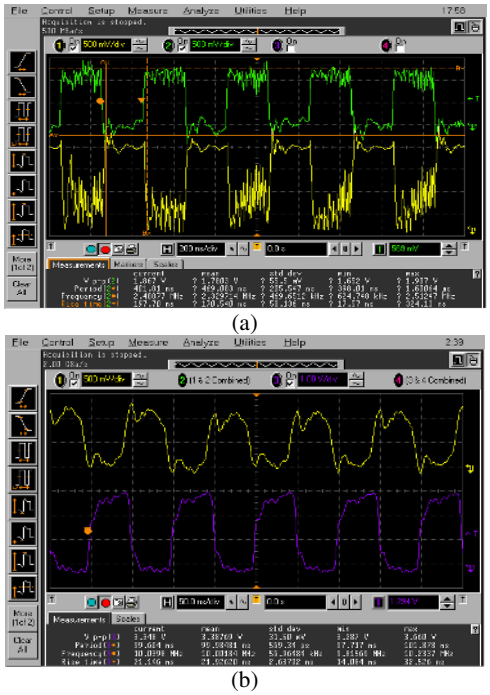


Fig. 7: The hardware-efficient MRF_CLA chip die photo.

Table 1: MRF chip performance summary

| | |
|---|---|
| Process | TSMC 0.13um |
| Area | 0.14mm*0.14mm |
| Transistor | 2940 |
| Energy | 1.9 uw/MHz @ 0.25V<br>3.1 uw/MHz @ 0.3V<br>7.7 uw/MHz @ 0.45V<br>13.7 uw/MHz @ 0.6V<br>31.9 uw/MHz @ 0.9V<br>58.0 uw/MHz @ 1.2V |
| BER | 7.00E-05@10.6dB SNR<br>1.21E-05@11.5dB SNR<br>1.07E-06@12.6dB SNR<br>1.25E-08@13.7dB SNR |
| Noise Immunity Improved 24.5dB | |

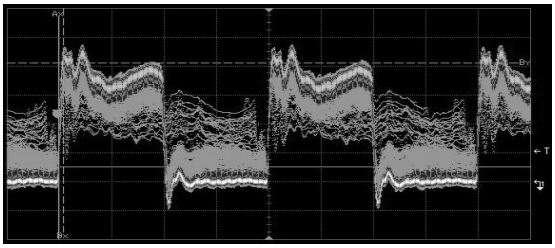
In measurement, as illustrated in Fig. 8, we can observe each single bit in the CLA output to compare waveforms under noise interference. We can further employ the eye-diagram to observe the output waveform of circuits under the interference of random noise by continually reduplicating "0" and "1" signals under random noise interference. Comparing the eye-diagram of Fig. 9 under AWGN noise interference with 14.1dB SNR, we can demonstrate the noise-tolerance performance of the proposed MRF noise-tolerant circuit is much better than the CMOS_CLA circuit. Under ultra-low voltage operation, we can use the histogram to compare the noise-tolerance under sub-threshold region, as illustrated in Fig. 10. The noise-tolerance of the proposed MRF design is much better than the CMOS_CLA circuit under ultra-low voltage operation.



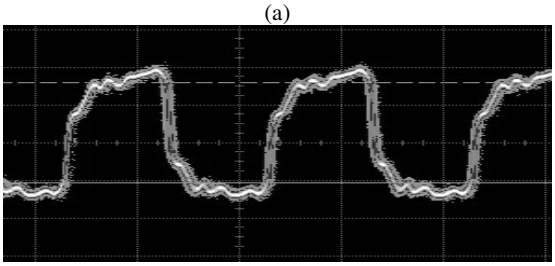
(a)

(b)

Fig. 8: Measured single-bit waveform of the CMOS_CLA (a) and the MRF_CLA circuit (b) under AWGN noise with 14.1dB SNR.

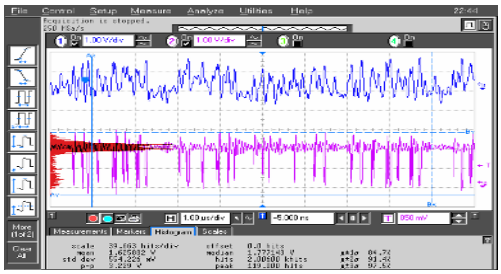


(a)

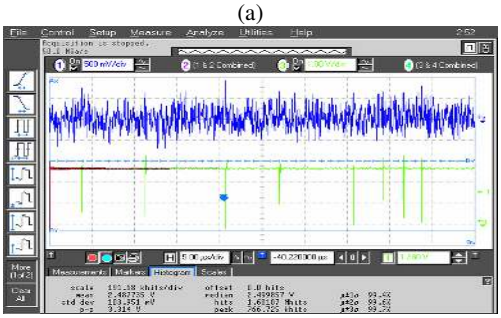


(b)

Fig. 9: Eye-diagram of the CMOS_CLA (a) and the MRF_CLA circuit (b) under AWGN noise interference with 14.1dB SNR.



(a)



(b)

Fig. 10: Histogram of the CMOS_CLA (a) and the MRF_CLA circuit (b) under sub-threshold region with noise interference.

By adjusting the noise power and supply power, we can measure the Bit-Error-Rate (BER) of the proposed hardware-efficient MRF_CLA, the MRF_CLA in [1] and CMOS_CLA circuits under various Signal-to-Noise Ratio (SNR) levels as illustrated in Fig. 11. Based on our real-time measurement results, the noise-immunity of the proposed MRF_CLA can be enhanced by 24.5dB, which means with about $2.8*10^2$ times improvement in BER, as compared to the conventional CMOS_CLA. High noise-immunity feature of the MRF circuit is very useful to low-power silicon circuits when they operate under very low Vdd condition. In 0.13µm process, under 10.6dB low SNR condition, the proposed MRF_CLA circuit can achieve $7*10^{-5}$ BER. Under 0.25V supply voltage, the proposed MRF_CLA circuit consumes only 1.9µw/MHz. This MRF_CLA chip has demonstrated the superiority in

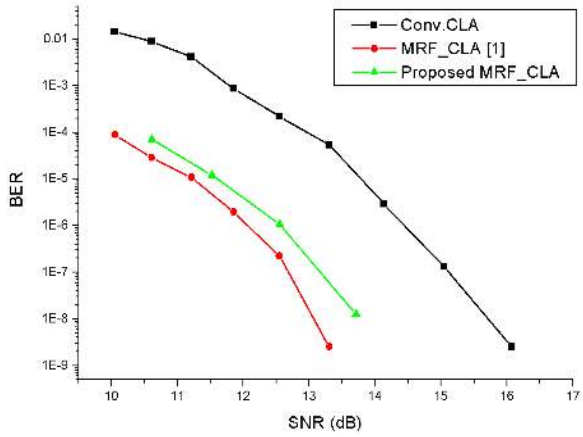



Fig. 11: Noise-Immunity Comparison of MRF_CLA and CMOS_CLA circuit under various SNR.

noise-tolerant capability. The hardware overhead can also be greatly reduced by 42%. Hence, it is a good candidate for future nanoscale circuit designs where the operating environment is very noise intensive.

## IV. Conclusion

In this paper, we design and implement a hardware-efficient probabilistic-based noise-tolerant circuit, an 8-bit MRF_CLA, in TSMC 0.13µm CMOS process. Instead of directly implementing all valid states, we separate the truth table into two groups according its output logic states and implement it by master and slave MRF networks. By this way, we can maintain the superiority of noise-tolerant performance in MRF design with lower hardware overhead. The measurement results show that the proposed MRF adder can provide 24.5dB of noise-immunity enhancement as compared with its conventional CMOS design. The transistor count can be saved 42% as compared to the state-of-art MRF design [1]. With better MRF design and nanofabrication technology, we expect the performance to improve further.

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