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Citation	Park, M., and M. Perrott. "A 0.13[mu]m CMOS 78dB SNDR 87mW 20MHz BW CT [DeltaSigma] ADC with VCO-based integrator and quantizer." Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International. 2009. 170-171,171a. ©2009 IEEE.
As Published	http://dx.doi.org/10.1109/ISSCC.2009.4977362
Publisher	Institute of Electrical and Electronics Engineers
Version	Final published version
Citable link	http://hdl.handle.net/1721.1/60071
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9.5 A 0.13μm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-Based Integrator and Quantizer

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Voltage-controlled oscillator (VCO) based ADCs have become a topic of great interest due to the unique and attractive signal-processing properties they offer in the design of oversampling converters. Assuming a ring-oscillator structure, the outputs of a VCO toggle between two discrete levels (V_{DD} and GND) like a CMOS digital gate, enabling simple multibit quantization using D-flip-flops. Since only one VCO output phase transitions at a given sampling instant while all others saturate to the positive/negative supply, quantization is robust to flip-flop voltage offsets and metastability, and has guaranteed monotonicity. Furthermore, the VCO behaves as a CT integrator in that its output phase is proportional to the time integral of the applied control voltage. As long as it oscillates, the VCO output phase accumulates endlessly, implying that it is also an integrator with infinite DC gain.

However, the nonlinearity in the VCO's voltage-to-frequency (K_v) transfer characteristic seriously limits the resolution of VCO-based ADCs (Fig. 9.5.1, top). In all prior published work, the VCO output frequency is the desired output variable due to its proportional relationship with the input signal. Therefore, exercising the full DR of these converters requires the input signal to span the entire nonlinear K_v transfer characteristic, incurring harmonic distortion and limiting resolution to less than 8 ENOB [1]. While the circuit in [2] improves distortion performance by placing a high-gain filter before the VCO and employing negative feedback, K_v nonlinearity still limits resolution to less than 11 ENOB in a 20MHz bandwidth.

In this paper we demonstrate a new technique that eliminates the impact of K_v nonlinearity by preserving the integral relationship of the VCO output phase to the input signal (Fig. 9.5.1, bottom). Leveraging the VCO output phase directly precludes the need to span the entire nonlinear K_v characteristic since small perturbations (in the range of 10s of mV) at the tuning node are sufficient to shift the VCO phase by a substantial amount. Since an open-loop VCO is sensitive to frequency offsets and drift, and easily saturates its phase detector for large input signals, some form of negative feedback is necessary. Here, a multibit DAC subtracts the previously quantized phase value from the VCO input, creating a residue that is integrated during the next clock cycle. This feedback loop not only allows large signals to drive the VCO without incurring distortion from K_v nonlinearity, but also it is a 1st-order CT ΔΣ ADC loop, and it therefore 1st-order shapes quantization noise.

Although this simple 1st-order architecture is largely free of distortion from K_v nonlinearity, a higher-order quantization noise-shaping filter is needed to achieve >11 ENOB resolution in a 20MHz bandwidth. To that end, a 4th-order architecture that requires only 3 opamps (a 4th integration is performed by the VCO) with a 900MHz sampling rate (OSR=22.5) and a 4b quantizer/DAC, is chosen (Fig. 9.5.2). A feedback loop delay compensation scheme similar to the one reported in [3] is adopted here. But since the quantizer can only be stimulated by the integrated voltage-to-phase signal, the compensation is implemented using a digital 1st-order difference circuit (to cancel the integration) and an RZ DAC. The highly digital nature of the VCO integrator/quantizer is observed in Fig. 9.5.3. The VCO delay element is based on a current-starved inverter, and enables pseudo-differential control as well as frequency and K_v tuning to cover process variations. A sense-amplifier flip-flop (popular in digital memory designs) quantizes the VCO output phase. Phase detection and 1st-order difference computation are achieved using static CMOS XOR gates and TSPC flip-flops.

Opamp-RC integrators are chosen for their linearity and ability to drive resistive loads. A modified nested-Miller topology [4] is implemented, and achieves moderate gain (>60dB) and wide unity-gain bandwidth (>3GHz) for fast set-tling. Since its noise appears directly at the input, the 1st opamp consumes the most current (15mA), while the 2nd and 3rd opamps consume half as much. Each integrator includes a fixed capacitance and a 5b binary-weighted capacitor bank to enable tuning over the combined RC process variation of ±40%.

Current-steering NRZ and RZ DACs are implemented for their fast switching speeds. Unit-element mismatch errors in the main NRZ feedback DAC appear directly at the input of the converter and can seriously degrade SNDR. Errors from the minor-loop NRZ and RZ DACs are suppressed by the preceding loop filter gain, but can still limit performance when >11 ENOB resolution is desired. Therefore, DEM must be performed on all feedback DACs, as indicated by the shaded regions in the system schematic of Fig. 9.5.2. Fortunately, it is shown in [5] that when a ring VCO's quantized output phases are 1st-order differenced, a thermometer code is generated that is equivalent to a 1st-order dynamic-weighted-averaging (DWA) sequence. Consequently, if these thermometer bits are tied directly to the RZ DAC unit elements, then the DAC mismatch is 1st-order shaped (Fig. 9.5.4, top). DWA need only be explicitly performed on the undifferentiated thermometer code that drives the NRZ DACs, a computation that has a full sample period to complete (Fig. 9.5.4, bottom).

The architecture in Fig. 9.5.3 is fabricated in a 0.13μm CMOS process, occupying an active area of 0.45mm² (Fig. 9.5.7) and dissipating 87mW from a 1.5V supply, with the analog and digital supplies drawing roughly 46mA and 12mA, respectively. Simulations indicate that the DWA logic consumes more than 75% of the digital power due to the use of current-mode logic to meet timing margins, with the VCO phase quantizer flip-flops and clock generation/distribution circuits comprising the remainder. The SNR and SNDR versus input amplitude curves (Fig. 9.5.5) are calculated over a 20MHz input bandwidth. For a 2MHz -2.4dBFS input tone, the ADC achieves a peak SNR of 81.2dB, and a peak SNDR of 78.1dB (12.7 ENOB, FOM ~330 fJ/conversion-step). A table summarizing the ADC performance is shown in Fig. 9.5.6.

An FFT of the ADC output with a 2MHz input signal at -2.4dBFS is shown in Fig. 9.5.5. The peak SNR is 3dB lower than anticipated due to a slight increase in the noise floor in the 5-to-20MHz range, and the peak SNDR is 3dB lower than the peak SNR due to the presence of even and odd-order distortion tones (present even with no input power). Simulations suggest that these errors are caused by mismatches in the main NRZ DAC unit-element currents and switching transients (ISI). Varying the DAC switch buffer's voltage supply provides evidence of ISI, as perturbing the supply worsens in-band distortion due to larger clock/data charge injection and slower switching transients. While results indicate that SNDR is improved with better matching and a lower-ISI DAC structure, they more importantly demonstrate that the architecture is robust to K_v nonlinearity, and that the VCO-based ADC is viable for high-performance (≥12 ENOB, 20MHz bandwidth) applications.

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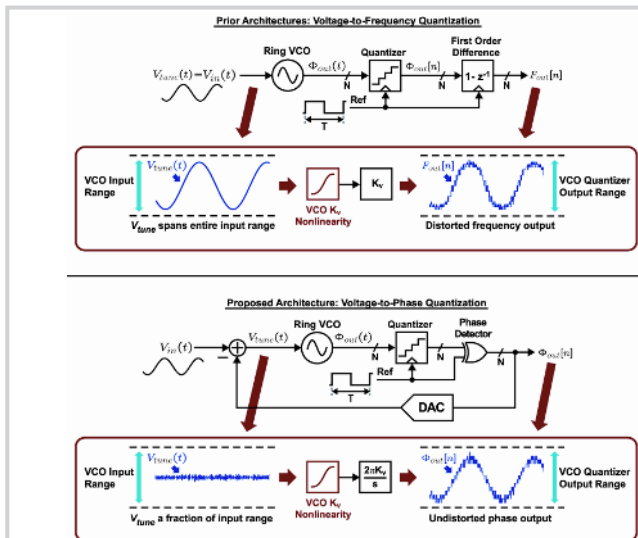
Figure 9.5.1: Block diagrams of previously reported voltage-to-frequency VCO-based ADCs [1] (top) and the proposed voltage-to-phase VCO-based ADC.
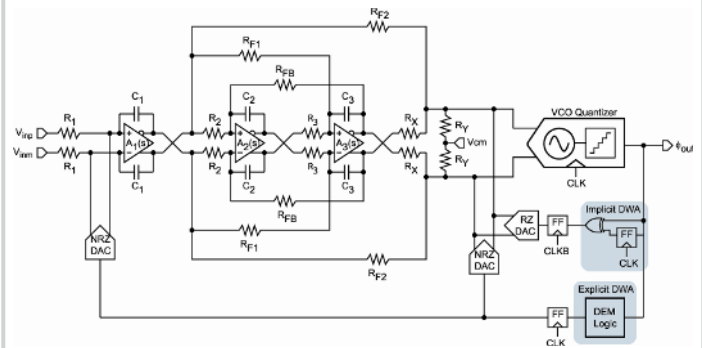

Figure 9.5.2: 4th-order CT $\Delta\Sigma$ VCO-based ADC schematic. The 4th integration is performed by the VCO integrator, and hence only 3 opamps are used.
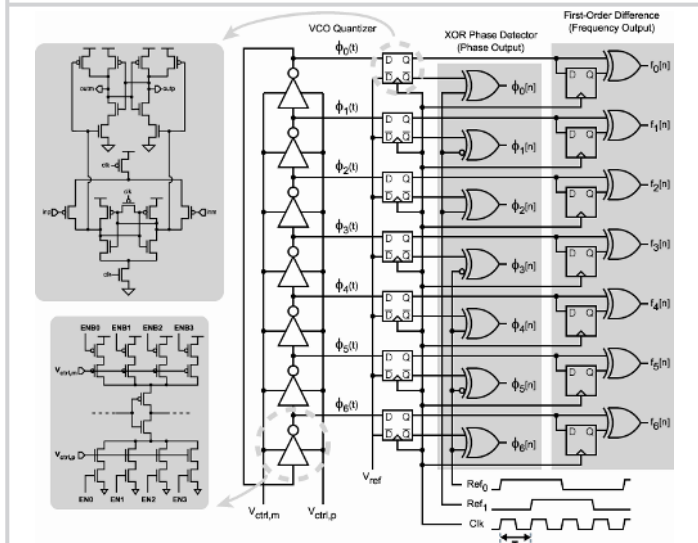

Figure 9.5.3: 3b example of the VCO integrator and quantizer circuitry, associated phase detector and 1st-order difference logic.
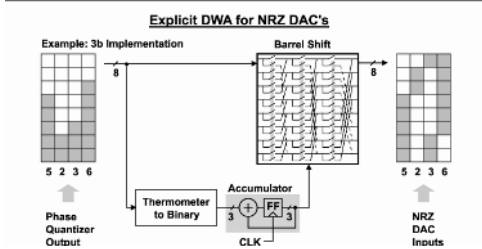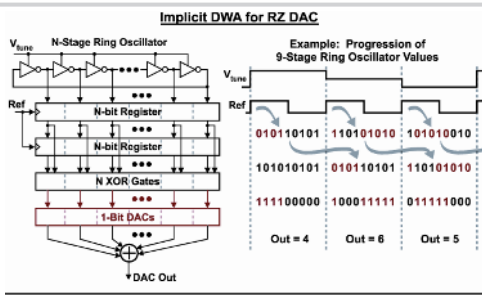

Figure 9.5.4: Implicit DWA from VCO quantization and differentiation (top), and explicit DWA implementation (bottom).
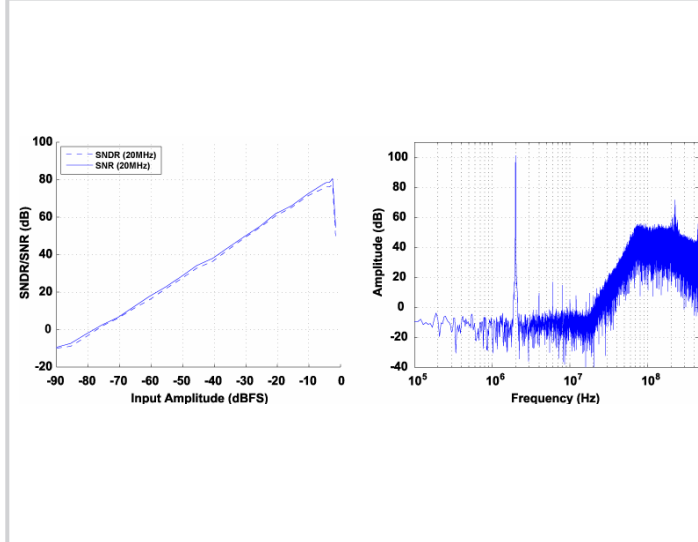

Figure 9.5.5: Measured SNDR/SNR over a 20MHz bandwidth while sweeping input amplitude (left), and a 10,000-point FFT for a 2MHz -2.4dBFS input tone (right).

Specification	Value
Sampling Frequency	900MHz
Input Bandwidth	20MHz
Peak SNR	81.2dB
Peak SNDR	78.1dB
Analog Power	69mW (1.5V)
Digital Power	18mW (1.5V)
FOM = power/(2*BW*2^{ENOB})	330fJ/conv.
Active Area	0.45mm^2
Technology	0.13um IBM CMOS

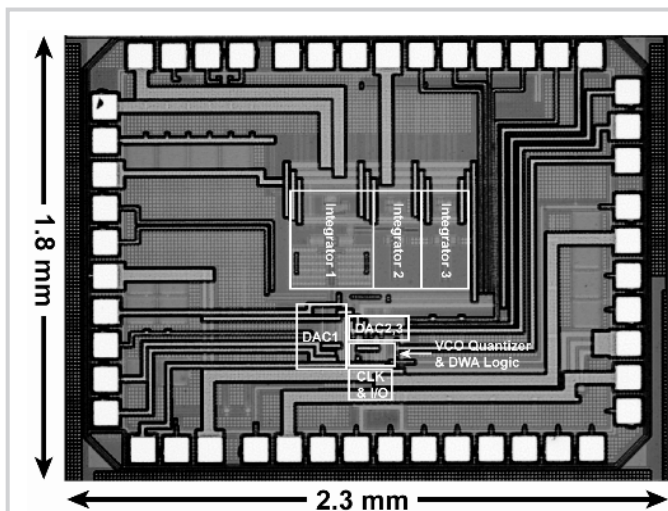Figure 9.5.6: Summary table of results.

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Figure 9.5.7: Die micrograph of the ADC implemented in 0.13μm CMOS. The total active area is 0.45mm^2. DAC1 corresponds to the main NRZ feedback DAC, and DAC2 and DAC3 correspond to the minor-loop NRZ and RZ feedback DACs.