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10.7 A 0.16mm² Completely On-Chip Switched-Capacitor DC-DC Converter Using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS

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Reducing power consumption through V_{DD} scaling is a major trend in nanometer CMOS circuits. In modern wireless SoCs, multiple power domains operate below 1.2V and draw less than 10mA of current. Currently, these domains are powered from a 1.8V rail through a low drop-out linear regulator (LDO). The 1.8V rail is obtained from a Li-ion battery using a switching regulator with off-chip passives. It is highly inefficient to power circuit blocks that operate below 1.2V through LDOs. Switched-capacitor (SC) DC-DC converters are a viable solution to replace LDOs in some on-chip power domains but they currently occupy a large on-chip area [1]. Also, the voltage regulation schemes employed by current SC converters are either unsuitable in wireless systems or do not provide high efficiencies in on-chip use cases due to the dominance of bottom-plate and switching losses [2]. In this paper, a completely on-chip SC DC-DC converter that uses a digital capacitance modulation scheme to achieve voltage regulation is presented. The converter occupies only 0.16mm² in total area and provides up to 8mA of current to output voltages between 0.8V to 1V from a 1.8V input while switching at 30MHz.

Figure 10.7.1 shows the G2BY3 gain setting (gain of 2/3) used to deliver load voltages between 0.8V to 1V. The signals ϕ_1 and ϕ_2 are non-overlapping phases of a clock switching at frequency f_s. The circuit is two-way interleaved to reduce input current and output voltage ripple. The load current handling capability [2] of the G2BY3 gain setting is given by

$$I_L = Q_L f_s = 144C_B\,(1.2–V_L)f_s \qquad (1)$$

where $64C_B$ is the total on-chip charge-transfer capacitance used, Q_L is the charge delivered to the load every switching cycle and I_L is the current delivered at the load voltage of V_L. It can be observed from Eq. (1) that in order to regulate the output to a specified voltage V_L while delivering a load current I_L, the only available knobs are f_s or Q_L. Pulse frequency-modulation (PFM) [2] schemes change f_s to maintain regulation. While this is useful in certain digital systems, in wireless systems, where the digital load being supplied co-exists with critical analog/RF blocks, tones that cover a wide frequency range are challenging (if not impossible) to handle. Hence, a constant frequency regulation scheme is required. Constant frequency control methods often use duty cycle [1] or segmented switch width [3] modes of control to change Q_L. These control schemes do not scale switching and/or bottom-plate losses with change in load current leading to a drop in efficiency at low loads. Also, effective regulation with a wide change in load current is difficult to achieve with the abovementioned methods especially when taking process variations into account.

To overcome these problems, a digital-capacitance-modulation (DCM) mode of control is introduced, where regulation is maintained by controlling the amount of capacitance that takes part in the charge transfer process. Figure 10.7.2 shows how the capacitors are partitioned for one tile of the interleaved structure. The charge transfer capacitance ($16C_B$) is broken into 5 different banks of sizes 8×, 4×, 2×, 1× and 1×,FINE. As the size of the charge transfer capacitors change in each bank, so do the width of the switches, such that every bank has similar charge/discharge times. The 8×, 4×, 2× and 1× banks are enabled by the COARSE mode signals *C<0:3>*, respectively. The 1×,FINE bank remains always on. The charge-transfer capacitance in this bank is further subdivided into three capacitances of value $C_B / 7$, $2C_B / 7$ and $4C_B / 7$. While the $C_B / 7$ capacitance is always engaged, the other capacitances are engaged only when the FINE signals *F<0>* and *F<1>* are high.

Figure 10.7.3 shows the architecture of the SC DC-DC converter. The switch matrix contains the capacitor banks and the switches. The converter tries to maintain the feedback voltage V_{FB} within the hysteretic band $[V_{REF} - \Delta V, V_{REF} + \Delta V]$, where V_{REF} is a reference voltage (0.53V) and ΔV is set to 20mV. The load voltage is set digitally by the 3-bit reference signal *REF<0:2>*. The 2 clocked comparators COMP1 and COMP2 help maintain regulation of V_L by generating the *GO_DOWN* or *GO_UP* signals when V_{FB} goes above or below the hysteretic band. These signals feed into the logic block where the MODE DECISION unit generates the *FINE/COARSE* and *DCM/PFM* signals which determine the operating mode of the converter. Following this, the ADD/SUB block suitably modifies the *C<0:3>, F<0:1>* signal which controls the amount of charge-transfer capacitance engaged. An extra comparator COMP3 that generates the *COARSE_EN* signal is used to detect sudden changes in load voltage.

The converter normally operates in the DCM mode but at very light load conditions (<500μA), it automatically switches to PFM mode control to maintain efficiency by making the *DCM/PFM* signal go low. The transition from DCM to PFM occurs when the logic block in Fig. 10.7.3 encounters multiple *GO_DOWN* signals when *C<0:3>* is at '0000'. This happens when the output load current is very low. It returns to DCM mode when the *GO_UP* signal goes high signifying an increase in the load current.

For fast transient response, the converter employs COARSE regulation during startup and load transients. In this mode, only *C<0:3>* is changed, *F<0:1>* is set to '11', and the capacitor step size for regulation is $1C_B$. Once the transients have settled, to prevent limit cycling with COARSE regulation, the converter enters FINE regulation where the capacitor step-size is reduced to $2C_B / 7$, as shown in Fig. 10.7.2. This enables the converter to settle within narrow hysteretic bands without any unwanted low-frequency oscillations.

As shown in Fig. 10.7.4, the transition from the COARSE to FINE mode occurs either when there is a *GO_UP* signal followed by a *GO_DOWN* signal or when all 4-bits in *C<0:3>* are zero and a *GO_DOWN* signal occurs. The first situation happens when the load voltage transitions from falling to rising and the second case occurs when the load current is too small. The transition from the FINE to COARSE mode occurs when the *COARSE_EN* signal output by COMP3 goes high. This happens during sudden load increases and helps the converter to settle fast while minimizing the droop in V_L. The rising edge of the *COARSE_EN* signal also causes *C<0>* to go high further reducing the settling time.

Figure 10.7.5 shows measured waveforms of the load transient response. With the comparator COMP3 enabled, the converter can transition to the COARSE mode and hence settles within 120ns when the load current changes from 270μA to 7.6mA. With COMP3 disabled, it takes 1.2μs for the converter to settle, with a more pronounced droop in V_L.

Figure 10.7.6a shows the measured efficiency of the converter with change in V_L while delivering a load current of 5mA. The converter provides above 60% efficiency over the load voltage range from 0.8V to 1V, which is much higher than that of LDOs and other completely on-chip SC converters [4]. Figure 10.7.6b shows the efficiency with change in I_L while delivering a 0.9V output. The DCM mode of control helps to keep the efficiency constant over a wide range of load current. At light loads, the PFM mode control sets in to reduce switching losses and improve efficiency.

Figure 10.7.7 shows the die micrograph and performance summary of the 45nm CMOS test chip. The active area of the SC converter which includes the charge-transfer and load capacitors is only 0.16mm². All the capacitors used are obtained using gate-oxide capacitors.

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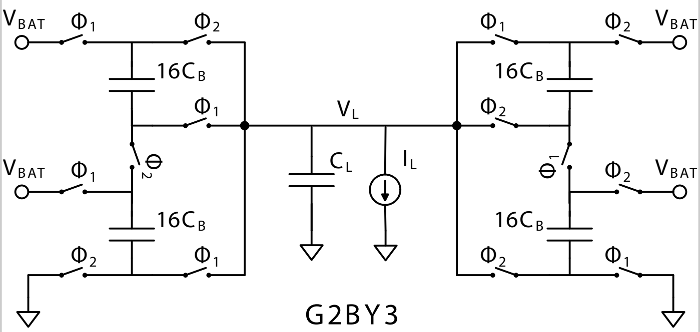

Figure 10.7.1: A two-way interleaved G2BY3 gain setting to provide voltages below 2/3rd of the input voltage (1.8V). The total on-chip charge- transfer capacitance used is 534pF (=64C$_B$), and the load capacitance is 700pF.

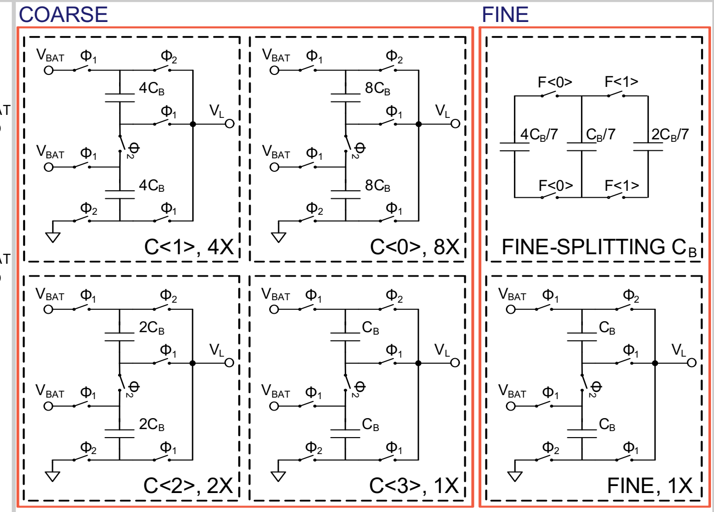

Figure 10.7.2: Binary-weighted partitioning of the charge transfer capacitors and switches for digital capacitance modulation. *C<0:3>* turns ON or OFF the coarse blocks. *F<0:1>* controls the finer splitting of the 1C$_B$ capacitor.

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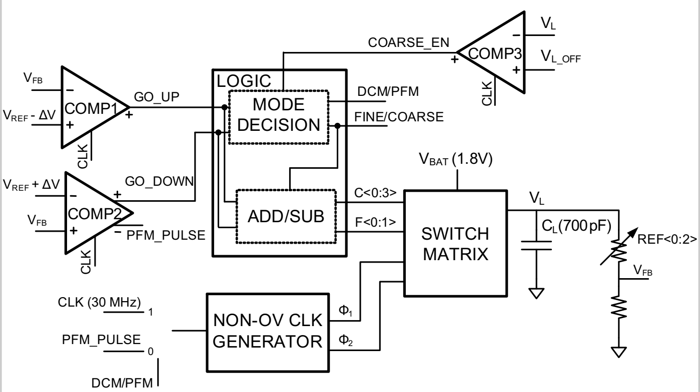


Figure 10.7.3: Architecture of the switched-capacitor DC-DC converter system. COMP3 compares V_L with a reference voltage V_{L_OFF} which is generated on-chip and is designed to be 100mV less than the required V_L.

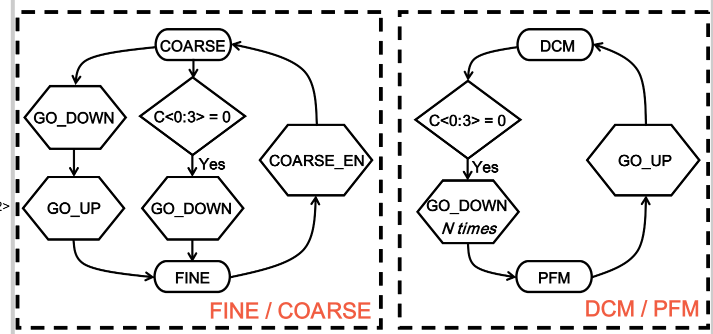


Figure 10.7.4: Flowchart showing the events leading to transition between FINE/COARSE modes of regulation and DCM/PFM modes of control. '*N*' can be set to 4 or 8.

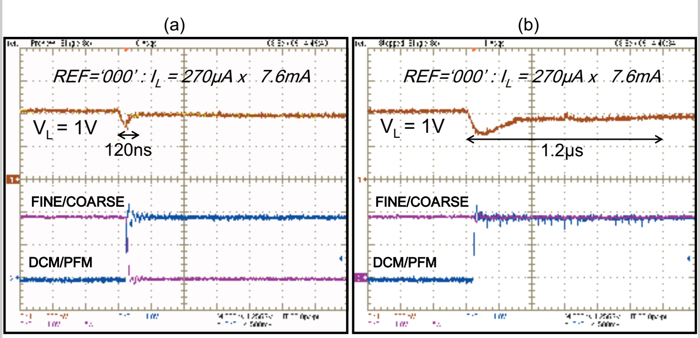


Figure 10.7.5: Measured load transient performance of the SC converter with COMP3 (a) enabled and (b) disabled for a load current change from 270μA to 7.6mA. The converter is in PFM mode when *DCM/PFM* is low and in COARSE mode when *FINE/COARSE* is low.

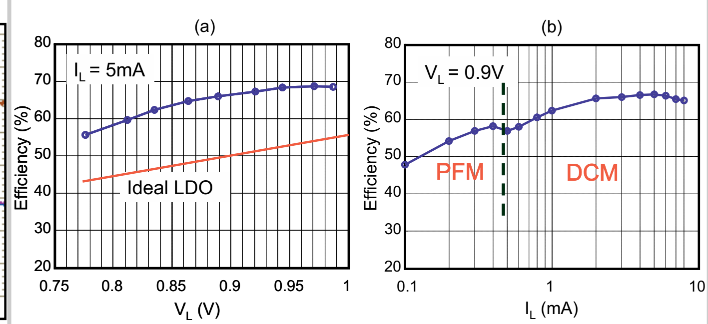
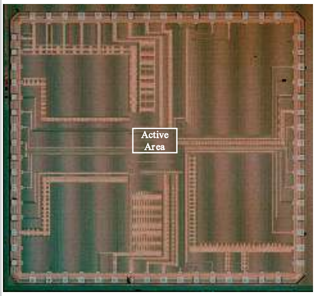


Figure 10.7.6: Efficiency of the switched-capacitor DC-DC converter with (a) change in load voltage while delivering a load current of 5mA (b) change in load current while delivering a load voltage of 0.9V from a 1.8V input supply.



Technology	45nm CMOS
Active Area	0.16mm^2
Switching Frequency	30MHz
Input Voltage	1.8V
Output Voltage	0.8V – 1V
Maximum Load Current	8mA
Peak Efficiency	69%
Charge Transfer Capacitance	534pF
Load Capacitance	700pF
Capacitor Type	Gate-oxide

Figure 10.7.7: Die micrograph of the switched capacitor DC-DC converter identifying the area consumed by the active blocks. The table shows a summary of the key features of the converter.

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