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A 0.18 μm CMOS Voltage-to-Frequency Converter with Low Circuit Sensitivity

K.C. Koay, *Student Member, IEEE,* and P.K. Chan, *Senior Member, IEEE*

***Abstract*—A process, voltage and temperature insensitive resistor-to-frequency converter is proposed. This insensitivity is achieved by matching the current defining capacitor in a novel switched-capacitor (SC) voltage-to-current (V-I) converter with the integrating capacitor in a conventional relaxation oscillator. Implemented in 0.18 μm CMOS technology, the SC V-I converter together with the relaxation oscillator and voltage regulator occupies 0.45mm^2. The proposed work has shown a sensitivity of 199.9 Hz/(μΩ/Ω) which is based on a center frequency of 125kHz. Testing with a commercial sensor, the sensor interface has demonstrated a sensitivity of 1.269 kHz/psi. The sensor interface consumes only 112.5 μW at 1.5V power supply. Therefore, it is suitable for Internet-of-Things applications.**

***Index Terms*— Transconductor, switched-capacitor circuit, voltage-to-current converter, voltage-to-frequency converter, Internet-of-Things**

I. INTRODUCTION

AS the Internet-of-Things becomes more popular, a robust and low-power sensor network system is highly desirable. Resistive sensors are widely preferred due to its insensitive to electromagnetic interference, relatively higher immunity against environmental parasitic capacitances, low cost and ease of integration [1], [2]. They are typically used in physical force related to sensing parameters such as pressure, stress and strain. Any change in the physical force will be converted into change in resistance. To convert this variation of resistance into change in voltage, the resistive sensors are typically configured in a Wheatstone Bridge configuration.

The maximum change in resistance for the resistive sensors are typically 2% in terms of its bridge resistance. This corresponds to a change of 24mV for a full Wheatstone Bridge sensor with a supply voltage of 1.2V. Hence, this change of voltage will often be amplified and converted into digital code for transmission to permit ease of maintaining signal fidelity [3]–[7]. Another way of maintaining signal fidelity is to convert this voltage signal into frequency domain signal [8]–[13]. The key benefits of this conversion scheme are that the output signal is having higher noise immunity compared to voltage domain signal and it allows ease of interfacing with digital circuit on the basis of little or no synchronization [11], [14]. Conventional voltage-to-frequency (VF) converter often requires a resistor for current conversion and a capacitor to convert the current into frequency domain signal through a relaxation oscillator. Due to the difference in device types used, the output frequency will vary widely across process and temperature variations. This in turn requires more elaborate calibration process, causing higher time to market and increase the production cost.

To minimize the process variation caused by the mismatch between device types, a clocked VF converter was proposed [15]. In this work, the switched-capacitor (SC) technique is utilized to translate voltage input into frequency output. This eliminates the need of resistor, thus providing better stability across process and temperature variations. However, when the output frequency is quantized, the quantization effect is worsened when the output frequency approaches the clock frequency. To eliminate this issue, a SC VF converter is proposed. This converter will convert the input voltage into a continuous-time current through a SC voltage-to-current converter with the embedded integrator. The smoothed signal current is then injected into an integrating capacitor and converted into a frequency domain signal. As a result, this eliminates the quantization issue in [15] while maintaining the output frequency stability across process variation and temperature variation. Fig. 2 shows the block diagram of the proposed VF converter.

In Section II, the respective building block will be described. The measurement results will be presented in Section III. In Section IV, the performance of SC VF converter will be compared with other state-of-the-art works. Finally, the concluding remark will be drawn in Section V.

II. PROPOSED SENSOR INTERFACE

Fig. 1 shows the proposed sensor interface that converts a Wheatstone Bridge sensor output voltage into a frequency domain signal output. The proposed sensor interface consists of two main blocks, which are the VI converter and the current-to-frequency (IF) converter. Table I shows the capacitance of each capacitor used in the design. The Wheatstone Bridge sensor translates the change of physical parameter, such as pressure in this case, into the resistive change on each arm of the Bridge.

The differential output of a full Wheatstone bridge is given as

$$V_{IN} = \frac{\Delta R}{R} V_{DD} \tag{1}$$

where V_{IN} is the differential output voltage of sensor that will be processed by the proposed interface, ΔR is the variation of resistance relative to the bridge resistance, R, and V_{DD} is the supply voltage of the Wheatstone Bridge. As shown by (1), the output voltage, which refers to the input voltage of the proposed sensor interface, is linearly proportional to the supply voltage. In order to maintain a stable supply, a low dropout (LDO) regulator with an output voltage of 1.2V is

The authors are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798. (e-mail: koay0013@e.ntu.edu.sg; epkchan@ntu.edu.sg).

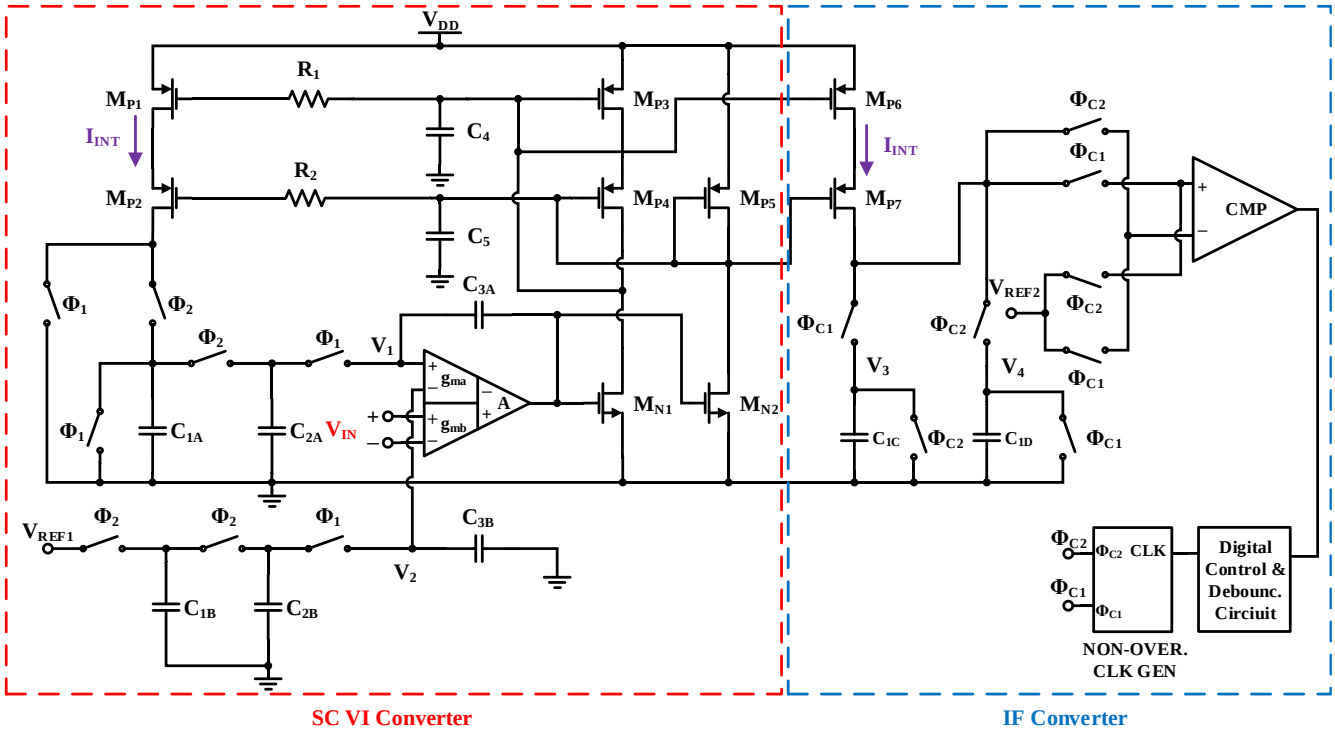


Fig. 1 Proposed SC VF converter.

adopted to power the Wheatstone Bridge sensor. In this design, the sensor system is targeted to achieve untrimmed accuracy of less than 1.5%, as the conventional pressure sensor will have a span variation of 5% full scale span variation. Since the error caused by the delay, τ, is $\tau \times f_{OUT}^2$, in conjunction with the comparator delay in the range of 10ns

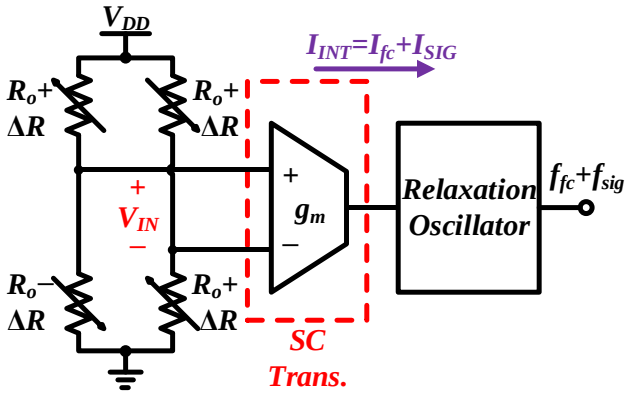


Fig. 2 Block diagram of proposed VF converter.

to 25ns, the maximum output frequency is chosen as 185kHz to limit the error to 0.5%. Therefore, the chosen sensitivity is based on the input range, the ratio of the input pairs' transconductance, the current mirror ratio and the capacitor ratio. To maintain good matching for the current mirror and capacitor, their ratio is fixed as 1/1. For the input pair, a gain of 2 is adopted in the design. With this design criteria, when the sensitivity is chosen as 199.9Hz/(μΩ/Ω), this gives a theoretical center frequency of 125kHz with an input range of ±0.02 Ω/Ω.

The design of VI converter will be discussed in subsection A whereas the IF converter will be discussed in subsection B. The chopping Differential Difference Amplifier (DDA) that is used in the VI converter will be discussed in the subsection C.

TABLE I
SIZING OF CAPACITORS IN THE PROPOSED SC VI CONVERTER

Cap.	Size (pF)	Cap.	Size (pF)
C_{1A}, C_{1B}, C_{1C}, C_{1D}	20	C_{3A}, C_{3B}	11
C_{2A}, C_{2B}	2	C_4, C_5	1

A. VI Converter

To transform the sensor voltage into current, a SC VI converter which is based on [16], [17] coupled with a DDA [18], is used. In this work, the SC VI converter is modified to a quasi-differential structure so as to reduce the charge injection as well as clock feedthrough effect. The resistor-capacitor low-pass filters formed by resistors R_1, C_4 and R_2, C_5 are used to filter the switching noise coupled from the drain of M_{P1} and M_{P2} to the gate of M_{P3} and M_{P4}. During Φ_1, C_{1A} is being discharged to ground while C_{2A} is being forced to $V_{REF1}+2V_{IN}$ because the DDA is designed to have a gain of 2. The detailed discussion on the design of DDA will be discussed in Section II-C. At this juncture, C_{2B} is disconnected to C_{1B} and connected to C_{3B}. When the VI converter goes into Φ_2, C_{1A} together with C_{2A} is connected to the drain terminal of M_{P2}. It is being charged up by a constant current, I_{INT}, while C_{1B} and C_{2B} are being charged up by V_{REF1}. In next clock cycle, C_{2A} will then be connected to V_1. The excess positive charge of C_{3A} will be injected into C_{2A} if the voltage on C_{2A} is lower than virtual ground, thus increasing the charging current I_{INT}. On the contrary, if the voltage on C_{2A} is higher than virtual ground, the excess positive charge on C_{2A} will be injected into C_{3A}, thus decreasing I_{INT}.

From [17], the expression for the charging current I_{INT} under a clock with 50% duty cycle can be given as

$$I_{INT} = 2\left(V_{REF1} + 2V_{IN}\right)C_{1A} f_{CLK} = I_{DC} + I_{SIG} \quad (2)$$

where V_{REF1} is the reference voltage employed to generate a dc reference current. This reference current will provide a center frequency for the VF converter. The voltage is chosen to be 150mV in this design. f_{CLK} is the clock frequency generated by off-chip crystal oscillator and chosen to be 500kHz. The I_{DC} and I_{SIG} are the DC current generated from voltage reference and the signal current resulted from the differential output voltage of the Wheatstone Bridge sensor, respectively. Referenced from (2), the targeted design values for I_{DC} and I_{SIG} are 3µA and ±0.96 µA, respectively in this design.

B. IF Converter

To convert I_{INT} into a frequency domain signal, a relaxation oscillator is needed. This relaxation oscillator makes use of a self-chopped topology similar to [19]. The goal is to reduce the offset effect and low-frequency noise introduced by the comparator. During Φ_{C1}, the I_{INT} is injected into C_{1C} while C_{1D} is being discharged to ground. C_{1C} is also connected to the non-inverting input of comparator while V_{REF2} is connected to the inverting input of comparator. At this juncture, the output of comparator is low. When the voltage V_3 is being charged up to pass $V_{REF2}+V_{OFFSET\_COMP}$, the output of comparator will be switched to high. The V_{OFFSET_COMP} is the offset voltage modelled as a DC voltage in series with the V_{REF2}. Besides, a debouncing circuit is used to prevent the noise from causing unwanted switching activity by maintaining the comparator output for about 10ns after each switching activity. The debouncing circuit's output will then go through a non-overlapping clock generator to set the SR latch output to high. The SR latch is used as the output signal for VF converter. This SR latch output will go through another non-overlapping clock generator to trigger Φ_{C2} to high and Φ_{C1} to low. In Φ_{C2}, C_{1D} will be charged up by I_{INT} while C_{1C} will be discharged to ground. In this phase, V_4 will be connected to the inverting input of the comparator while V_{REF2} will be connected to the non-inverting input of comparator. When V_4 is charged up to the value of $V_{REF2} - V_{OFFSET\_COMP}$, the output of comparator will switch to low, thus setting Φ_{C1} to high and Φ_{C2} to low. The output frequency can be obtained as follows:

$$f_Q = \frac{2\left(V_{REF1} + 2\Delta R / R\right) C_{1A} f_{CLK}}{C_{1C}\left(V_{REF2} + V_{OFF\_COMP}\right) + C_{1D}\left(V_{REF2} - V_{OFF\_COMP}\right)} \tag{3}$$

$$f_Q = \frac{2\left(V_{REF1} + 2V_{IN}\right) C_{1A} f_{CLK}}{C_{1C}\left(V_{REF2} + V_{OFF\_COMP}\right) + C_{1D}\left(V_{REF2} - V_{OFF\_COMP}\right)} \approx \frac{\left(V_{REF1} + 2V_{IN}\right) f_{CLK}}{V_{REF2}} = f_{DC} + f_{SIG} \tag{4}$$

where f_{DC} is the output offset frequency and f_{SIG} is the output signal-dependent frequency. From (3), one can deduce that the output frequency, f_Q, is independent of the comparator offset. Moreover, if the capacitors C_{1A}, C_{1B}, C_{1C} and C_{1D} are well matched, the output frequency will be independent of actual capacitor value and only dependent on the reference voltage, the reference frequency and the input voltage signal. It can be seen that f_{DC} can be made to be independent of process, voltage and temperature variations if the reference voltages are generated using a well-matched resistor ladder. With V_{REF1}=150mV, V_{REF2} = 600mV and a V_{IN} of ±24mV, the f_{DC} and f_{SIG}'s range are theoretically calculate as 125kHz and ±40kHz, respectively.

C. Chopping Differential Difference Amplifier

Fig. 3 shows the proposed chopping DDA. This DDA is a folded DDA for M_{P1} and M_{P2}, while a differential amplifier OA_1 with cascode active load for M_{P3} and M_{P4}. This reduces the channel length modulation effect due to the large input common-mode difference between the two input ports. However, conventional biasing for the cascode devices M_{N4} and M_{N5}, where the gate of M_{N4} and M_{N5} are tied to the same biasing voltage, is not ideal for this architecture. This is due to the difference in current density for the cascode devices when the input voltage is varying. In other words, the V_{DS} values of M_{N4} and M_{N5} will vary with the input signal. To reduce the signal dependency, a low-power operational amplifier (op-amp) [20] is used to generate the biasing voltage for M_{N5} so that V_5 and V_6 are equalized. In this design, the DDA is designed to have a gain of 2 between two input ports, V_1-V_2 and $V_{IN+}-V_{IN-}$. This gain aims to widen the signal frequency

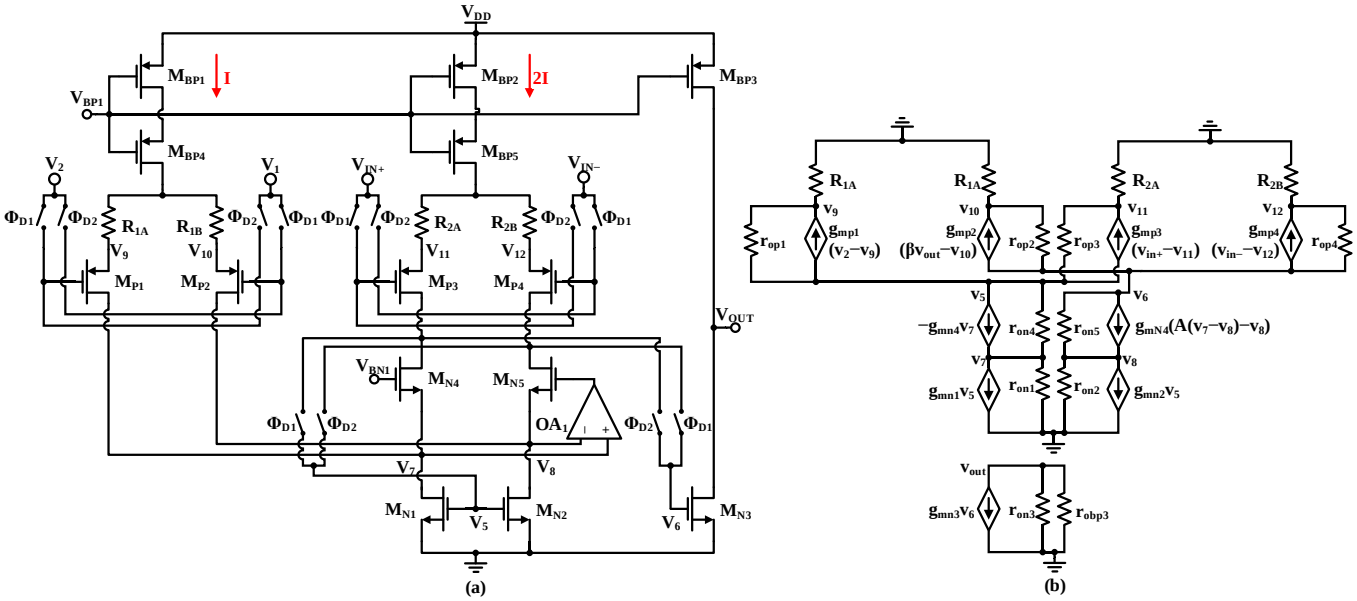


Fig. 3 (a) Proposed DDA (b) Small-signal model of proposed DDA during Φ_{D1}.

range without increasing the size of C_{1A} and C_{1B}. It can be derived through the small-signal model as shown in Fig. 3 (b). Several assumptions are made to simplify the derivation. They are given as follows:

(i) The input pairs and the current mirror pairs have the same transconductance. They are $g_{mp1} = g_{mp2}$, $g_{mp3} = g_{mp4}$, $g_{mn1} = g_{mn2}$ and $g_{mn4} = g_{mn5}$. Although the input pairs will exhibit difference in their transconductances at different input signals, the difference can be reduced through the source-degenerated resistors R_{1A}, R_{1B}, R_{2A} and R_{2B}.

(ii) The input pairs and the current mirror pairs have the identical output impedance. They are $r_{op1} = r_{op2}$, $r_{op3} = r_{op4}$, $r_{on1} = r_{on2}$, $r_{on4} = r_{on5}$.

(iii) The resistance pairs are identical, with $R_{2x} = R = 0.5R_{1X}$.

(iv) The gain factor $g_{mx}r_{ox}$ for each transistor and the gain A for the op-amp is much larger than 1.

(v) As V_2 is close to V_{REF1}, its small-signal value is 0V.

Since V_1 contains the feedback signal, it is equal to βvout, where $\beta=C_{3A}/(C_{2A}+C_{3A})$ during Φ_1 and $\beta=C_{3A}/(C_P+C_{3A})$, with C_P is the parasitic capacitance seen at V_1. As the values of C_P and C_{2A} are much smaller than that of C_{3A}, β is approximately equal to 1. The transfer function is obtained as follows:

$$\frac{v_1}{v_{in}} = \frac{\beta v_{out}}{v_{in}} = \frac{g_{mp3}\left(2g_{mp1}R+1\right)}{g_{mp1}\left(g_{mp3}R+1\right)} \tag{5}$$

From (5), to achieve a gain of 2, g_{mp3} needs to be two times of g_{mp1}. Thus, the current of M_{P3} and M_{P4} needs to be double of M_{P1} and M_{P2} because M_{P1}-M_{P4} are biased in the subthreshold region.

To eliminate the offset of amplifier, the chopping technique is employed by chopping the input pairs M_{P1}-M_{P2} and M_{P3}-M_{P4}, together with the active loads M_{N1}-M_{N2}. The offset for the transistors pair can be modeled as a voltage source at the gate of transistor. For simplicity, M_{P1}, M_{P3} and M_{N2} are assumed to have the respective offset voltage of V_{off_P1}, V_{off_P3} and V_{off_N2}. The effect of the offset on V_1 during Φ_{D1} is then derived to give

$$V_1 = \begin{cases} V_{REF1} + 2V_{IN} + V_{off\_DDA} & t \subseteq \Phi_{D1} \\ V_{REF1} + 2V_{IN} - V_{off\_DDA} & t \subseteq \Phi_{D2} \end{cases} \tag{6}$$

with $V_{off\_DDA} = V_{off\_P1} + 2V_{off\_P3} - V_{off\_N2}g_{mn1}(2g_{mp1}R+1)/g_{mp1}$. Substituting (5) into (6), we have

$$f_Q = \begin{cases} \dfrac{\left(V_{REF1} + 2V_{IN} + V_{off\_DDA}\right) f_{CLK}}{V_{REF2}} & t \subseteq \Phi_{D1} \\ \dfrac{\left(V_{REF1} + 2V_{IN} - V_{off\_DDA}\right) f_{CLK}}{V_{REF2}} & t \subseteq \Phi_{D2} \end{cases} \tag{7}$$

From (7), it can be observed that the average output frequency of two phases is independent of offset voltage of DDA.

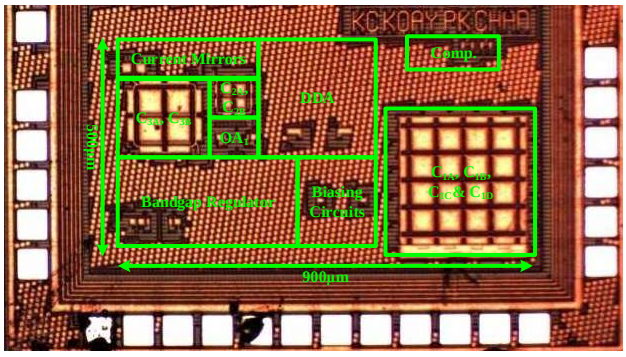
The measurement of the output frequency at each of the Φ_{D1} and Φ_{D2} chopping phase will begin after 100μs from the start of Φ_{D1} and Φ_{D2}, respectively. This is to cater for the settling time needed by the VI converter. The frequency of VF converter will then be calculated and the average frequency of Φ_{D1} and Φ_{D2} will be obtained.

III. Experimental Results

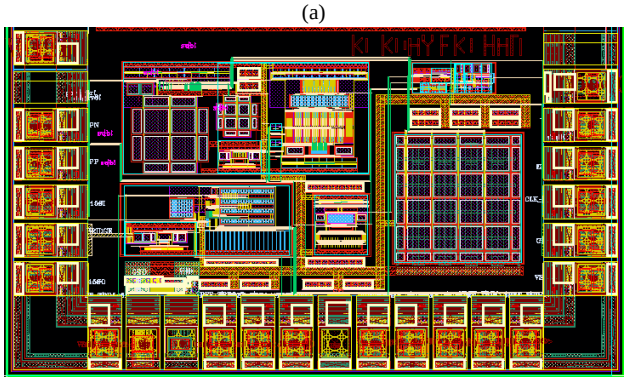
Implemented in AMS-0.18μm CMOS technology, the VF converter occupies an active area of 0.45 mm^2 as depicted in Fig. 4. The equipment employed for testing are Agilent DSO-X 4043A oscilloscope, Agilent 33600A function generator, Agilent 34461A multimeter, and Wiltech AS20W compressor and vacuum pump. The performance of the chips has been measured in three types of configuration. They are: (i) VF converter, (ii) full Wheatstone bridge configuration and (iii) pressure sensor configuration.

A. VF Converter

In this configuration, the supply current of VF converter is 75μA at 1.5 V supply voltage. The measured transient waveforms are shown in Fig. 5, with the chopping clock displayed as the top trace and the VF



(a)



(b)

Fig. 4 (a) Chip micrograph and (b) layout of the VF converter.

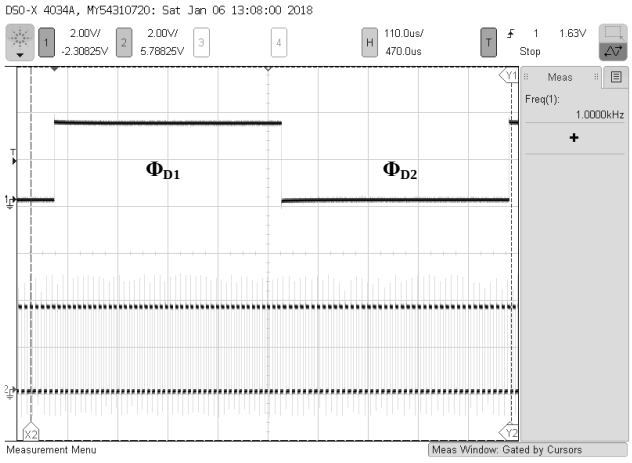


Fig. 5 Transient waveform of the VF converter.

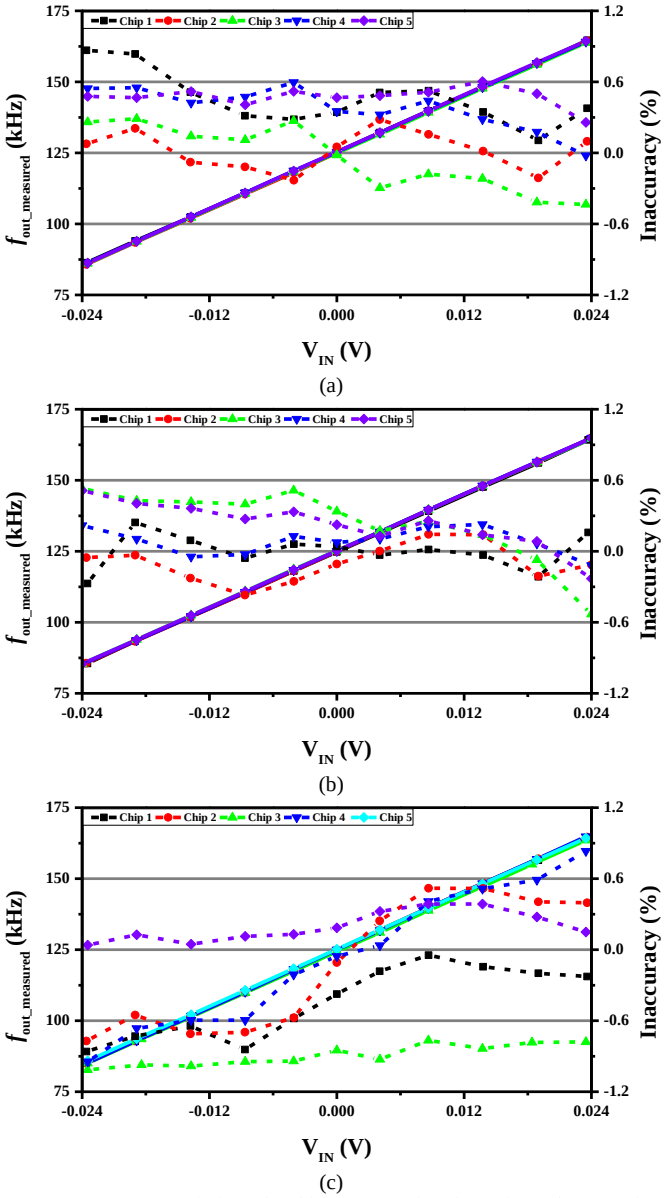


Fig. 6 Temperature variation of 5 chips at (a) 80 ˚C, (b) 25 ˚C and (c) −40 ˚C, with solid lines representing the transfer function of VF converters and dashed lines representing the accuracy of VF converters.

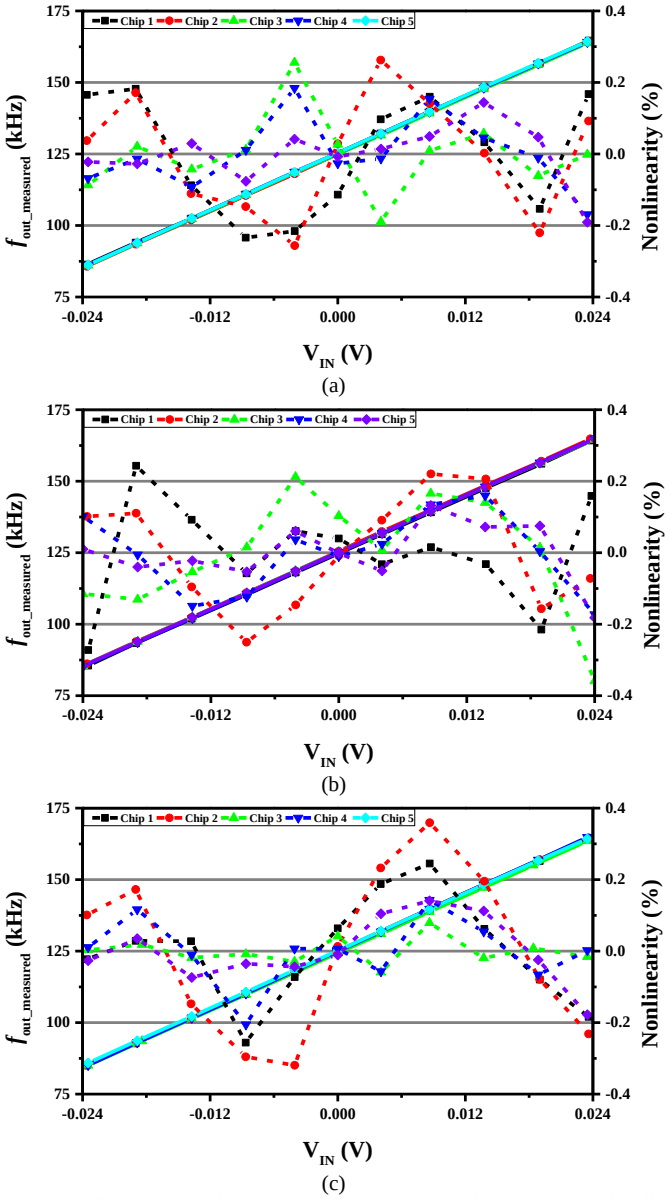


Fig. 7 Nonlinearity of 5 chips at (a) 80 ˚C, (b) 25 ˚C and (c) −40 ˚C, with solid lines representing the transfer function of VF converters and dashed lines representing the nonlinearity of VF converters.

converter's output displayed as the bottom trace. Fig. 6 has shown the transfer function of VF converter which is characterized at temperature of 80 ˚C, 25 ˚C and −40 ˚C. It is noted that these measurements are conducted by injecting a DC input differential voltage with a value ranging from −24mV to 24mV. The inaccuracy is defined as follows:

$$\text{Inaccuracy} = \frac{f_{out\_measured} - f_{out\_ideal}}{f_{ideal\_max} - f_{ideal\_min}} \times 100\% \quad (8)$$

where $f_{out\_measured}$ is the measured output frequency, f_{out_ideal} is the ideal output frequency, f_{ideal_max} is the maximum output frequency at V_{in}=+24 mV, which is 165kHz. f_{ideal_min} is the minimum output frequency at V_{in}=−24 mV, which is 85kHz. Along with the transfer function, the measured inaccuracies are illustrated in Fig. 6. At temperature of 80 ˚C, 25 ˚C and −40 ˚C, the average sensitivity of sensor is obtained as 1.6605 kHz/mV, 1.6609 kHz/mV and 1.6822 kHz/mV, respectively whereas the average offset frequency is obtained as 125.2 kHz, 125.02 kHz and 124.79 kHz. Over all temperatures, the five measured chips have shown worst inaccuracy of less than 1.1% at -40 ˚C. This is highly stable when compared to that of conventional counterparts which rely on the accuracy of a resistor and a capacitor. For CMOS process, a resistor will have a typical variation of ±15% while a capacitor will have a variation of about ±10% across process corners. This leads to a variation of +56.8% and −30.4% in the output frequency as encountered for conventional VF converters. The non-linearity of sensor interface is also measured and the results are depicted in Fig. 7. The nonlinearity is defined as follows:

$$\text{Nonlinearity} = \frac{f_{out\_measured} - f_{out\_bfc}}{f_{out\_bfc\_max} - f_{out\_bfc\_min}} \times 100\% \quad (9)$$

where f_{out_bfc} is the best-fit-curve output frequency at the given input voltage, $f_{out\_bfc\_max}$ is the maximum best-fit-curve

output frequency and $f_{out\_bfc\_min}$ is the minimum best-fit-curve output frequency. As revealed in Fig. 7, the worst nonlinearity is 0.36%. The frequency variation exhibited by the interface due to DC supply variation is also measured at an output frequency of 165kHz at 25 ˚C. The measurement results are shown in Fig. 8. The worst-case frequency variation is observed as 3.7 Hz/mV.

B. *Full Wheatstone Bridge Configuration*

The proposed VF converter is tested with a full Wheatstone Bridge test setup. The test setup is shown in Fig. 9. Emulating a sensing bridge with a bridge resistance of 10 kΩ ± 2%, each R_1, R_2, R_3 and R_4 consists of a 25-turns potentiometer of 1 kΩ and a fixed resistor of 9.76 kΩ. The resistance variation of R_1 and R_4 are equal in magnitude but in opposite direction than that of R_2 and R_3. The transfer function of the interface with respect to the bridge resistance change is shown in Fig. 10. The test subject is based on one of the 5 chips, which is chip 5 in this case. The measured nonlinearity is −0.11% and the worst-case inaccuracy is 0.34%. The measured sensitivity of sensor interface with the full Wheatstone bridge is 199.9 Hz/(μΩ/Ω). while the offset frequency is obtained as 125.2 kHz. To find the frequency uncertainty of sensor interface, 128 samples of the output frequency is taken with Altera DE0 [21] at the maximum bridge imbalance of +2%. Fig. 11(a) depicts the distribution of the output frequency. The standard deviation of the measured output frequency is 22.35 Hz. Fig. 11 (b) depicts the input referred power spectrum density of the proposed interface based on 128 points-FFT. The input referred noise is estimated as 13μV_{rms}. This leads to a resolution of 10 bits.

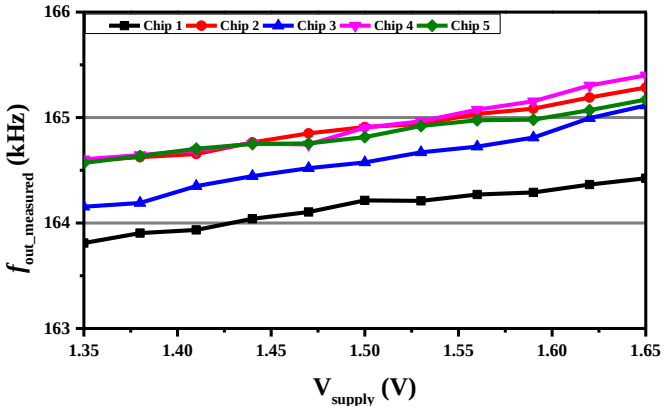


Fig. 8 Frequency variation of the VF converter against voltage supply variation

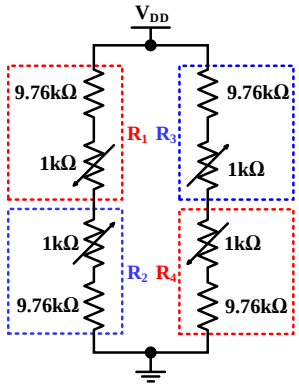


Fig. 9 Full Wheatstone bridge sensing configuration.

C. *Pressure Sensor Configuration*

The sensor interface is then tested with a full Wheatstone bridge based Honeywell pressure sensor NSC-DANN030PGUNV [22] to measure the pressure in a tank. A pump AS20W is used to inject and drain the air from this pressure tank. Fig. 12 shows the output of commercial pressure sensor. It has shown that the commercial sensor displays a sensitivity of 0.765 mV/psi and an offset voltage of -0.032 mV. Turning to the sensor interface in conjunction with the sensor, it yields a sensitivity of 1.269 kHz/psi with an offset frequency of 125.2 kHz.

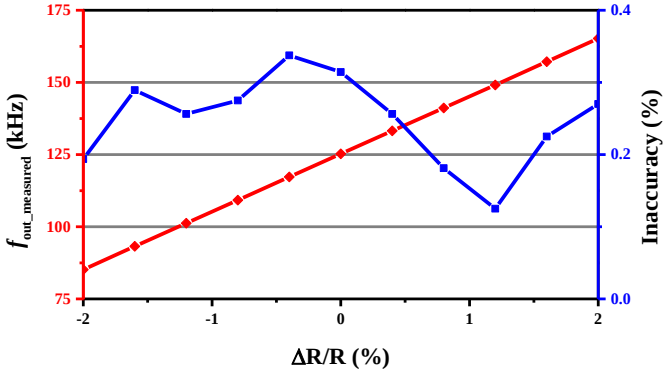
IV. Performance Comparison

Table II shows the performance comparison of the proposed VF converter with other representative frequency converters. With a power consumption of 112.5 μW and a measurement time of 1 ms, the proposed converter has demonstrated low energy-noise product while maintaining good accuracy across temperature variation and process variation. The proposed converter offers good linearity in comparison to other VF converters because the delay arising from the discharge of capacitor in the conventional IF conversion is eliminated. Three Figure-of-Merits, FOM_1 [23], FOM_2 and FOM_3, are adopted to evaluate the efficiency of VF converters. They are defined as follows:

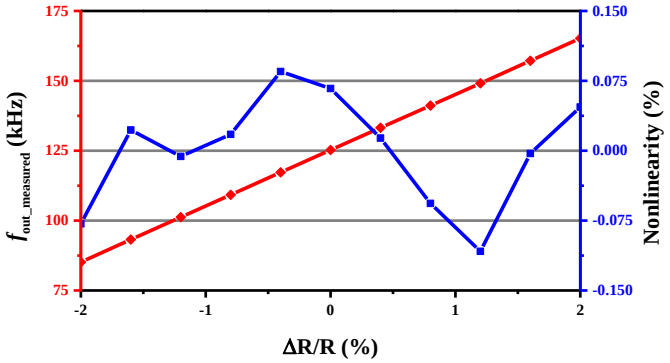
$$\mathrm{FOM}_1 = Power \times T_{measured} \times \frac{\sigma_f}{f_{\max} - f_{\min}} \tag{10}$$

$$\mathrm{FOM}_2 = Power \times T_{measured} \times \left(\frac{\sigma_f}{f_{\max} - f_{\min}} \right)^2 \tag{11}$$

$$\mathrm{FOM}_3 = \frac{Power \times T_{measured}}{ENOB} \tag{12}$$

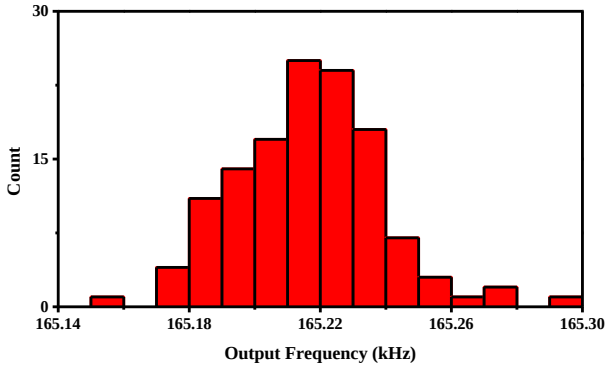


(a)

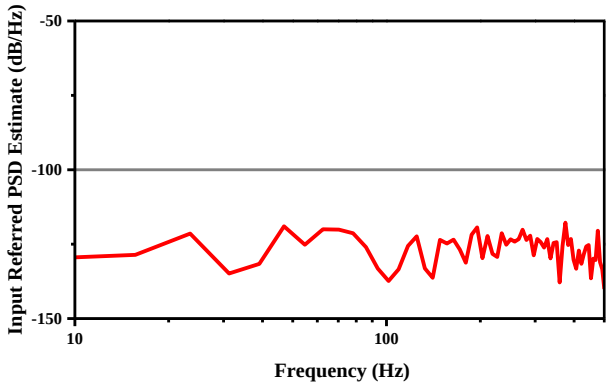


(b)

Fig. 10 Measured output frequency: (a) inaccuracy and (b) nonlinearity of the sensor interface in full Wheatstone bridge configuration.

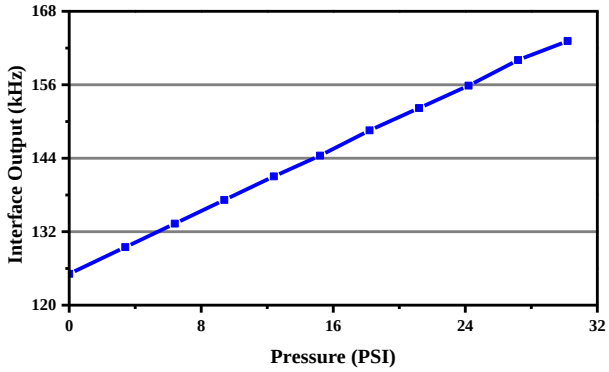


(a)

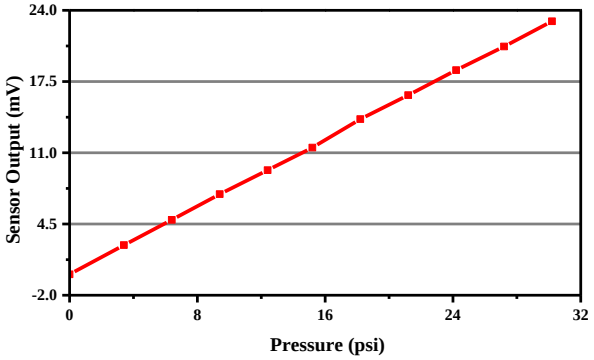


(b)

Fig. 11 (a)Output frequency distribution and (b) power spectral density of proposed sensor interface.



(a)



(b)

Fig. 12 Measured (a) output frequency of the sensor interface and (b) output voltage of the commercial pressure sensor.

Table II Performance comparison of the proposed converter with the reported works

Parameter	[8] TIM 1998	[10] TIM 2000	[28] TCAS II 2006	[11] Sens. Act., A 2007	[29] ETRI 2007	[12] TIM 2011	[13] Sensors J. 2013	[23] TIM 2015	[26] JSSC 2016	[27] ISSCC 2017	**This work**
Technology	Disc.	Disc.	0.25 µm CMOS	0.7 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	65 nm CMOS	0.18 µm CMOS	0.18 µm CMOS	**0.18 µm CMOS**
Supply (V)	3.3	±6.5	2.5	5	1.5	1.8	1.2	1.2	1.55	1.8	**1.5**
Input Range	±15mV*	5mΩ/Ω	0.1-0.8V	±0.025Ω/Ω	±0.01Ω/Ω	0-1.2V	0-1.2V	30n-60µA	±10mV###	±10mV	**±0.02 Ω/Ω**
Power (mW)	NA	81.3**	NA	67	0.270	0.375	0.080	0.168	2.42	2.16	**0.1125**
Sensitivity	NA	0.5 Hz/(µΩ/Ω)	520 kHz/V	60.4 Hz/1000ppm	5 µV/V/mmHg	861 kHz/V	750 kHz/V	41.5 Hz/nA	NA	NA	**199.9 Hz/(µΩ/Ω)**
Temp. Range (°C)	0 to 50	NA	NA	NA	NA	-20 to 120	−40 to 120	−30 to 80	NA	NA	**-40 to 80**
Nonlinearity (%)	0.186	±0.2#	±1#	±0.4#	0.23	0.4	0.009##	±0.6# | 11m##	NA	NA	**±0.11# | 1.75m##**
Timing Capacitor	External	External	Integrated	External	Integrated	Integrated	Integrated	Integrated	NA	NA	**Integrated**
σ_f (Hz)	NA	0.2	NA	0.3	NA	NA	NA	539	NA	NA	**22.35**
Freq. Range, Δf (Hz)	15-368k	10k±2.5k	52-416k	6.4k±1.51k	NA	0.1-1.1M	0.1M-1M	1.3k-2.489M	NA	NA	**85k-165k**
σ_f / Δf (µHz/Hz) or $(2\sqrt{2}\times SNR)^{-1}$(µV/V)	NA	40.0	NA	99.3	NA	NA	1411†	216	130	16.5	**279.4**
Conversion time (ms)	NA	10	NA	20	3.3	NA	32.8	16	50	0.5	**1**
FOM_1 (nJ)	NA	32.5**	NA	133.2	NA	NA	3.7†	0.71‡	1.57	8.9×10^{-3}	**31.4×10^{-3}**
FOM_2 (pJ)	NA	0.325**	NA	82.6	NA	NA	131†	0.95‡	2.05×10^{-2}	7.4×10^{-5}	**8.78×10^{-3}**
FOM_3(µJ/ENOB)	NA	63	NA	120	NA	0.34	0.26	NA	11	0.07	**0.01**

*Differential input voltage.
**Estimated.
#Maximum nonlinearity in % full scale.
##1-R^2 nonlinearity.
###Calculated based on full scale range/max IA gain.
†Estimated based on +5% $\Delta R/R$ in half bridge configuration.
‡ Bias current of 30µA for center frequency included.

where $T_{measured}$ = gate time, f_{max} = maximum output frequency, f_{min} = minimum output frequency, σ_f = maximum standard deviation of output frequency and ENOB is the number of effective bit of the interface. The lower the three FOM values, the better are the performances. From (11), the $\sigma_f/(f_{max}-f_{min})$ can be interpreted in an alternative representation as

$$\frac{\sigma_f}{f_{\max}-f_{\min}} \equiv \frac{1}{2\sqrt{2}(SNR)} \tag{13}$$

, where SNR is the signal-to-noise ratio. This is because f_{max}-f_{min} is equivalent to maximum output signal range and σ_f is equivalent to the rms output noise voltage. The FOM_1 is in similar form with Walden FOM [24] whereas FOM_2 is in similar form with thermal FOM [25].

FOM_3 is defined as the energy consumption per ENOB. It is mainly because IoT application deals with energy efficiency and hence FOM_3 is regarded as the critical evaluation parameter for performance comparison. From the comparison results, it can be seen that the proposed VF converter has achieved better FOM_1 and FOM_2 with respect to that of the reported works [10]–[13], [23], [26]. Besides, in comparison to the instrumentation amplifier with sigma-delta ADC sensor interface [27], despite the sensor interface displays relatively higher values in FOM_1 and FOM_2, the proposed circuit shows 7 times lower in the energy consumption per ENOB as interpreted from FOM_3 whilst offering reasonable good signal-to-noise ratio. Therefore, it is suitable for IoT applications.

V. Conclusion

A low-energy low-noise VF converter with reduced circuit sensitivity has been proposed. Through the SC tracking design in the novel circuit architecture that involves SC VI and IF conversion techniques, good output frequency accuracy across process, voltage and temperature variations is obtained. In addition, by incorporating the chopper stabilization technique to reduce the offsets and low-frequency noise arising from both the amplifier and comparator, the circuit's performance in terms of precision, noise and output signal frequency jitter effect is greatly improved. As a result, the proposed circuit has achieved the compromising good results from the three FOMs with respect to the reported works whilst offering a simple architectural solution.

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Kuan Chuang Koay (S15) was born in Malaysia. He received his B. Eng (Hons) degree from Nanyang Technological University (NTU), Singapore, in 2012. He joined Qualcomm, Singapore as an analog integrated circuit designer in 2017. His research interests include frequency compensation techniques for low-dropout regulators, design of switching regulator and design of sensor interface IC.

Pak Kwong Chan (M'92–SM'10) was born in Hong Kong. He received the B.Sc. (Hons) degree from University of Essex, Colchester, U. K., in 1987, the M.Sc. degree from University of Manchester, Institute of Science and Technology, Manchester, U.K., in 1988, and the PhD degree from University of Plymouth, U.K. in 1992. From 1989 to 1992, he was a Research Assistant with University of Plymouth, working in the area of MOS continuous-time filters. In 1993, he joined Institute of Microelectronics (IME), Singapore as a Member Technical Staff, where he designed high-performance analog/mixed-signal circuits for integrated systems and CMOS sensor interfaces for industrial applications. In 1996, He was a Staff Engineer with Motorola, Singapore where he developed the magnetic write channel for Motorola 1st generation hard-disk preamplifier. He joined Nanyang Technological University, Singapore in 1997, where he is an Associate Professor in the School of Electrical and Electronic Engineering. He served the Program Director (analog/mixed-signal IC and applications) for the Center for Integrated Circuits and Systems (CICS) from 2003 to 2010. He also conducted numerous IC design short courses to the industry and IC design centers. His current research interests include sensor circuits and systems, mixed-mode circuits and systems, PVT-insensitive circuits and systems, precision analog circuits, ultra-low-voltage low-power circuits as well as power management IC for integrated sensors, system-on-chip and internet-of-things applications. Dr Chan has served as a Guest Editor for the Journal of Circuits, Systems and Computers and for the Sensors.