

## 12.1 A 0.18 $\mu$ m High Dynamic Range NTSC/PAL Imaging System-on-Chip with Embedded DRAM Frame Buffer

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CMOS technology provides the capability to integrate a complete imaging system on a single chip [1,2], and to extend dynamic range [4,5,6]. A CMOS imaging system-on-chip is described that is programmable and capable of producing color video at up to 500 frames/s with over 100dB of dynamic range using multi-capture and sensitivity better than 3 lux. The chip incorporates an image sensor with pixel-level Multi-Capture Bit Serial (MCBS) ADC [6], a micro-control engine, and a full 4.9Mb frame buffer. The chip is fabricated in a 0.18 $\mu$ m CMOS Image Sensor Technology [3]. When paired with a companion image-processing chip, via a digital LVDS interface, the system produces standard NTSC or PAL video output.

A photomicrograph of the chip that highlights its major sections is shown in Fig. 12.1.1. The image sensor consists of a 742 x 554 pixel array coupled with a 10b DAC, control line drivers, and readout circuitry used for reference comparisons in the pixel-level ADCs. The array includes additional columns and rows for demosaicing calculations and subtraction of dark current and reset offset. The microcontrol logic executes instructions in dual microcode buffers pertaining to exposure time, region of interest, image capture details, data format, etc. and controls the array's reset, MCBS readout, result storage and initial processing of the pixel data for later demosaic and image processing. The chip contains a 4.9Mb frame buffer used to store intermediate results in multi-capture scenarios to extend dynamic range. The high dynamic range image is reconstructed from these multiple captures. A high dynamic range image captured using the chip is depicted in Fig. 12.1.2. The dynamic range exceeds 100dB and allows details from the printing on the illuminated incandescent bulb as well as the dimly lit Macbeth chart to be captured in the same image.

Illustrated in Fig. 12.1.3, the pixel circuit comprises an MCBS ADC multiplexed among each of the 2x2 neighboring pixels that make up a color filter array unit. Only two multiplexed inputs to the ADC are shown. To achieve the non-destructive readout required by multi-capture, each pixel has a front-end transistor, M1-M4, connected in series with a multiplexing switch transistor, M5-M8, as shown in Fig. 12.1.3. The reset transistors, M9-M12, for each of the four pixels, reset their respective photodiodes to the value of the RAMP voltage when the corresponding reset gate is held high. In this state, the first stage of the ADC is configured as a unity gain feedback amplifier that serves to cancel comparator offset voltage, reducing fixed pattern noise.

Pixel-level ADC allows for very high speed, digital readout of sensor data. To avoid large signal swings on the bitline and to achieve high readout speed, current readout is adopted. Figure 12.1.4 shows the column level current detection circuit. The bitline is connected to a Wilson current source in which the negative feedback pins the bitline to a constant voltage. The current,  $I$ , is small (4 $\mu$ a) and serves to bias the bitline voltage to a constant level. A current,  $2I$ , is subtracted and thus does not contribute to the integrated bitline current. Pre-discharge of inte-

gration capacitor C1 occurs at the beginning of each clock cycle and the sense amp then sits open waiting for bitline current to present itself anywhere within the 10ns cycle time. The integration capacitor holds the bitline current even after the word line goes low. This current is integrated on the capacitor, amplified through two stages of inversion and latched on the rising edge of the clock. This data is subsequently moved to the on chip frame buffer. This sense amp design eliminates the need for more complex timing and control signals.

The reference signal RAMP is produced for the entire array by the 10b DAC. Internal to the pixel, the RAMP is compared against the photodiode voltage, which is consequently digitized. A fast settling class AB output stage is used to satisfy the requirement of driving the large, capacitive pixel array load, on the order of 1nF. The DAC output value, offset, and gain are controlled by the microcontrol logic. A scope photo of the RAMP voltage generated by the DAC during image capture is shown in Fig. 12.1.5. The inset in the figure shows a detailed view of the settling time of the RAMP voltage driving the large capacitive load on chip and settling in approximately 40ns.

Figure 12.1.6 summarizes the significant characteristics of the sensor and Fig. 12.1.7 describes the important characteristics of the system.

The integration of a sensor with pixel-level ADCs, a microcode engine, frame buffer, and logic allows for an adaptive, flexible, high-quality imaging system that is designed and manufactured with minimal additional components. The imaging system can automatically optimize its exposure controls based on light level and motion characteristics for highest dynamic range and best picture quality. Great care is taken to ensure clean analog performance while supporting high-speed digital logic and I/O signaling. The flexibility of this architecture allows enhanced image quality and performance through firmware, and allows for easy extension into numerous derivative products.

### Acknowledgements

The authors express their gratitude to TSMC for fabricating the design and to MoSys for the integrated 1T-SRAM<sup>®</sup>.

### References

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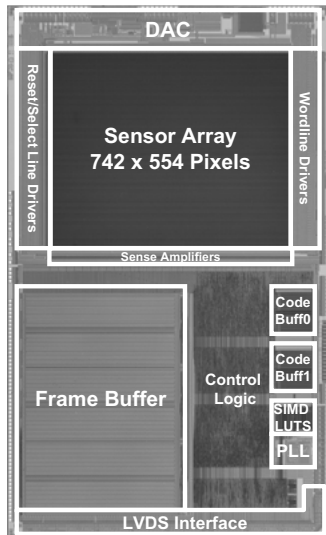


Figure 12.1.1: Chip micrograph.



Figure 12.1.2: High dynamic range image.

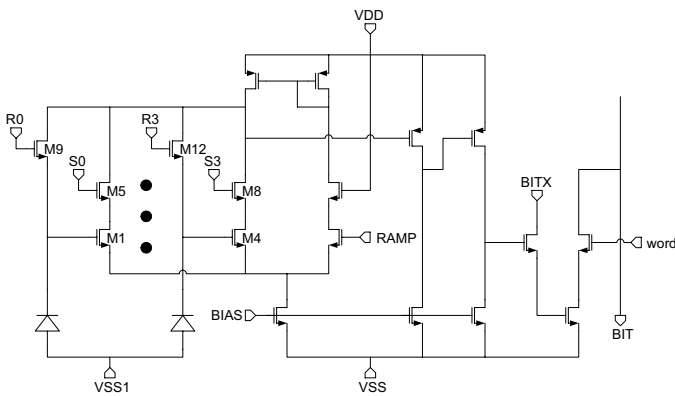


Figure 12.1.3: Pixel schematic.

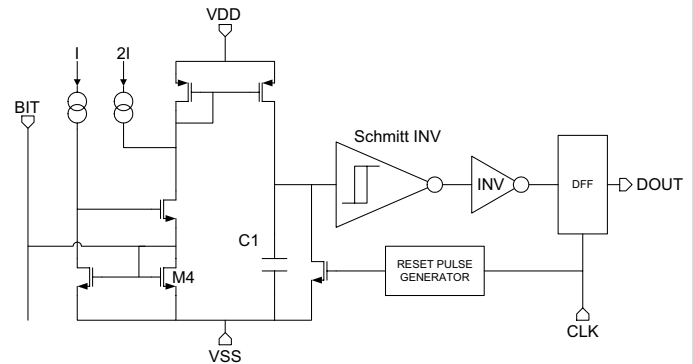


Figure 12.1.4: Column readout circuit.

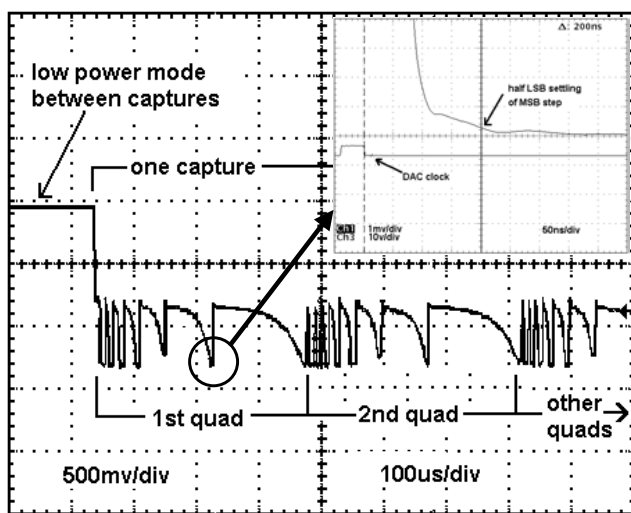


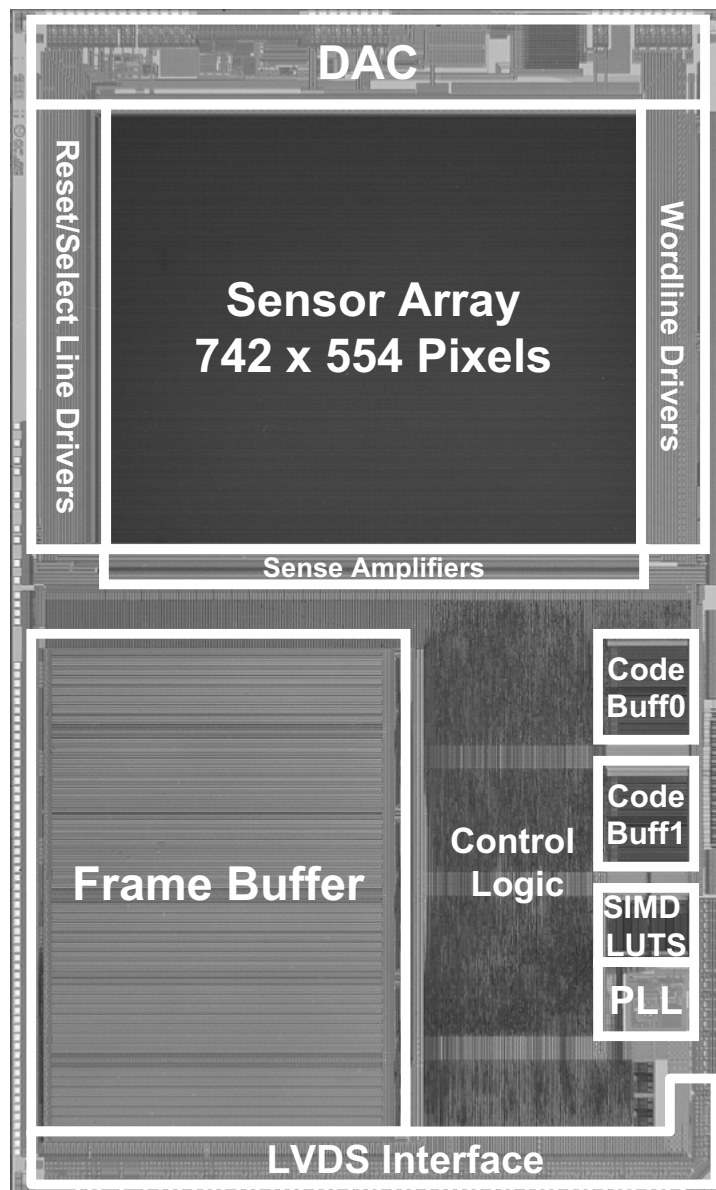
Figure 12.1.5: Ramp signal during image capture.

Technology	0.18 $\mu$ m 1P4M CMOS
Sensor Size	742 x 554 pixels
Pixel Size	7 $\mu$ m x 7 $\mu$ m
Transistors/pixel	6
Fill Factor	>42% (70% with ulens)
Photodetector	n-well to p-sub diode
Quantum Efficiency (550nm)	48% (no CFA/ulens)
Dark Current	<1nA/cm <sup>2</sup>
SNR	>45dB
Dynamic Range	>100 dB
Frame Rate	500 fps

Figure 12.1.6: Image sensor characteristics.

<b>ADC</b>	<b>10b MCBS</b>
<b>Signal Swing</b>	<b>.5V</b>
<b>Package</b>	<b>181 pin PBGA</b>
<b>Supply Voltage</b>	<b>1.8V Core, 3.3V I/O</b>
<b>Power Consumption at 30 fps</b>	<b>500mW total 40mW sensor only</b>
<b>LVDS interface</b>	<b>200Mhz DDR</b>
<b>System clock speed</b>	<b>100Mhz</b>
<b>Die area</b>	<b>6.8mm x 10.7mm</b>

Figure 12.1.7: Image system characteristics.



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**Figure 12.1.2: High dynamic range image.**



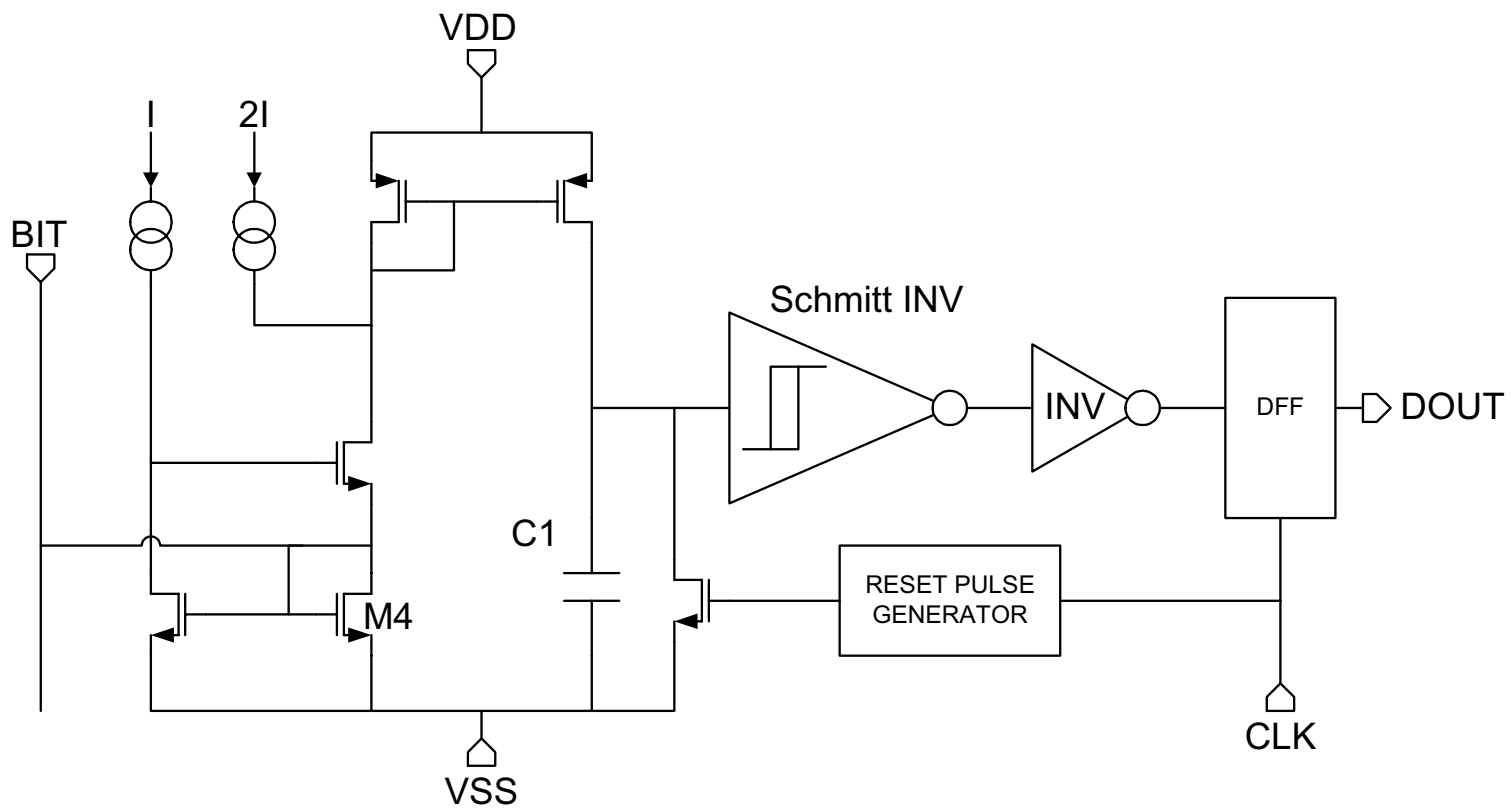


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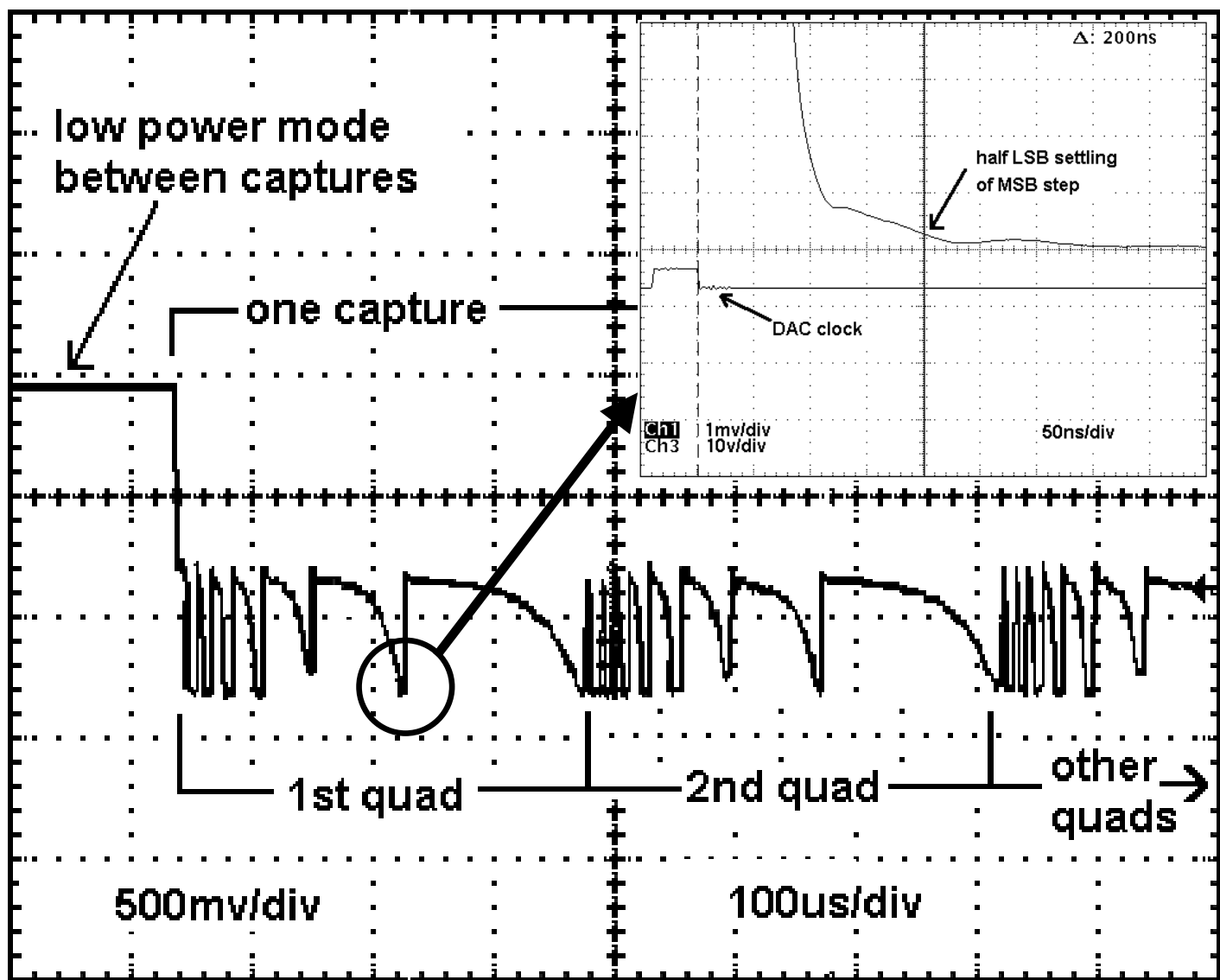


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<b>Fill Factor</b>	<b>&gt;42% (70% with ulens)</b>
<b>Photodetector</b>	<b>n-well to p-sub diode</b>
<b>Quantum Efficiency (550nm)</b>	<b>48% (no CFA/ulens)</b>
<b>Dark Current</b>	<b>&lt;1nA/cm<sup>2</sup></b>
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