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6.2 A 0.18µm CMOS 802.15.4a UWB Transceiver for Communication and Localization

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Recently, IEEE 802.15.4a has specified a UWB PHY for low-rate commutation with ranging capability for wireless personnel area and sensor network applications [1]. Related work is reported on low-rate energy-efficient UWB radios [2-4]. However, they are not fully standard compliant or localization enabled. 802.15.4a supports three bands of operation, i.e., sub-1GHz band (249.6 to 749.6MHz), low band (3.1 to 4.8GHz) and high band (6.0 to 10.6GHz) with 16 channels in total. A combination of the burst position modulation (BPM) and binary phase shift keying (BPSK) is adopted. With different coding rate, bursts per symbol, and chips per burst, the mean pulse repetition rate (PRF) could vary from 3.9 to 62.4MHz for data throughput of 120kHz to 31.2MHz. This work presents an UWB RF transceiver which supports 12 channels, variable date rate, and ranging capability as specified in IEEE802.15.4a.

Figure 6.2.1 shows the RF transceiver architecture. On the TX side, the digital clock (TX_clk) triggers a baseband pulse-shaping filter (BPSF). The output pulses are modulated by the TX binary data. The signal is then upconverted by a mixer and amplified by a driver amplifier (DA) prior to the antenna. On the RX side, the weak signal is amplified by an LNA, is downconverted by I/Q mixers and is low-pass filtered to recover the phase of the transmitted BPSK signals. A VGA, in each I and Q path, is then used to boost the signal level. The output of each VGA is used in two paths. In one path it is connected to an integrator followed by an ADC for recovering the digital data while in the other path it goes through a signal detector (squarers and a limiting amplifier) to recover a clock (denoted as RC_clk). The delay time between the rising edge of RC_clk and that of TX_clk are extracted through a digital edge detector. The low-pass filtered output is thus precisely proportional to the delay and can be used for ranging calculation in baseband. The muti-tone frequency generator produces I/Q LOs. Typically, the duration of UWB pulses occupies a small duty cycle (<5%) allowing TX or RX to be powered down accordingly whenever there is no pulse transmission.

The transmitter circuits are shown in Fig. 6.2.2. The BPSF consists of a cascade of a 1st-order and a biquad G_m-C filter with proper pole-zero placements to generate channel-mask-compliant pulses. Four switches, controlled by modulation data, change the polarity of the pulses. The upconvertor is a Gilbert-cell active mixer optimized for high linearity and is resistively loaded to cover the full UWB band. The mixer achieves a conversion gain of –9.6dB, IIP3 of 15.2dBm, NF of 15.4dB. The differential DA is a switched Class-A amplifier in order to preserve the constrained spectral and improve the efficiency. M3/4 and M5/6 allow DA to be turned off when no pulse is being transmitted. The complementary control inputs (Cr/Crb) are slightly delayed from each other to prevent undesired pulse generation by Ll/L2 during fast transitions of the control signals. The input transistors M1/M2 use resistive feedback to improve their bandwidth. The DA achieves a gain of 6 to 8dB, a BW of 6GHz (3 to 9GHz), and maximum output power of 8dBm. The TX draws a peak current of 8mA when generating 500MHz PRF pulses.

Two measured pulse sequences at two mandatory channels and their spectrum are demonstrated in Fig. 6.2.3. For low-band mandatory Channel 3, the generated BPSK pulses are of 2ns width and the PSD spectrum of the transmitted signal complies with both the FCC-band mask and channel mask. Similarly, a pulse sequence generated in the high-band mandatory Channel 9 and its PSD spectrum are also shown.

The RX front-end circuits are shown in Fig. 6.2.4. The LNA is designed to operate at one channel at any given time, through band switching and channel selection, to minimize power consumption. The capacitive cross-coupled input stage is used to boost the G_m of the stage, and reduce input-referred noise while achieving good input matching. The band switching between low and high band can be done by transistors M3/M4 and M5/M6. Within each band, there are two-stage cascaded amplifiers. The first stage is an LC-tuned load where a capacitor bank is used to tune to the desired channel. The second stage is a common-source amplifier with an LC-tunable loading network. A double-balanced differential Gilbert cell is used as the mixer and its resistive loads are used to cover the entire UWB band. The combined RF front-end achieves a voltage gain of 30.4/21.3dB, an NF of 5.5/7dB, and an IIP3 of –16.7/–10.7dB for low and high bands, respectively.

The RX LPF is implemented by a 3rd-order elliptical G_m-C filter with cut-off frequency of 250MHz. The five-stage cascaded dB-linear VGA achieves a dynamic gain from –20 to 50dB with 400MHz BW. The variable BW integrator captures the reflected pulses from multipath and extends the duration of the demodulated pulses. For localization purpose, two squarers and one nonlinear low-pass filter (NLPF) [5] are used to regenerate RC_clk, where the squarers are used to detect the signal energy and NLPF is used to boost signal level to rail-to-rail. Through the edge detector, a digital pulse train is turned on and off at the rising edge of TX_clk and RC_clk, respectively. A passive 5th-order RC LPF with cut-off frequency of 500kHz is applied to average the jitter and noise and hence to significantly improve the ranging accuracy. Operating at 500MHz PRF, the peak current of the RX is 31mA.

A nine-tone frequency generator is shown in Fig. 6.2.5. A digital frequency-tuning loop is used to lock the quadrature VCO (QVCO) output frequency to an external 15.6MHz crystal reference. Once the QVCO is tuned to the desired channel, as determined by the lock detector, the tuning loop is powered off. The VCO tuning voltage is stored as a digital word in an 11b latch, where 3 bits are used for coarse tuning and the 8b DAC output is used for fine tuning. The accuracy of frequency tuning is <10MHz, which is limited by DAC resolution. To significantly reduce the die size, a four-stage ring oscillator with a frequency doubler is used as the QVCO core. The ring oscillator generates 45°/90° phase difference LOs covering 2.8 to 4.75GHz, and the frequency doubler generates quadrature LOs covering 5.6 to 9GHz. The measured QVCO start-up time is 5.39ns, and has a phase noise of –90dBc/Hz at 1MHz offset for 4.5GHz LO with output power of –2.1dBm. The peak current is 40mA.

The transceiver IC is implemented in a 0.18µm CMOS technology. The chips are housed in a QFN48 package and mounted on Rogers PCB for evaluation. A transmitted data pattern (at the TX input), received pulse pattern (at the RX input), and demodulated data pattern (at the integrator output) are shown in Fig. 6.2.6. Also a measured ranging result is illustrated where the measured time delay is 14.9ns which corresponds to the ranging distance of 223.5cm. Furthermore, the system can achieve 0.2ns resolution which translates to two-way ranging accuracy of 3cm [1]. The transceiver performance is summarized in Fig. 6.2.6. Targeting low-cost and high-energy-efficiency implementation, it achieves 0.74nJ/pulse for TX and 6.5nJ/pulse for RX while occupying 4.5mm² of die area. The chip micrograph is shown in Fig. 6.2.7.

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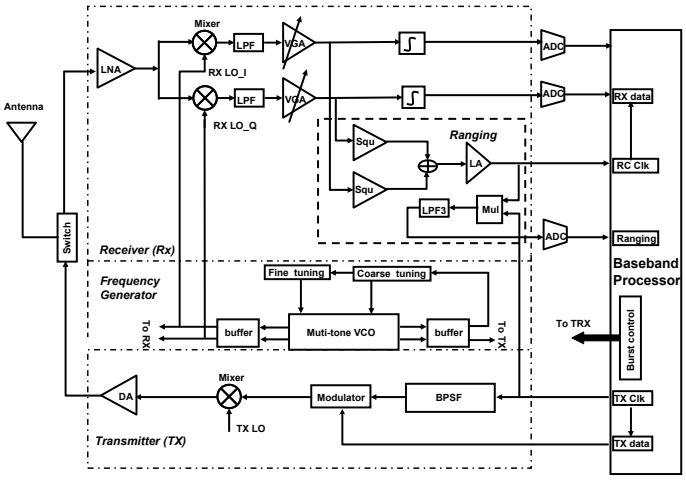

Figure 6.2.1: 802.15.4a BPM-BPSK UWB Transceiver System Architecture.

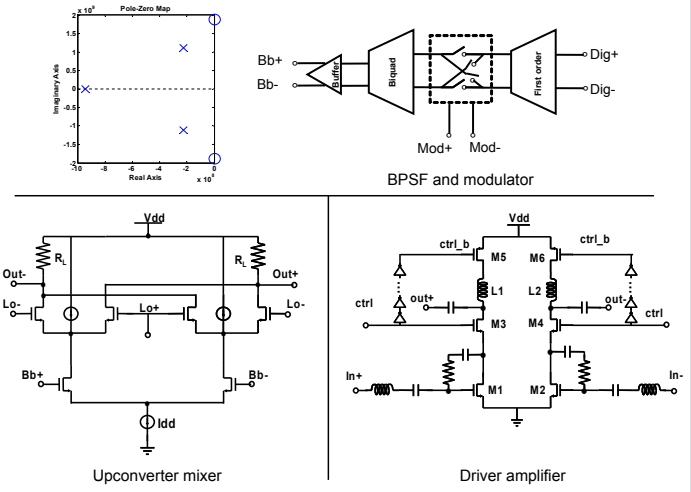

Figure 6.2.2: Transmitter circuits.

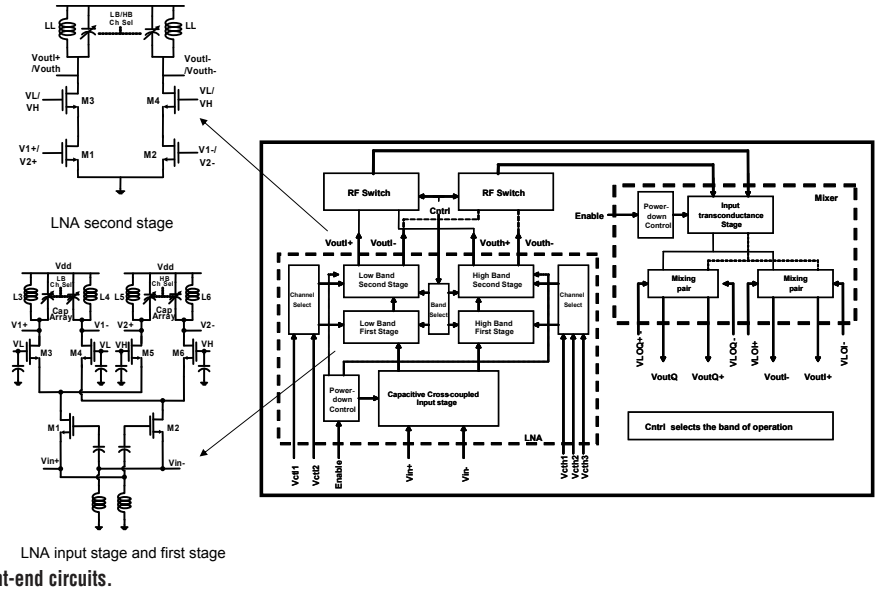

Figure 6.2.4: Multi-channel front-end circuits.

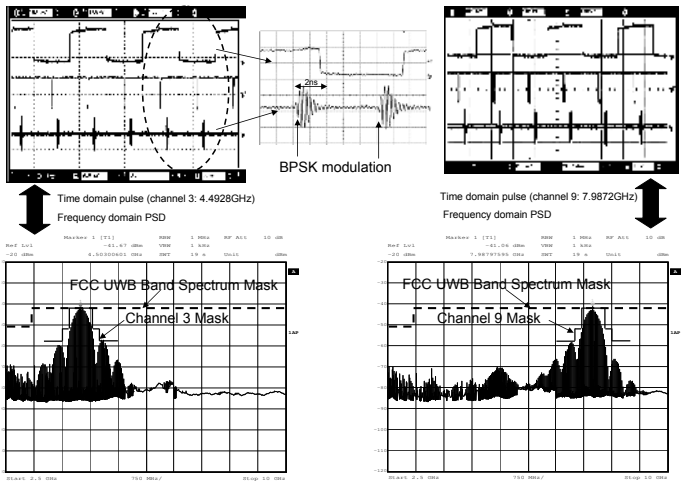

Figure 6.2.3: Measured transmitted pulses and their spectra.

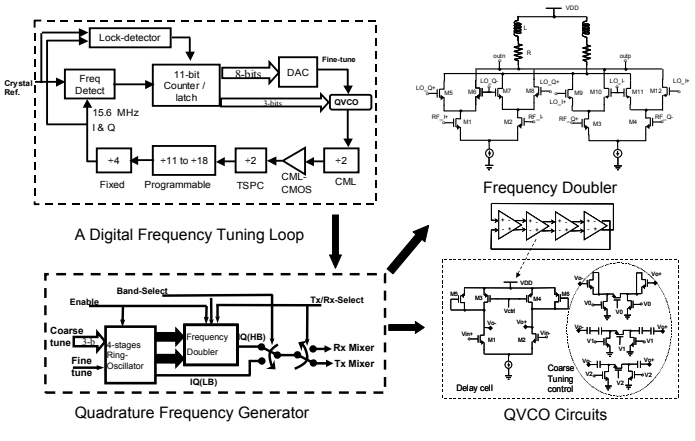

Figure 6.2.5: Multi-tone frequency generator.

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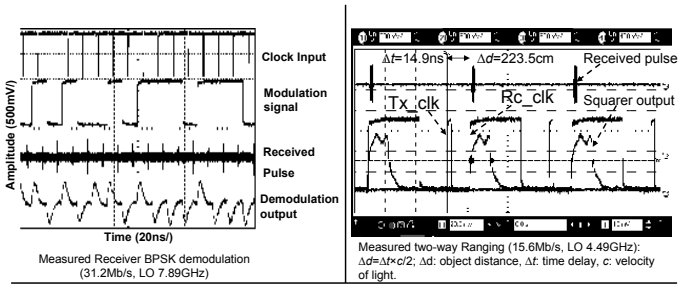

Measured Receiver BPSK demodulation (31.2Mb/s, LO 7.89GHz)

Measured two-way Ranging (15.6Mb/s, LO 4.49GHz): $\Delta d=\Delta t \times c/2$; Δd: object distance, Δt: time delay, c: velocity of light.

Transmitter		Receiver		Overall	
Peak PRF:	499.2/1000MHz	Receiver gain (LB/HB):	80/90dB	VDD:	1.8V(can be as low as 1V)
Modulation:	BPM-BPSK	Noise Figure (LB/HB):	8.2/9.4dB	Technology:	0.18μm CMOS
BW:	499.2/1331.2MHz	Sensitivity (LB/HB):	−75/−70dBm	Freq. generator:	Ring QVCO based
Energy/pulse:	0.74nJ/p@1.8V	IIP3:	−12/−8dBm	Freq range:	3 to 9GHz/12 channels
Pulse duration:	2/1ns	Energy/pulse:	6.51nJ/p@1.8V	Ranging accuracy:	3cm
Start-up time:	6.9ns	Start-up time:	25.5ns	Die size (die size):	4.5mm²

Figure 6.2.6: Measured transceiver performance.

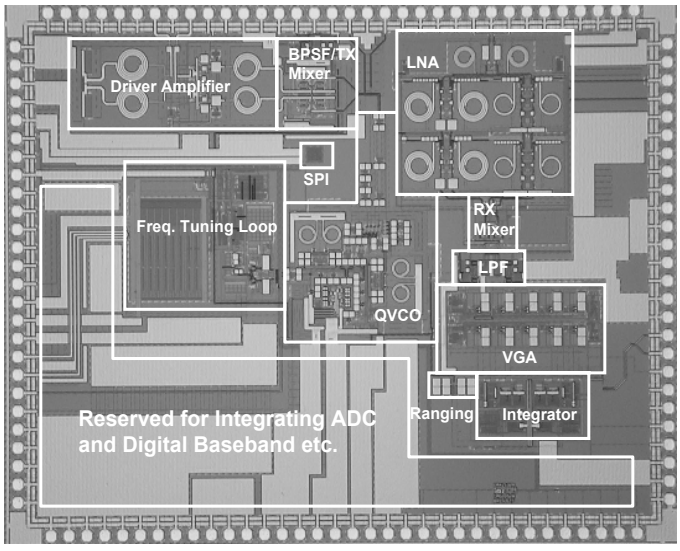

Figure 6.2.7: TRX chip micrograph.

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