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# A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving ⩾11dBm IIP3 and ⩽6.5 dB NF — Source link

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## 12.4 A 0.2-to-2.0GHz 65nm CMOS Receiver Without LNA Achieving >11dBm IIP3 and <6.5 dB NF

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Spurious-free dynamic range (SFDR) is a key specification of radio receivers and spectrum analyzers, characterizing the maximum distance between signal and noise+distortion. SFDR is limited by the linearity (intercept point IIP3 mostly, sometimes IIP2) and the noise floor. As receivers already have low noise figure (NF) there is more room for improving the SFDR by increasing the linearity. As there is a strong relation between distortion and voltage swing, it is challenging to maintain or even improve linearity intercept points in future CMOS processes with lower supply voltages. Circuits can be linearized with feedback but loop gain at RF is limited [1]. Moreover, after LNA gain, mixer linearity becomes even tougher. If the amplification is postponed to IF, much more loop gain is available to linearize the amplifier. This paper proposes such an LNA-less mixer-first receiver. By careful analysis and optimization of a passive mixer core [2,3] for low conversion loss and low noise folding it is shown that it is possible to realize IIP3>11dBm and NF<6.5dB, i.e. a remarkably high SFDR>79dB in 1MHz bandwidth over a decade of RF frequencies.

High linearity is offered by passive mixers, but at the cost of conversion loss. In Fig. 12.4.1 a passive switching mixer and sampling mixer are compared (ideal switches are assumed), with conversion gain and NF shown. The switching mixer switches between the input signal and ground, effectively multiplying the rectangular clock with the input. As a consequence, a lossless 50% duty cycle switching mixer already has 6.9dB of conversion loss, severely boosting the NF of the stage after the mixer. The sampling mixer filters the input with the resistor-capacitor when the switch is closed and holds the output voltage on the capacitor when the switch is opened, resulting in a much lower conversion loss, since the signal does not return to zero. By balancing the switching mixer the NF is reduced to 3.9dB due to even-order cancellation. An amateur-radio application [2] and low-power transceiver design [3] have shown that the Quadrature Sampling Mixer (QSM)- also shown in Fig. 12.4.1- provides *image rejection* as well as even-order cancellation, with a maximum 25% duty cycle to avoid overlap between the switches. Compared to the 3.9dB NF of the balanced switching mixer, a 25% duty cycle QSM offers a much lower NF of 0.9dB and a conversion loss of only 0.9dB. In this case the effective resistance as seen by the capacitor is 4-times increased. This places a pole at the mixer output at one-fourth of the RC cutoff frequency, thus by choosing the value of C the mixer bandwidth can be set to the desired value.

Figure 12.4.2 shows the proposed direct-conversion architecture including a *double*-balanced QSM driven by an on-chip clock divider generating the four clock phases. The clock divider consists of transmission gates and inverters driven by an off-chip generator with 4-times higher clock frequency. A completely differential design cancels out second-order distortions, ensuring that third-order harmonics dominate the linearity performance. The resistance for the QSM consists of the 5Ω switch on-resistance added to the 50Ω source impedance. The switch resistance increases the mixer NF to 1.9dB and limits the IIP3 to +26dBm.

Figure 12.4.3 shows the feedback amplifier. The NMOS transistor with current-source load provides most of the loop gain. It is followed by a PMOS common-source stage driving the resistive feedback network with feedback to the source of the NMOS. The 4-to-1 ratio in the feedback network results in a 13.5dB voltage gain and transistor sizes result in a 3dB amplifier NF. The simulated loop gain shown in Fig. 12.4.3 is about 32dB and rolls off to 29dB at 9MHz. The decreasing loop gain diminishes the linearizing effect of the feedback at higher IF frequencies, resulting in a lower IIP3 for out-of-band interferers. This effect is compensated by the increasing conversion loss of the mixer (the mixer bandwidth is set to 25MHz with C=64pF) for higher IF frequencies, resulting in a minimum system IIP3 of +12.5dBm. In this proof-of-concept design the amplifier is kept simple and its IIP3 is still dominant for the system linearity. As the IIP3 of the passive mixer is +26dBm, there seems to be room for improving the IIP3 yet another 13dBm.

The circuit is fabricated in a standard 65nm LP CMOS technology. Figure 12.4.7 shows a die micrograph, die size is 0.95×1.1mm$^2$. Measurements are performed with wafer-probing and a hybrid for wideband single-to-differential conversion. The incident voltage wave generated by the source $V_S$ is fed into the Δ port of the hybrid, which outputs an in-phase voltage wave at the 0° output and an inverted voltage wave at the 180° output. The voltage swing on both the 0° and 180° outputs is 3dB lower than the voltage swing on the Δ port and the output ports are in anti-phase. Therefore the *differential* voltage wave between the ports is 3dB *higher* than the voltage swing on the Δ port. The voltage waves after the hybrid travel to IN+ and IN- where they are fully reflected by the high input impedance of the receiver. The incident and reflected voltage waves are in phase and the resulting voltage swing between IN+ and IN- is therefore doubled [4]. The hybrid combined with the high input impedance result in an effective voltage gain in front of the mixer of 9dB. The equipment for combining the I and Q outputs and performing image rejection was not available. For a direct-conversion receiver with the mixer first in the receiver chain the DSB NF is equal to the SSB NF with image rejection, so DSB NF measurements were performed on a single I or Q output alone. Gain and IIP3 (50kHz tone spacing) are also measured on a single I or Q output. Figure 12.4.4 shows the measured performance figures at different IF frequencies and an RF frequency of 500MHz as markers, while the simulated figures are shown as lines. The measured voltage conversion gain rolls off from 22dB to 20.5dB due to the mixer IF pole. The NF is lower than 6.5dB and increases at lower IF frequencies due to flicker noise of the amplifiers and at higher IF frequencies due to a decrease in gain. The measured minimum IIP3 is +11dBm. Figure 12.4.5 shows the measured performance figures at different RF frequencies and an IF frequency of 5MHz as markers, while the simulated figures are shown as lines. The clock divider limits the RF frequency to 2GHz. The phase mismatch between outputs was measured to below 2 degrees. LO radiation occurs at the input at multiples of the clock frequency with a maximum level of -65dBm. The clock divider consumes 7mW and the mixer plus amplifiers consume 60mW from a 1.2V supply.

Figure 12.4.6 compares the measured parameters with two other state-of-the-art wideband receivers [1,5] and a commercially available spectrum analyzer [6]. Indeed, the SFDR is about 8dB better than for other CMOS chips and even in the range of expensive test equipment.

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[6] Tektronix RSA2200A Real-Time Spectrum Analyzer Data Sheet.

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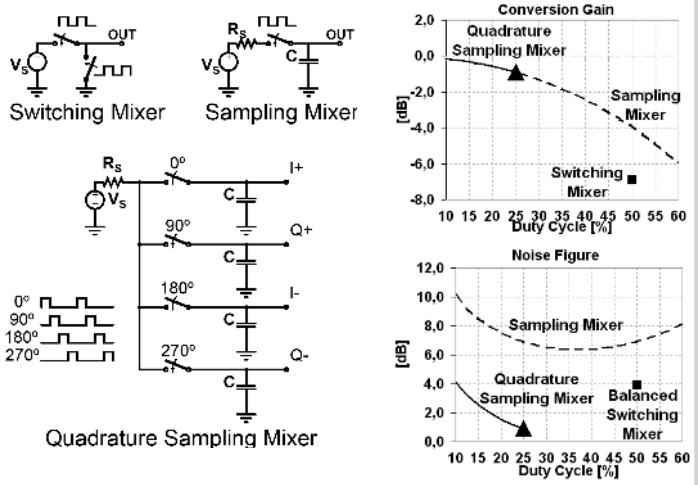


Figure 12.4.1: Switching mixer and sampling mixer.

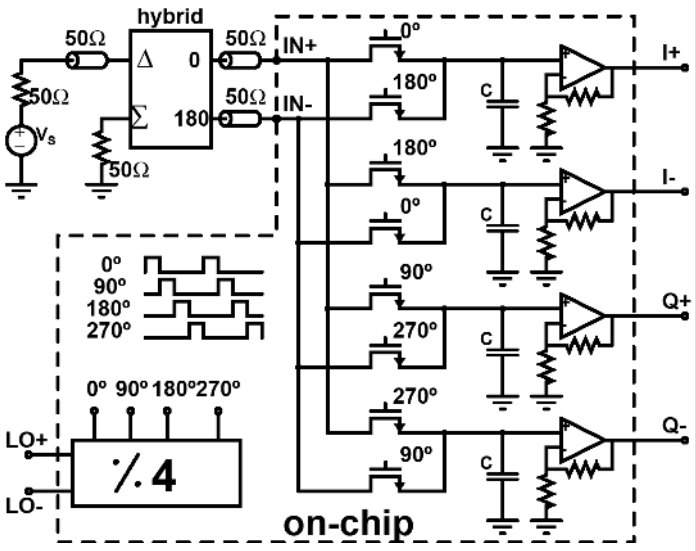


Figure 12.4.2: Direct conversion receiver architecture.

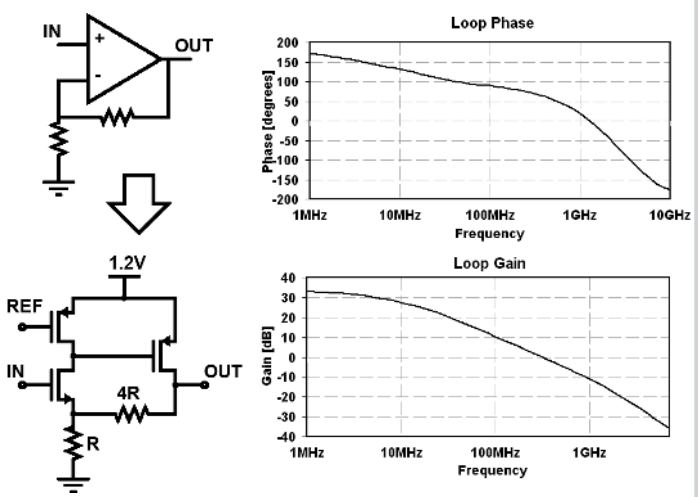


Figure 12.4.3: Negative feedback amplifier with simulated loop gain and loop phase.

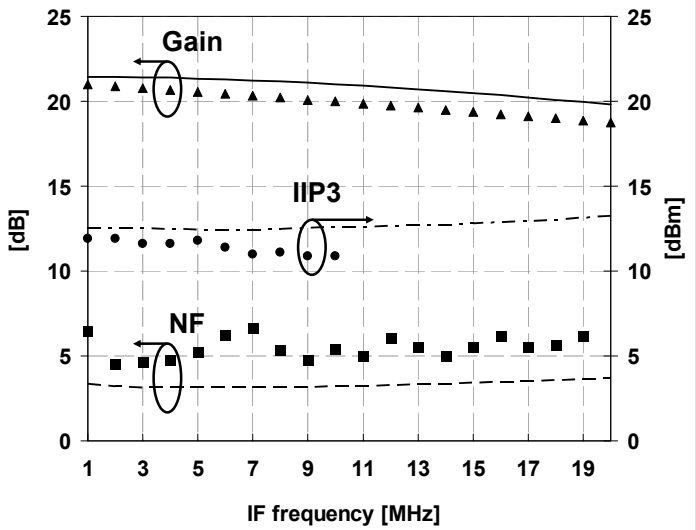


Figure 12.4.4: Gain, NF and IIP3 versus IF frequency, fixed 500MHz RF frequency, single I or Q output (lines are simulations, markers are measurements).

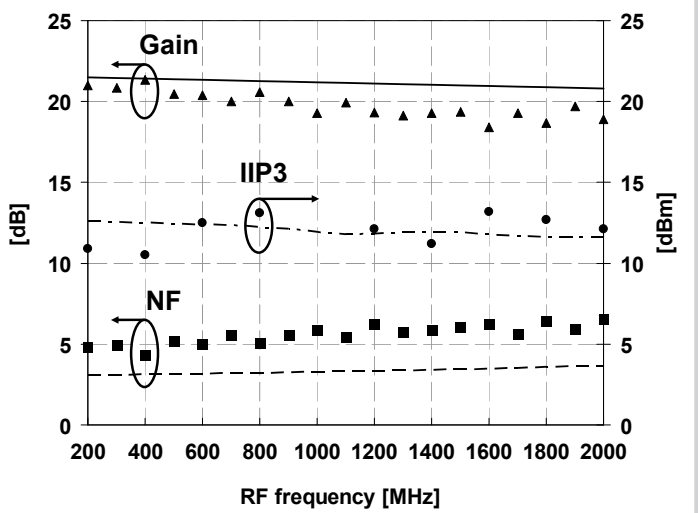


Figure 12.4.5: Gain, NF and IIP3 versus RF frequency, fixed 5MHz IF frequency, single I or Q output (lines are simulations, markers are measurements).

| | This Work | [5] | [1] | Tektronix RSA2200A [6] | |
|---|---|---|---|---|---|
| RF Frequency | 0.2 - 2.0 | 0.8 - 6 | 0.6 - 10 | 0 - 3 | GHz |
| IF -3dB Bandwidth | 25 | 20 | 264 | ~10 | MHz |
| Gain | 19 | 20 | 14 | | dB |
| DSB NF | 6.5 | 5 | 7 | 24 | dB |
| IIP3 | +11 | -4 | 0 | +30 | dBm |
| IIP2 | +65 | +60 | +20 | | dBm |
| SFDR | 79 | 70 | 71 | 80 | dB |
| Power Dissipation | 67 | 60 | 90 | | mW |
| Supply Voltage | 1.2 | 2.5 | 1.2 | | V |
| Active Area | < 0.13 | 3.8[1] | < 0.2 | | $mm^2$ |
| Technology | 65nm | 90nm | 45nm | | CMOS |

[1] Includes synthesizer and baseband filters

Figure 12.4.6: Comparison to other designs.

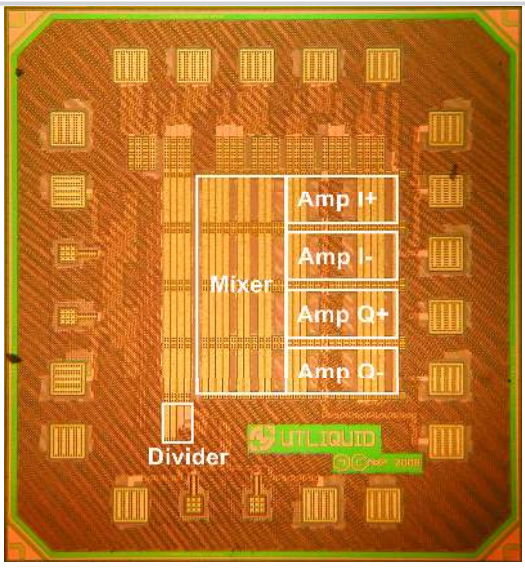


Figure 12.4.7: Chip micrograph.


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