A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS

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***Abstract*—We present a 0.2-V open-loop voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC) intended for IoT wireless sensor nodes. A resistor-based frequency-tuning scheme helps in mitigating odd-order harmonic distortion induced by the VCO nonlinear transfer characteristic. It also provides a reconfigurable input range, allowing it to exceed the supply by 2.5× (single-ended), and maintaining tolerance against ±10% supply variations. Latch, flip-flops, and logic gates within the frequency-to-digital converter are designed for minimum propagation delays, allowing sampling at 30 MS/s. The ADC is implemented in 28-nm CMOS and achieves a peak SNDR of 68 dB, equivalent to an ENOB of 11, over a 61-kHz bandwidth with a 1-V_{pp} input differential sinewave. It consumes 7 μW, resulting in a state-of-the-art Walden and Schreier FoM of 27.8 fJ/c-s and 167.4 dB, respectively.**

***Index Terms*—0.2 V, analog-to-digital converter (ADC), deep-subthreshold, IoT, nonlinear, quantization (Q)-noise, ultralow voltage (ULV), voltage-controlled oscillator (VCO)-based ADC.**

I. Introduction

Analog-to-digital converters (ADCs) that are capable of operating at a low supply voltage can support wider range of energy sources (e.g., harvesters) in IoT wireless sensor networks. Voltage-controlled oscillator (VCO)-based ADCs are suitable candidates for ultralow voltage (ULV) operation as they are amenable to deep CMOS scaling thanks to their digitally intensive nature and time-domain operation (i.e., VCO phase quantization), in addition to their inherent first-order quantization noise shaping. However, they are severely impaired by the highly nonlinear *V-to-f* tuning curve of the ring VCO (RVCO), which considerably limits the maximum achievable resolution. Such issue has been addressed both from an architectural perspective and leveraging on intensive digital calibration [1]. Closed-loop, multistage, phase-domain, hybrid, and nonuniform sampling architectures [1]–[5] all proved to be effective solutions, despite often entailing an increased system complexity and power consumption, as well as embedding operational amplifiers and current sources, thus rendering them quite analog-intensive.

VCO-based ADCs have demonstrated proper functionality in weak inversion at an ultralow 0.2-V supply [6], [7]. Although preferable in terms of power consumption, a low sampling rate results in a low dynamic range (DR) for a given signal bandwidth. Multibit phase quantization is a way of increasing the signal-to-quantization noise ratio (SQNR), although it requires the use of a digital counter, whose critical path comprises several cascaded full-adders and would therefore exhibit an excessively long propagation delay at 0.2 V, violating setup-time of the following digital processor. Furthermore, a multibit topology is more sensitive to mismatches of the RVCO delay cells and to the offset of phase samplers [e.g., sense-amplifier flip-flops of an XOR-based frequency-to-digital converter (FDC) [2]], both causing nonuniformly distributed phase quantization levels. Such mismatches, more severe in weak inversion, impact the ADC noise floor. This letter presents a single-bit deep-subthreshold open-loop VCO-based ADC operating at 30 MS/s under a 200-mV nominal supply, yielding peak ENOB of 11. The tenfold increase in sampling rate compared to [6] and [7] extends the ADC input bandwidth and reduces in-band quantization (Q)-noise. Single-bit operation enhances immunity from device mismatches and minimizes system complexity and power. The RVCO nonlinearity is mitigated through a mixed voltage/current-mode tuning technique [8] while providing tolerance versus 20% variations in nominal supply. Furthermore, to accommodate diverse input and DR requirements of multiplexed sensor arrays, the resistor network allows the input range to be reconfigured, with a single-ended maximum voltage from 0.2 V up to 0.5 V.

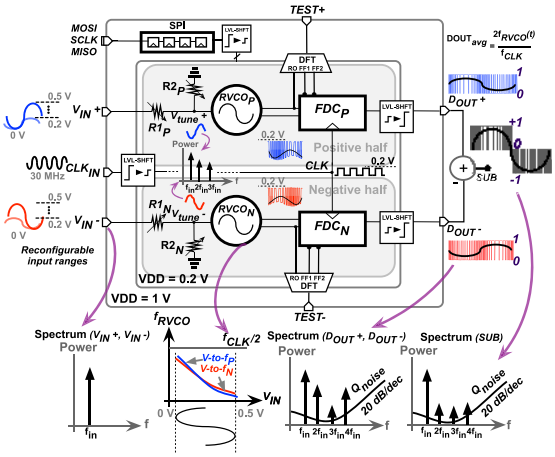

Fig. 1. VCO-based ADC architecture.

II. 0.2-V VCO-Based ADC Architecture

Fig. 1 shows the architecture of the proposed subthreshold VCO-based ADC. The ADC core is split into two complementary halves, yielding a pseudo-differential configuration (labeled as *positive* and *negative half*), each of which embeds the R_1/R_2 input resistive tuning network, RVCO and FDC. Peripheral circuitry, such as input clock buffer, serial-to-parallel interface (SPI), and design-for-testability circuits [(DFTs), mainly multiplexers], operates at 1 V. All of the signals interfacing between the 1-V and 0.2-V domains are level-shifted. The input signal V_{IN} (either $V_{IN}+$ or $V_{IN}-$) directly connects to the resistive network producing V_{tune} according to

$$V_{tune} = \frac{R_2||R_{NL}(V_{tune})}{R_1 + R_2||R_{NL}(V_{tune})} \cdot V_{IN} \quad (1)$$

where $R_{NL}(V_{tune})$ is a nonlinear impedance which models the current flowing into the input resistive network from the RVCO (thus also dependent on V_{tune}). Differently from [8], resistors R_1 and R_2 are

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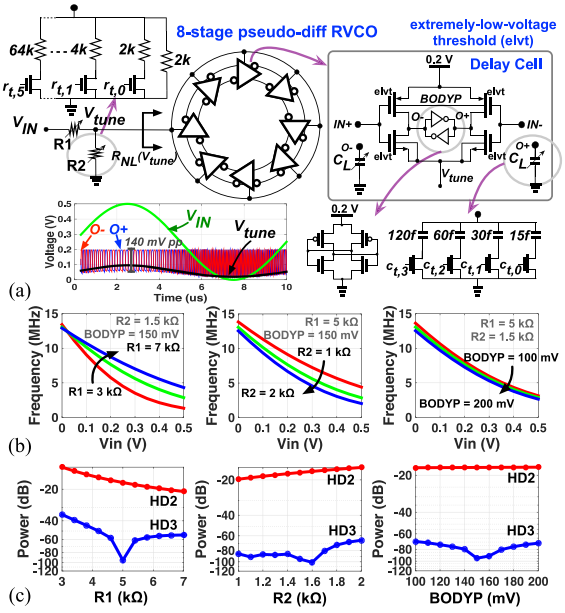

Fig. 2. (a) RVCO implementation, (b) simulated *V-to-f* transfer characteristic versus R_1, R_2, and bulk voltage BODYP of pMOS transistors, and (c) associated second- and third-order HD.

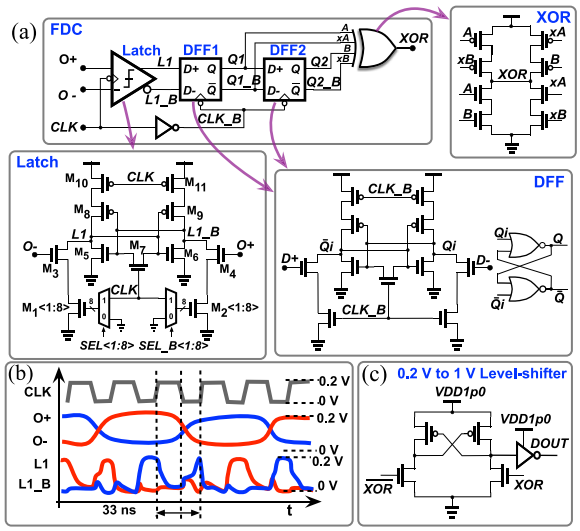

Fig. 3. (a) FDC implementation, (b) timing diagram of the sampling latch signals, and (c) output voltage level-shifter.

programmable so as to accommodate process and voltage variations, more severe in deep-subthreshold. Indeed, appropriate sizing of R_1 and R_2 is required to pursue optimum voltage-current interaction for nonlinearity mitigation of the RVCO *V-to-f* transfer characteristic.

The principle of tuning the RVCO frequency using the input resistive network was originally demonstrated for an RVCO operating at 1 V [8], and it is adopted here for the deep-subthreshold regime. However, the employed resistive network, although useful in mitigating third-order harmonic distortion (HD3), has only marginal effect in suppressing even-order harmonics (i.e., HD2 of single VCO-based ADC half is limited to about -20 dB), which justifies the adopted pseudo-differential ADC topology. Despite the $2\times$ power consumption and area, such solution entails a 3 dB higher SNR and superior power supply rejection compared to the single VCO-ADC path. The RVCO waveforms are sampled and differentiated by XOR-based FDCs, later shown in Fig. 3. The XOR-based topology limits the maximum RVCO frequency (f_{RVCO}) to less than half of the clock frequency (f_{CLK}). The FDC generates a 1-bit output stream whose time average is $2f_{\text{RVCO}}/f_{\text{CLK}}$. The ADC's Q-noise is first order noise shaped, while the oscillator phase noise (PN) appears in the low frequency region of the ADC output spectrum. To enable different input ranges (0.2 V to 0.5 V), the resistive network can be reconfigured to "map" the input signal to the desired frequency output range (as close as possible to its maximum, spanning from 0 to $f_{\text{CLK}}/2$), exploiting frequency-domain quantization to preserve the maximum achievable SQNR.

III. Circuit Implementation

The RVCO, whose schematic is shown in Fig. 2(a), comprises the input resistive tuning network of R_1, R_2, and a loop of eight cascaded delay stages implemented as pseudo-differential inverters. To maximize the RVCO gain, the delay stages employ extremely low-voltage threshold (elvt) MOS devices. As shown in Fig. 2(b), tuning R_1, R_2, and the pMOS bulk voltage BODYP allows shaping of the RVCO *V-to-f* transfer curve. In reality, due to the strong sensitivity of HD3 over R_1, it is the latter that is mostly tuned to suppress HD3, whereas R_2 and BODYP are only slightly adjusted to achieve fine matching between the positive and negative RVCO halves for further mitigation of even-order harmonics. An additional benefit of the adopted resistive divider scheme is that V_{tune} can be kept well below the 0.2-V core supply, ensuring that the RVCO maximum oscillating frequency is bounded to be less than the aforementioned half of the clock frequency, and furthermore allowing the input signal V_{IN} to significantly exceed 0.2 V. The aspect ratio of the pMOS and nMOS elvt transistors in RVCO is 96 μm/30 nm and 48 μm/30 nm, respectively. These are considerably large dimensions so as to limit the effect of process variations. R_1 and R_2 are poly resistors nominally equal to 5 kΩ and 1.5 kΩ, resulting in an input voltage range of 0.5 V, equivalent to $2.5\times$ the supply. Full-scale input ranges of 0.2, 0.3, and 0.4 V are achieved by configuring R_1 to 1.6-kΩ, 2.7-kΩ, and 4-kΩ, respectively. The R_1 and R_2 values are programmable between 1.6 kΩ and 7 kΩ and between 0.65 kΩ and 2 kΩ, respectively, in order to partly compensate for the *V-to-f* nonlinearity arising from random mismatch and supply variations. The spread in the RVCO center frequencies induced by random mismatches and voltage variations can instead be accommodated through tunable capacitors connected at the output of each of the oscillator's delay stages [indicated with C_L in Fig. 2(a)], which are implemented using custom fringe capacitors. The source terminals of the nMOS transistors within the back-to-back inverters cross-coupling the complementary outputs of each delay stage [$O+$ and $O-$ in Fig. 2(a)] are connected to ground rather than to V_{tune} so as to maximize the output swing (140 mV_{pp} when V_{IN} is at the upper bound of DR). This is in contrast to [8] where the lower bound of $O+/-$ would indeed be equal to V_{tune}, (only 30 mV_{pp} output swing for V_{IN} at the upper bound of DR and for the same transistor sizing). Such configuration would pose more challenges on the design of the following sampling latch (later shown in Fig. 3), whose regeneration time and input-referred offset would exhibit a higher sensitivity to the input signal amplitude (i.e., both the input peak-to-peak common mode voltage of the latch and the difference between maximum and minimum derivative of the voltage at nodes $O+$ and $O-$ would be higher).

The implementation of FDC is presented in Fig. 3(a) and consists of the aforementioned sampling latch, two D flip-flops (DFFs), and a XOR gate. All MOS are elvt devices so as to reduce the propagation delay. The sampling latch acts as a discrete-time preamplifier providing additional gain, reducing the regeneration time of the following

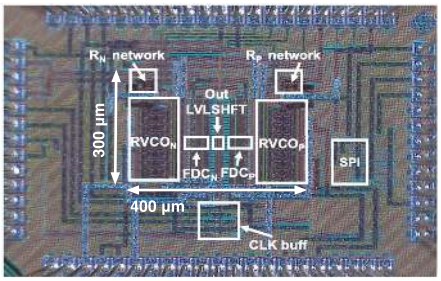

Fig. 4. Chip micrograph of the implemented VCO-based ADC.

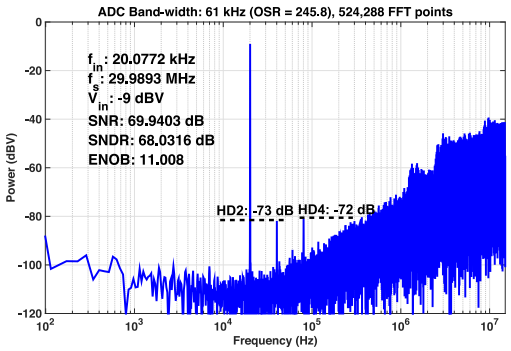

Fig. 5. Measured output spectrum of a 20-kHz 1 V_{pp} (−9 dBV) input differential sinewave sampled at 30 MS/s.

DFF and thus minimizing its metastability, which otherwise would be severe due to the slow transition edges of the RVCO waveforms as well as the signal-dependent level of the logic zeros that the sampling latch must sample. The latch tracks the differential RVCO outputs $O+$ and $O-$ when CLK is logic high, and it latches its value when CLK low is asserted, as shown in Fig. 3(b). The regeneration time of the sampling latch is shorter, about 5 ns, when the voltage at node $O+$ ($O-$) is constant at the moment the latching phase is asserted and, in particular, when it is equal to zero, which corresponds to the input terminal $V_{IN}+$ ($V_{IN}-$) being equal to zero. Sampling is instead particularly critical when, simultaneously, $V_{IN}+$ is close to the upper limit of the input range (0.5 V) and nodes $O+$ and $O-$ are commutating while the high-to-low CLK transition is occurring. In such case, the regeneration time of the latch can instead be as long as 12 ns, which is almost half of the clock period. The input transistors M3 and M4 act to modulate the effective impedance at nodes *L1*, *L1_B* seen into their drains. Transistor M7 resets the latch during tracking, while outputs *L1* and *L1_B* are pulled low. The input-referred offset is calibrated in foreground by tuning the number of parallel nMOS devices M1 and M2 connected to the source terminals of M3 and M4, which in subthreshold act as programmable source degeneration resistors. DFF1 and DFF2 front latch has the same topology as the upstream sampling latch. The XOR output is level-shifted to 1 V and buffered toward the output of the IC [see Fig. 3(c)] so as to be compatible with the off-chip data acquisition.

IV. Measurement Results

Fig. 4 shows the chip micrograph of the 0.2-V VCO-based ADC, fabricated in TSMC 28-nm LP CMOS and occupying an active area of 0.12 mm^2. The output spectrum of a 20-kHz input differential 1 V_{pp} (−9 dBV) sinewave sampled at 30 MS/s is presented in Fig. 5, demonstrating a peak SNDR of 68 dB over 61-kHz bandwidth.

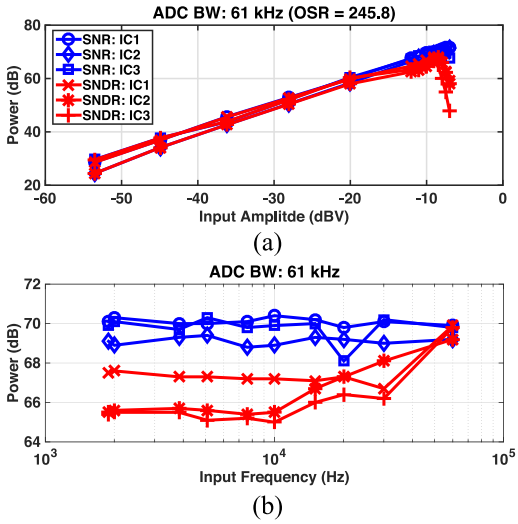

Fig. 6. Measured SNR and SNDR versus (a) input signal amplitude and (b) input frequency for three different ICs, with full-scale input range set to 0.5 V.

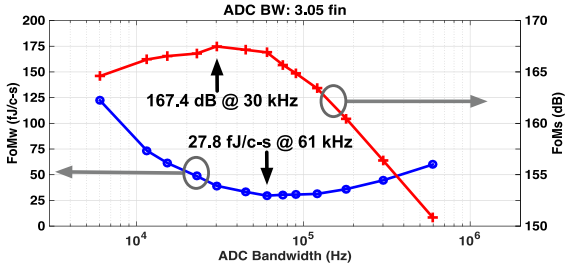

Fig. 7. Measured Walden and Schreier FoM versus ADC bandwidth, with full-scale input range configured to 0.5 V.

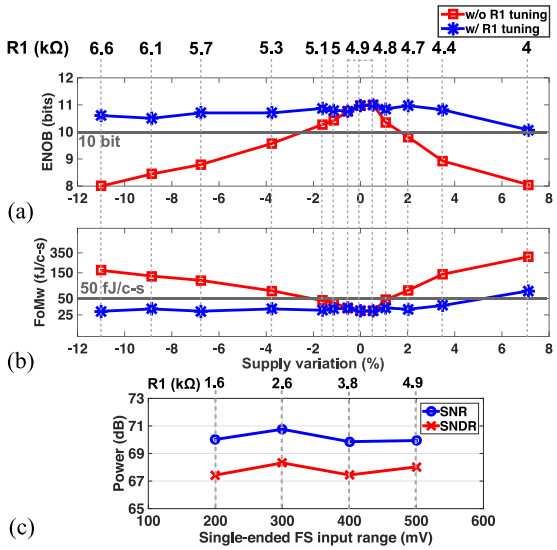

Fig. 8. (a) ENOB and (b) Walden FoM versus supply variation w/i and w/o input resistive R_1 tuning and with the input full-scale range configured to 0.5 V. (c) Measured SNR and SNDR versus input full-scale range.

The total harmonic distortion (THD) is dominated by the second and fourth harmonics, indicating a finite (but still effective) cancelation by the chosen pseudo-differential ADC topology, while odd-order harmonics contribute negligibly. The total consumed power is 7 μW: 6.5 μW for the RVCOs and 500 nW for the FDCs. This results

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART VCO-BASED AND SUBTHRESHOLD ADCS

Parameter	[4]	[3]	[5]	[9]	[10]	[6]	[7]	**This work**	
Type	Closed-loop VCO Phase domain	2-step VCO	NUS-VCO	CT-DS	DT-DS	Open-loop VCO	Open-loop VCO	**Open-loop VCO**	
Process (nm)	40	40	65	90	130	90	90	**28**	
Supply (V)	-	0.9	1.05	0.4	0.25	0.2	0.2	**0.2**	
Area (mm^2)	0.028	0.16	0.13	0.144	0.34	0.02	0.016	**0.12**	
Power (μW)	524	4,980	19,700	26.4	7.5	0.44	7.5	**7**	
Fs (MHz)	330	1,600	4,000	10.4	1.4	3.4	3.4	**30**	
BW (kHz)	6,000	40,000	200,000	50	10	20	20	**61**	
Single-ended input range (V)	0-VDD	0-0.9	0-1.05	0-0.4	0-0.25	+/- 0.2	+/- 0.2	**0-0.2**	**0-0.5**
SNR_{max} (dB)	69.1	68.7	60.1	74.4	-	47.4	68.9	**70.02**	**69.9**
$SNDR_{max}$ (dB)	68.6	66.8	58.5	74.4	61	44.2	60.3	**67.42**	**68**
$SFDR_{max}$ (dB)	84.7	77.1	63.6	85.2	70	-	-	**71.19**	**71.8**
ENOB (bits)	11.1	10.8	9.4	12.1	9.8	7	9.7	**10.91**	**11**
$FoM_{w,1}$ (fJ/c-s)	18.7	28	59.6	61.5	-	57.4	82.3	**22.4**	**22.3**
$FoM_{w,2}$ (fJ/c-s)	19.8	34.8	71.6	61.5	410	83	221.7	**29.9**	**27.8**
FoM_s (dB)	169.2	165.8	158.6	167.2	152.2	150.8	154.6	**166.8**	**167.4**

$FoM_{w,1}$: Power/($2^{(SNR-1.76)/6.02}$·2BW), $FoM_{w,2}$: Power/(2^{ENOB}·2BW), FoM_s: SNDR+10$\log_{10}$(BW/Power)

in Walden and Shreier FoM of 27.8 fJ/c-s and 167.4 dB, respectively. The characterization of SNR and SNDR versus input signal amplitude and frequency (f_{IN}) for three different ICs is presented in Fig. 6, where R_1, R_2 are optimized for 1 V_{pp} full-scale differential input. Fig. 7 shows instead the Walden and Schreier FoM versus signal bandwidth (f_{BW}), having fixed the sampling rate to 30 MS/s and the ratio f_{BW}/f_{IN} to slightly above 3 (so as to include the dominant harmonics into the SNDR calculation), while varying the oversampling-ratio (OSR), outlining that the best power efficiency is achieved when f_{BW} lies between 60 and 100 kHz. Indeed, for higher f_{BW}, the SNDR is mainly impaired by Q-noise power, while for lower f_{BW} it is dominated by the RVCO PN. The ADC effective resolution and power efficiency characterization versus 20% voltage variation across the nominal RVCO supply are shown in Fig. 8, resulting in a 3-bit ENOB deterioration at the boundary of such range. However, by properly adjusting R_1 between 4 kΩ at the maximum supply and 6.7 kΩ at the minimum, the ADC SNDR and power efficiency are restored to almost their maximum values. The same optimization can be applied to recover performance against temperature variations. Having identified the tuning "knobs" which are effective to restore the RVCO tuning range and linearity to their nominal value (R_1, R_2, C_L, and BODYP) spurs the interest toward the implementation of digitally assisted analog calibration techniques for process–voltage–temperature (PVT)-aware subthreshold designs. Fig. 8(c) demonstrates that input ranges from 0.2 to 0.5 V can be configured by tuning the resistor network accordingly as to obtain the maximum SNR and SNDR at nominal supply. Table I compares the proposed work with state-of-the-art in VCO-based and ULV $\Delta\Sigma$ ADCs. It achieves among the highest signal bandwidth and ENOB compared to ADCs with supply $\leq$ 0.4 V, demonstrating among the best power efficiency for both strong-inversion and subthreshold VCO-based ADCs.

V. CONCLUSION

The presented open-loop deep-subthreshold VCO-based ADC operates at 0.2 V. The maximized sampling rate of 30 MS/s enables wider bandwidths compared to previously reported 0.2-V designs. The VCO nonlinearity is mitigated with the mixed voltage/current-mode frequency tuning scheme of a tunable input resistive network. Such network allows the input signal range to be configured, with a maximum range exceeding the supply by 2.5$\times$ and further provides robustness versus supply variations. The merger of deep-subthreshold operation, minimization of the propagation delay of sampling latch, DFFs, and logic gates within the FDC, and the adopted resistive-based nonlinearity mitigation, enables the proposed ADC to overcome state-of-the-art of both weak and strong-inversion VCO-based ADCs, as well as that of near- and subthreshold ADCs.

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