A 0.20 mm² 3 nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS

A 0.20 mm^2 3 nW Signal Acquisition IC for Miniature Sensor Nodes in 65 nm CMOS

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***Abstract*—Miniature mm^3-sized sensor nodes have a very tight power budget, in particular, when a long operational lifetime is required, which is the case, e.g., for implantable devices or unobtrusive IoT nodes. This paper presents a fully integrated signal acquisition IC for these emerging applications. It integrates an amplifier with 32 dB gain and 370 Hz bandwidth that includes positive feedback to enhance input impedance and dc offset compensation. The IC includes also a 10 bit 1 kS/s SAR ADC as well as a clock generator and voltage and current biasing circuits. The overall system achieves an input noise of 27 μV_{rms}, consumes 3 nW from a 0.6 V supply, occupies 0.20 mm^2 in 65 nm CMOS, and has a single-wire data interface. The amplifier achieves an noise-efficiency factor (NEF) of 2.1 and the ADC has a figure-of-merit (FoM) of 1.5 fJ/conversion-step. Measurements confirm reliable operation for supplies from 0.50 to 0.70 V and temperatures in the range of 0–85 °C. As an application example, an ECG recording is successfully performed with the system while a 0.69 mm^2 photodiode array provides its power supply in indoor lighting conditions.**

***Index Terms*—ADC, amplifier, analog front-end, CMOS, ECG, sensor, signal acquisition.**

I. Introduction

SIGNAL acquisition systems for emerging applications, such as implantable or unobtrusively wearable autonomous sensors, large sensor arrays, or wireless self-powered sensors, require a minuscule form factor and sufficient operational lifetime. For instance, in case of implantable electronics, a lifetime of several years is demanded, while the smallest possible form factor will allow to reach more locations in the human body. The small size and weight inherently imply that the amount of energy available to supply the system will be limited. Thus, in order to achieve sufficient operational lifetime, the average power consumption has to be very low. Fig. 1 shows a few state-of-the-art examples of energy sources, when scaled to a size of 1 mm^3. As can be seen, the power available from a state-of-the-art 1 mm^3 solid-state thin-film battery is limited to 4 nW for a 10 year lifetime [1], and a 1 mm^3 energy harvester attached to a running person delivers only 7.4 nW [2]. In other words, the power consumption budget for a multiyear operational lifetime is in the order of 1–10 nW/mm^3. One of the critical tasks in these miniature systems is signal acquisition: signal conditioning and digitization of information from sensors. However, low-power signal acquisition systems that are presently available, for instance, as proposed in [3]–[5], have a power consumption that is still in the 20–1000 nW range as shown in Fig. 1. Furthermore, the required circuits do not only need a low absolute power (within a 1–10 nW budget), they also need to maintain high power efficiency, i.e., deliver high performance given their power consumption. This is nontrivial, as the impact of fixed power dissipators such as biasing networks, clock generation, and leakage currents will start to become more pronounced at such low-power consumption levels. One approach to overcome this issue is to use more simplistic circuitry, for instance, by simplifying biasing networks or common-mode feedback (CMFB) networks. However, such an approach could lead to higher PVT sensitivity and lower reliability, as will be detailed later in Section III.

This work, which is an extended version of [6], presents a fully integrated signal acquisition IC including an amplifier and ADC, as well as voltage and current biasing and clock generation circuits. As a proof of concept, it shows that a low absolute power, a high power efficiency, and a PVT-robust design can be achieved at the same time. With 3 nW power consumption and state-of-the-art power efficiency, it can still ensure enough circuit reliability, precision, and bandwidth to enable practical applications.

This paper is organized as follows. Section II describes the design and optimization of the overall signal acquisition system, Section III presents the circuit-level implementations, followed by measurement results in Section IV. Finally, conclusions are drawn in Section V.

II. System Design and Optimization

Fig. 2 presents the implemented system, which requires only a single supply voltage, has five external connections and no external components. It contains a differential amplifier, an SAR ADC, a serial data interface, a clock generator, and voltage and current biasing circuits. A reduced supply voltage is used to save power. Theoretically, more power can be saved at lower supply levels, but this comes at the cost of losing dynamic range, speed, and robustness. As a compromise, a nominal supply of 0.6 V was selected as it allows to use relatively conventional circuit implementations, provides sufficient performance and robustness, and also saves substantial power.

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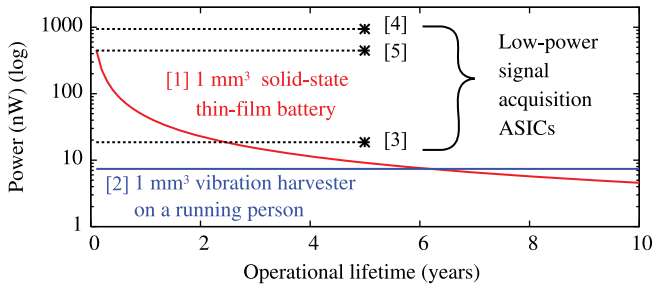

Fig. 1. State-of-the-art energy sources and signal acquisition ICs.

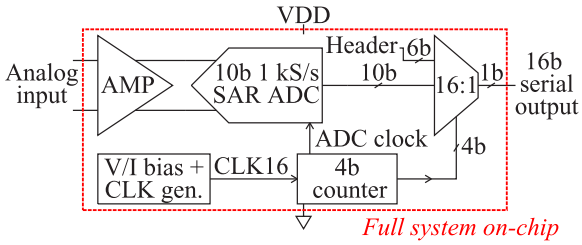

Fig. 2. Fully integrated signal acquisition system.

Typically, signal acquisition systems are optimized for a particular application. In this case, due to the very scarce energy resources that are available in an mm^3-sized node, a feasibility calculation is performed first to investigate the potential performance given a power budget of 3 nW. First of all, considering that the amplifier and ADC are the most critical blocks, 1 nW is assigned to each of these circuits, leaving 1 nW for the remaining auxiliary circuits. Next, the dynamic range of the system is determined, which is related to the effective resolution or ENOB of the ADC. A higher dynamic range is desirable as it allows a better signal-to-noise-ratio (SNR), it can tolerate larger signal-strength variations, and it can tolerate larger interference signals such as motion artifacts without saturating the system. Typical low-power signal acquisition systems [3]–[5], [7] use ADCs with a resolution of 8, 9, 10, or 12 bit, while achieving an ENOB from 7.1 to 10.2 bit. To be in line with these existing systems, a 10 bit ADC with an expected ENOB of 9 bit is selected in this work. The noise of this ADC is determined by the quantization noise as well as the thermal noise of the circuitry. The quantization noise, equal to $0.289V_{\mathrm{LSB}}$, can be estimated as 280 μV_{rms} for this 10 bit ADC, assuming a differential full-scale range $V_{\mathrm{FS,ADC}}$ of 1 V_{pp}. Including some budget for thermal noise, the total ADC noise is coarsely estimated as $V_{n,\mathrm{ADC}} = 400$ μV_{rms}. Next, using a well-known figure-of-merit (FoM) for ADCs, the achievable performance can be predicted. The following FoM is used [8]:

$$\mathrm{FoM} = \frac{P}{2^{\mathrm{ENOB}} \cdot \min(f_s, 2\mathrm{ERBW})} \tag{1}$$

where P is the power consumption, ENOB is the effective-number-of-bits, f_s is the sample rate, and ERBW is the effective resolution bandwidth of the ADC. A survey of state-of-the-art ADCs [9] reveals that 10 bit ADCs can nowadays achieve an FoM in the order of 2 fJ/conversion-step. As the ERBW is not a limiting factor in this low-speed application, and an ENOB of 9 bit is required, this implies that a sample rate of 1 kS/s should be achievable within the 1 nW budget.

As a next step, the parameters of the amplifier are optimized. Considering that the ADC's sampling rate is set to 1 kS/s, it is logical to set the amplifier's bandwidth to a value slightly lower than the Nyquist frequency of $\frac{1}{2}f_s$, for instance, 400 Hz. Using the noise-efficiency factor (NEF) defined in [10], the amplifier performance can now be predicted

$$\mathrm{NEF} = V_{n,\mathrm{amp}}\sqrt{\frac{2 \cdot I_{\mathrm{total}}}{\pi \cdot V_t \cdot 4kT \cdot \mathrm{BW}}} \tag{2}$$

where $V_{n,\mathrm{amp}}$ is the total input-referred noise (IRN), I_{total} is the total current consumption, V_t is the thermal voltage, and BW is the bandwidth of the amplifier. Existing low-power amplifiers [3]–[5], [11] show that an NEF around 2 is achievable. With a bandwidth of 400 Hz and a current consumption budget of 1.7 nA at 0.6 V supply, this leads to a predicted IRN of $V_{n,\mathrm{amp}} = 25$ μV_{rms}.

The final parameter to decide is the gain of the amplifier, which will determine the overall IRN as well as the full-scale input range. The IRN of the system ($V_{n,\mathrm{sys}}$) can be expressed as a combination of the amplifier noise ($V_{n,\mathrm{amp}}$), the ADC noise ($V_{n,\mathrm{ADC}}$), and the gain (A) of the amplifier

$$V_{n,\mathrm{sys}}^2 = V_{n,\mathrm{amp}}^2 + \frac{V_{n,\mathrm{ADC}}^2}{A^2}. \tag{3}$$

At the same time, the peak-to-peak full-scale input range $V_{\mathrm{FS,in}}$ is determined by the ADC's range divided by the amplifier gain

$$V_{\mathrm{FS,in}} = \frac{V_{\mathrm{FS,ADC}}}{A}. \tag{4}$$

Thus, on one hand, the gain A needs to be large enough to sufficiently suppress ADC noise (3), but on the other hand, it should be minimized to maximize the full-scale input range (4). As a compromise, the gain is set to $A = 40\times$, leading to a predicted system with an overall IRN of $V_{n,\mathrm{sys}} = 27$ μV_{rms}, an input range $V_{\mathrm{FS,in}}$ of 25 $\mathrm{mV_{pp}}$, a bandwidth of 400 Hz, and a power consumption of 2 nW for the core components.

As a result of the above analysis and optimization, it is demonstrated that it is feasible to develop a signal acquisition system within the assigned power budget. It should be noted that this system, in particular, in terms of IRN, cannot reach the same absolute level of performance as prior ASICs [3]–[5] due to the power constraints. Nonetheless, the envisioned performance enables extreme miniaturization of sensing nodes and is still sufficient for a variety of applications, such as ECG monitoring, physiological signal acquisition for implantable devices, or monitoring of environmental information.

III. Circuit Implementation

Based on the system-level design described in Section II, this section will discuss the circuit-level implementation of the amplifier, the ADC, and the auxiliary circuits.

A. Amplifier

The ac-coupled amplifier is composed of a two-stage amplifier (A_1, A_2) and a dc servo loop (DSL), as shown in Fig. 3. The

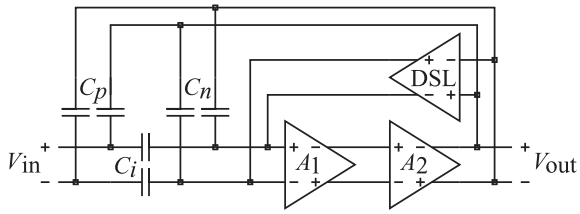

Fig. 3. Overview of the capacitively coupled amplifier.

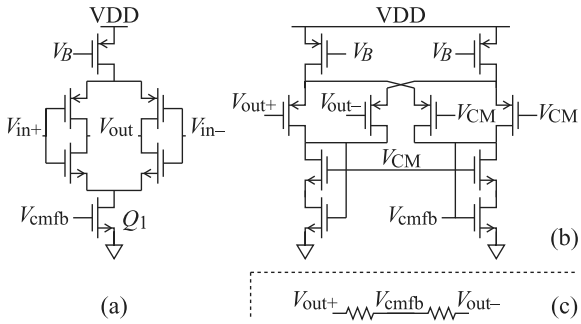

Fig. 4. Implementation of the (a) main amplifiers and their (b) active CMFB. Also shown is an (c) alternative CMFB topology.

capacitor ratio $C_i/C_n = 40$ pF/1 pF sets the differential gain to $40\times$ (32 dB) while capacitors C_p are used to increase the input impedance, as will be discussed later in detail. The DSL provides dc biasing to A_1, limits dc offset, and results in a high-pass corner frequency of the capacitively coupled amplifier. As the ac-coupled amplifier can only process ac information, the dc offsets of the amplifier stages and ADC are not calibrated or compensated. Their values are small enough to have no significant impact on the ac performance. To maintain stability, A_1 is dimensioned for relatively low gain and high bandwidth, while A_2 is dimensioned for high gain and low bandwidth. The latter can be achieved easily thanks to the large capacitive load already present at the second stage output node. In terms of noise, the first stage gain ($\approx 20\times$) can still sufficiently suppress the noise of the second stage.

The transistor-level implementation of amplifiers A_1 and A_2 is shown in Fig. 4(a). Both amplifiers use the same topology but with different parameters. For best power efficiency, the input transistors are biased in weak inversion, and an inverter-based input pair is applied to double the g_m. Based on noise requirements, the bias current for A_1 is set to 1 nA, while A_2 uses 0.2 nA. This biasing current is determined by voltage V_B, which is set by a bias current I_{amp} (discussed in Section III-C) through current mirrors. As the amplifiers are differential, a CMFB is required. Either a passive or an active CMFB could be adopted. As a first solution, a simple passive structure is considered. This approach uses two resistors connected in series to the differential output nodes of the inverter-based amplifier [Fig. 4(c)]. The midpoint of these resistors determines the common-mode voltage and can directly drive the gate of the CMFB transistor Q_1. However, in this structure, the common-mode output voltage is directly related to the threshold voltage and overdrive voltage of Q_1: $V_{\text{cm,out}} = V_{\text{th}} + V_{\text{ov}}$. While this solution

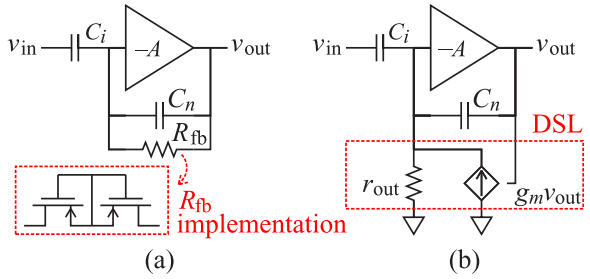

Fig. 5. DC biasing strategies. (a) Passive resistor network. (b) Active feedback.

can work well, it is dependent on PVT variations: V_{th} can typically shift with more than 100 mV over process and temperature corners, leading to a similar shift in $V_{\text{cm,out}}$. Considering the supply is only 0.6 V, this leads to a substantial loss of signal range. Further, when the supply voltage is changed, $V_{\text{cm,out}}$ will not track the midsupply level but remains at a fixed level set by Q_1. As a result, this implies that the output common-mode and hence the output swing reach an optimum for one particular supply only. Because of these drawbacks, this work implements active CMFB circuits as shown in Fig. 4(b), such that the $V_{\text{cm,out}}$ is correctly tuned to a V_{CM} reference of $\frac{1}{2}$VDD, irrespective of PVT variations.

The DSL amplifier implements three functions: first, the differential feedback reduces the amplifier's offset. Second, the CMFB of the DSL tunes the DSL's output common-mode voltage to $\frac{1}{2}$VDD. As this voltage is directly applied to the input of A_1, it thus indirectly provides biasing to the input pair of A_1. Third, the DSL sets the high-pass corner of the amplifier. Instead of using an active DSL, a passive circuit using only resistors could be used as well to implement exactly the same functionality; both these alternatives are shown in Fig. 5. As large resistor values are required in the passive solution [Fig. 5(a)], pseudoresistors using transistors are typically employed. In the active DSL solution [Fig. 5(b)], the DSL amplifier is modeled using a transconductance g_m and output resistance r_{out}. In the first case, the pole frequency is given by $f_{\text{hp}} = \frac{1}{2\pi R_{\text{fb}} C_n}$. As R_{fb} is implemented with a pseudoresistor, its value can shift substantially over PVT variations (about $100\times$ over a 0–85 °C temperature range according to simulations). This implies that the cutoff frequency cannot be defined accurately. Moreover, in case, the resistance is too large, it can lead to a substantial shift of the bias point of the amplifier due to voltage drop caused by gate leakage of the input pair of A_1. Because of the variability of the passive solution, this work proposes to use a DSL instead [Fig. 5(b)]. Now, the pole frequency is given by $f_{\text{hp}} = \frac{g_m}{2\pi C_n}$. In weak inversion, $g_m = \eta \frac{q}{kT} \cdot I_D$ is also temperature dependent but will show much less variation ($\sim 25\%$) than a pseudoresistor ($100\times$). Moreover, the bias current scheme generating I_D can be designed to counteract the temperature coefficient of g_m. As the DSL provides more robust performance, this solution was adopted in this work. The actual DSL implementation is shown in Fig. 6(a), with its CMFB in Fig. 6(b). The most important challenge in the DSL design is to minimize its g_m to enable a low-frequency cutoff point. To do so, the amplifier does not use inverter-based inputs but uses a normal differential pair. Further, the bias current is tuned down

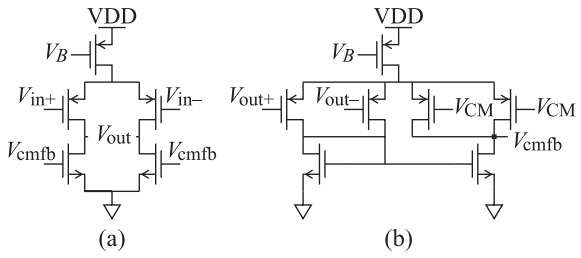

Fig. 6. Implementation of the (a) DSL amplifier and its (b) CMFB circuit.

to less than 2 pA and transistor lengths are increased to 40 µm. The simulated g_m equals 20 pA/V, yielding an estimated $f_{\rm hp}$ of 3 Hz.

Capacitors C_p (1 pF) create a positive feedback loop to increase the input impedance (Fig. 3). In the pass-band of the amplifier, the input will see C_i as well as C_p (assuming a single-ended view for simplicity). The voltage across C_i is equal to the input voltage $v_{\rm in}$, as the input of A_1 is a virtual ground. The voltage across C_p is equal to $v_{\rm in} - v_{\rm out} = -39\ v_{\rm in}$. Thus, the effective input capacitance seen by the input is $40 - 39 = 1$ pF, rather than the 40 pF without positive feedback applied. At the lower and higher end of the amplifier's bandwidth, the impedance will gradually change due to impact from the DSL or from the reduced amplifier gain. For near-dc signals (below the cutoff frequency of the DSL), $v_{\rm out}/v_{\rm in}$ approximates 0, and hence the input capacitance increases to $C_i + C_p = 41$ pF. Above the amplifier's bandwidth, the open-loop gain will go to zero, resulting in a floating node at the input of A_1 and $v_{\rm out}/v_{\rm in} = 0$ V. In this case, the input impedance is the series of C_i and C_n, in parallel to C_p, which is approximately 2 pF.

B. ADC

A low-power 10 bit 1 kS/s SAR ADC (Fig. 7) is implemented in this work. The differential analog input is first sampled on the top plates (nodes OUTP and OUTN) of the capacitor arrays that also implement the DAC functionality. During successive approximation, the DAC capacitively subtracts a voltage from the sampled voltage by means of charge redistribution, as in [12]. Therefore, the outputs OUTP and OUTN represent the difference between the sampled input voltage and the DAC-induced voltage. This output signal is thus forwarded to the comparator to close the SAR loop. To avoid the need of an oversampled clock, a self-synchronized architecture is used, meaning that a single rising edge on the external 1 kHz ADC clock is sufficient to perform an AD conversion. Internal synchronization of the various SAR operations is achieved by creating a clock locally using an oscillation loop formed by the comparator and a delay element [13], [14]. On the rising edge of the ADC clock, this oscillation is enabled and initiates the SAR operation. When all 10 bits are resolved, the oscillation loop is disabled and the ADC returns to a sleep state while the T&H starts to track the next analog input. Clock boosting is used to achieve sufficient T&H linearity [15] by boosting the switch driving voltage to about 1 V. Despite the low VDD of 0.6 V, high-V_t devices are used in the ADC to minimize leakage power. The dynamic comparator [16] is operating

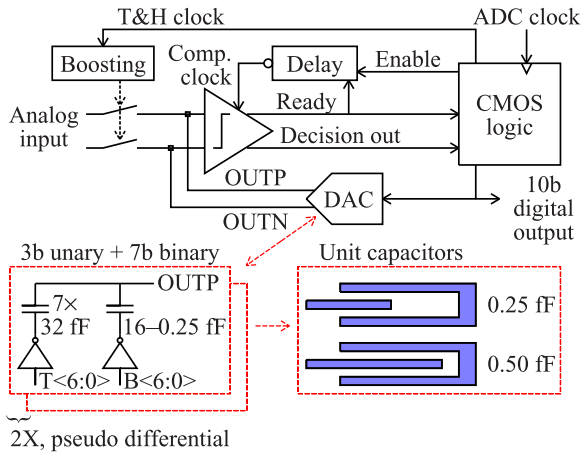

Fig. 7. 10b asynchronous SAR ADC implementation, DAC implementation, and capacitor layout.

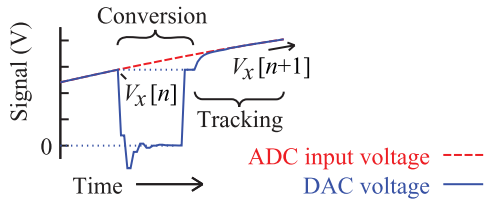

Fig. 8. Illustration of the ADC's input voltage and DAC voltage in time.

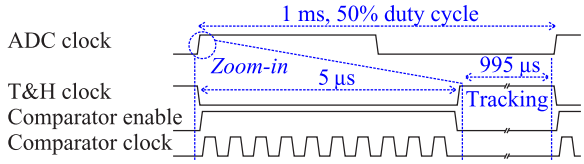

Fig. 9. Illustration of the analog-to-digital conversion process.

in subthreshold for best power efficiency. The 10b capacitive DAC uses a segmentation of three unary bits and seven binary bits to save power while improving DNL [14]. For simplicity, a single-ended view of the DAC is shown in Fig. 7, but the actual implementation uses two copies of this circuit. To save power, the LSB unit capacitor in the DAC is reduced to 0.25 fF, yielding an overall DAC capacitance of 300 fF (including parasitics), which is still sufficient for kT/C-noise requirements. In terms of mismatch, this small capacitor value is still expected to be sufficient based on previous experience, as discussed, for instance, in [12] and [14]. Hence, no calibration or trimming is applied. Ideally, each side of the DAC would be composed of $2^{10} - 1 = 1023$ unit capacitors of 0.25 fF. To save chip area and reduce parasitics, the DAC is in reality composed of 511 units of 0.5 fF and a single unit of 0.25 fF. These small units are based on fringing capacitors, of which a layout sketch is shown in Fig. 7 [12], [17]. To increase capacitor density while reducing parasitics to the substrate, two high metal layers are used in parallel to implement these capacitors. Mostly thanks to the small DAC capacitors, the simulated power consumption of the ADC is approximately 1 nW at 1 kS/s. Further, as the ADC has no static biasing but uses purely dynamic circuits, this power scales linearly with the sampling rate.

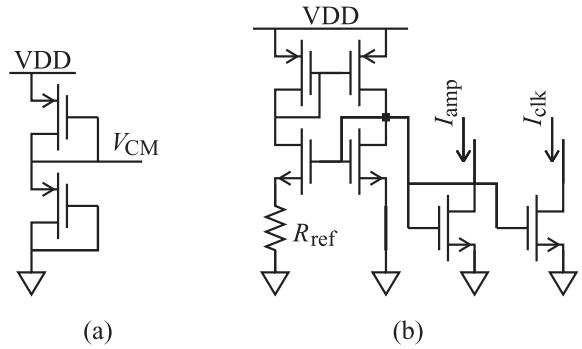

Fig. 10. (a) Common-mode reference circuit. (b) Bias current generation.

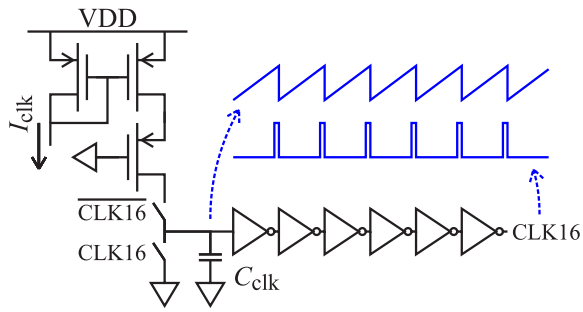

Fig. 11. 16 kHz clock generation circuit.

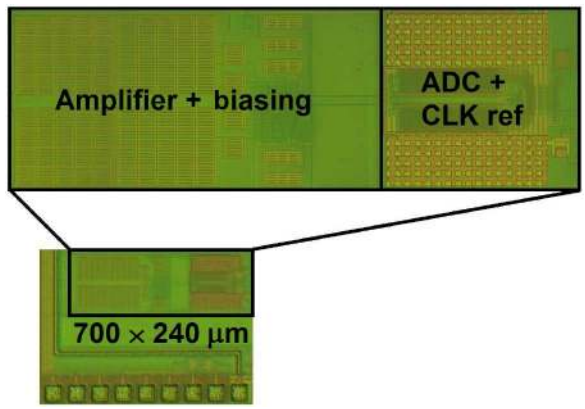

Fig. 12. Die photo in 65 nm CMOS.

To save power on system level when connecting the amplifier to the ADC, the conversion process in Fig. 8 is considered. As can be seen, during the tracking period, the DAC voltage follows the ADC's input voltage. During the conversion phase, the DAC is disconnected from the input node and will successively approximate the sampled input voltage $V_x[n]$. Typical SAR ADCs discharge the DAC to 0 V after each conversion before the tracking of the next input signal $V_x[n+1]$ starts. During the tracking phase, the equivalent DAC capacitance C_{DAC} thus needs to be charged from 0 V to $V_x[n+1]$ within the tracking time τ_t. Assuming a slew-rate limited situation, this implies that the current I_{out} drawn from the amplifier is given by

$$I_{\mathrm{out}} = C_{\mathrm{DAC}} \frac{V_x[n+1]}{\tau_t} \tag{5}$$

which thus depends on the DAC capacitance C_{DAC}, the amplitude of the input signal V_x and the duration of the tracking

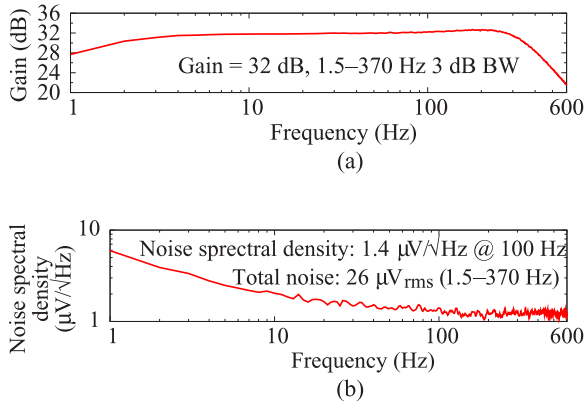

Fig. 13. Amplifier measurements. (a) Gain. (b) IRN.

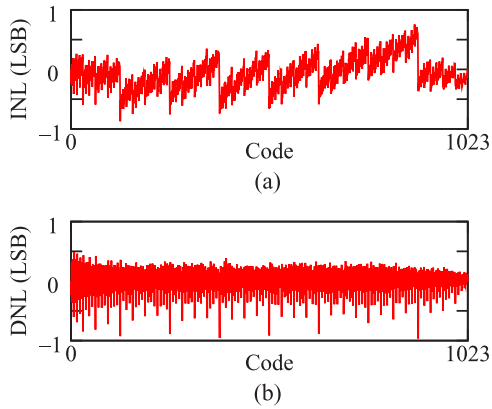

Fig. 14. Static ADC measurements. (a) INL. (b) DNL.

period τ_t. To save power, first of all the DAC capacitance is minimized by using small unit capacitors, as detailed before. Second, the DAC in this particular ADC is not reset to 0 V after conversion, but it returns to the previously sampled voltage $V_x[n]$ before starting to track the next voltage $V_x[n+1]$. Because of that, the current drawn from the amplifier is now given by

$$I_{\mathrm{out}} = C_{\mathrm{DAC}} \frac{V_x[n+1] - V_x[n]}{\tau_t} \tag{6}$$

which is dependent on the delta between consecutive input signals rather than their amplitude. Since in many biomedical applications, the highest amount of signal energy is concentrated at lower frequencies, and the power at higher frequencies is limited, the second alternative reduces the output current requirements for the amplifier. As a final step of power saving, the tracking time τ_t is maximized by taking advantage of the asynchronous clocking scheme of the ADC and the speed available from modern CMOS processes. As illustrated in Fig. 9, the AD conversion is initiated on a rising edge of the ADC clock. As soon as the conversion is finished, which is approximately in 5 µs, the ADC returns to tracking mode without waiting for the falling edge of the ADC clock. Since the total clock period is 1 ms, this results in a tracking phase which is 99.5% of the total clock period.

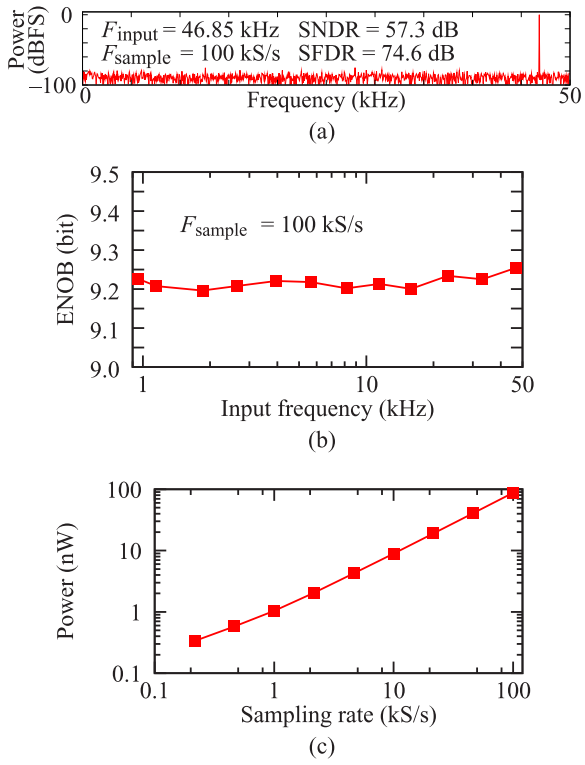

Fig. 15. Dynamic ADC measurements. (a) Single-tone output spectrum. (b) ENOB versus input frequency. (c) Power consumption versus sampling rate.

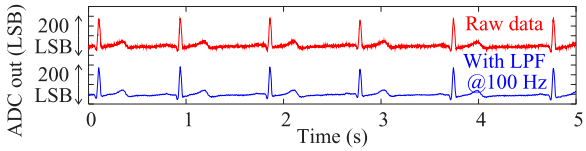

Fig. 16. Measured *in vivo* ECG using the complete signal acquisition system powered from a 0.69 mm^2 photodiode array.

C. Biasing Circuits, Clock Generation, and Serial Data Interface

This section describes the various auxiliary circuits that are needed to fully integrate the signal acquisition system. First of all, a common-mode reference V_{CM} for the amplifier is created by two diode-connected PMOS devices in subthreshold mode [Fig. 10(a)], consuming only 20 pW. Further, Fig. 10(b) shows a standard bootstrapped current reference circuit which creates two bias currents: one for the amplifier stages (I_{amp}) and one for the clock generator (I_{clk}). All transistors inside this reference circuit are biased in the subthreshold regime, allowing operation at supply voltages down to 0.5 V. A large R_{ref} of 40 MΩ is used to have reasonably stable operation over process corners, resulting in $\pm 20\%$ variation of the generated reference currents while consuming 0.4 nW.

The serial data interface in Fig. 2 multiplexes 16 bit of data into a single-wire interface. Each 16 bit packet contains 10 bit of ADC data, preceded by a fixed code pattern of 6 bit. This header enables a receiving chip to correctly synchronize itself to the received packets, and thus to recover the clock frequency and ADC data. For multiplexing the data, the 16:1 MUX is controlled by a 4 bit counter that runs at 16$\times$ the ADC sampling rate. Thus, a clock signal at 16 kHz is needed considering the ADC operates at 1 kS/s. To generate this clock, the previously generated reference current I_{clk} is mirrored and integrated on a capacitor C_{clk} of 10 fF, as shown in Fig. 11. A feedback loop resets C_{clk} after a threshold voltage is reached, thus creating a

TABLE I
SIMULATED POWER CONSUMPTION AT 0.6 V SUPPLY

Component	Power consumption
Amplifier	1.05 nW
A1 main stage	0.60 nW
A1 CMFB stage	0.24 nW
A2 main stage	0.12 nW
A2 CMFB stage	0.06 nW
DSL main stage	1 pW
DSL CMFB stage	30 pW
ADC	0.87 nW
DAC	0.19 nW
T&H	0.04 nW
Comparator	0.50 nW
Logic	0.14 nW
Other components	1.26 nW
VCM bias	0.02 nW
Current bias	0.40 nW
Clock generation	0.49 nW
Serial interface	0.35 nW
Overall system	3.18 nW

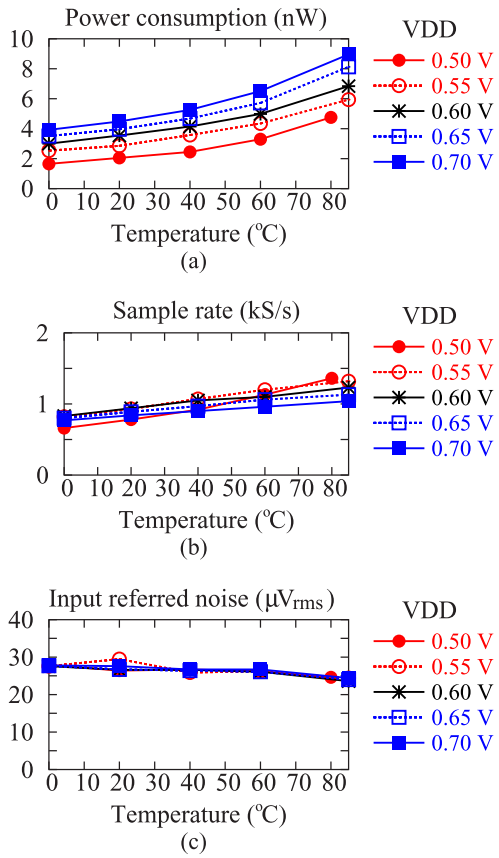

Fig. 17. Measurements as function of temperature and supply. (a) Overall power consumption. (b) ADC clock frequency. (c) Overall IRN.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

		This work	[3]	[4]	[5]	[11]	[14]		[18]
System	Process (nm)	65	65	180	350	180	65		40
	Area (mm^2)	0.20	0.6 *	0.25 *	1	0.25	0.076		0.0065
	VDD (V)	0.6	0.6	0.45	1	1	0.6		0.45
	VT corner measurements	0.50–0.70 V 0–85 °C	N/A	N/A	N/A	N/A	N/A		N/A
	Power (nW)	3	18.6	940	445–895	266	72	97	84
Amplifier	Power (nW)	1.0	16.8	730	33–337	266			
	BW min. (Hz)	1.5	<0.5	0.25	4.5 m–3.6	<1			
	BW max. (Hz)	370	250	10 k	31–292	>500			
	IRN (μV_{rms})	26	6.52	3.2	2.5	1.54			
	Gain (dB)	32	51–96	52	46–60	59 ##			
	CMRR (dB)	60 at 100 Hz	55	73	71	89			
	PSRR (dB)	63 at 100 Hz	67	80	84	92			
	NEF	2.1	2.64	1.57	3.26	1.38			
ADC	Power (nW)	1.1/88 **	1.8	1350 #	230		72	97	84
	Resolution (bit)	10	8	9	12		10	12	10
	ENOB (bit)	9.2	7.14	8.27	10.2		9.4	10.1	8.95
	INL (LSB)	0.87	1.8	1	1.4		0.48	1.90	0.44
	DNL (LSB)	0.96	1.0	0.5	0.8		0.32	0.97	0.45
	F_{sample} (kS/s)	1.1/100 **	0.5	200 #	1		40	40	200
	FoM (fJ/c.step)	1.7/1.5 **	25.5	22	196		2.7	2.2	0.85

*Estimated.
**Performance in integrated system and standalone at max sampling rate respectively.
ADC performance per 10 channels.
Open-loop.

saw-tooth wave as illustrated. The saw-tooth results in a clock signal CLK16 of nominally 16 kHz. A chain of six inverters is used to create delay in the feedback loop to ensure a sufficiently long on-pulse for the generated clock. Also, the first inverter uses transistors with increased lengths to avoid short-circuit power loss due to the saw-tooth input signal. As shown in Fig. 2, CLK16 drives a 4 bit counter which controls the MUX. At the same time, the counter acts as a clock divider to generate a 1 kHz ADC clock.

IV. MEASUREMENTS

The signal acquisition system was implemented in a 65 nm CMOS technology and occupies a chip area of 0.20 mm^2 including supply decoupling capacitors but excluding the pads (Fig. 12). The relatively large size of the amplifier and biasing circuits is caused by the passive components, mostly the 40 pF input capacitors and the $40\ M\Omega$ reference resistor. In the following, stand-alone measurement of the amplifier and ADC will be shown first, followed by characterization of the full system. Unless stated otherwise, all measurements are performed at 0.6 V supply and room temperature.

A. Stand-Alone Amplifier and ADC Measurements

The measured amplifier shows a gain of 32 dB and a -3 dB bandwidth from 1.5 to 370 Hz [Fig. 13(a)]. Fig. 13(b) shows the IRN density, which is $1.4\ \mu V/\sqrt{\text{Hz}}$ at 100 Hz. Integrated over the amplifier's bandwidth, this results in an integrated IRN level of 26 μV_{rms}. With a power consumption of 1 nW at 0.6 V supply, this gives an NEF of 2.1. The measured CMRR and PSRR (at 100 Hz) of the amplifier are 60 and 63 dB, respectively.

The stand-alone ADC was characterized at 0.6 V supply. It operates at sampling rates up to 100 kS/s thanks to the ~ 5 µs conversion time. As shown in Fig. 14, it achieves an INL and DNL of 0.87 and 0.96 LSB, respectively. Fig. 15(a) shows a measured near-Nyquist spectrum when operating at the maximum speed of 100 kS/s. The achieved SNDR is 57.3 dB, giving an ENOB of 9.2 bit. This ENOB is maintained throughout the full bandwidth as can be seen in Fig. 15(b). Further, Fig. 15(c) confirms that the dynamic power consumption of the ADC scales linearly with the sampling rate down to a leakage level of 0.15 nW. At 100 kS/s, the power consumption is 87.8 nW, resulting in an FoM of 1.5 fJ/conversion-step.

B. System Measurements

To provide an application example and to demonstrate the practical performance of the fully integrated system, the IC is used to perform an *in vivo* ECG recording. A three-electrode setup is used where two electrodes capture the ECG signal on the chest and a third electrode is used for grounding. Further, to demonstrate the low-power consumption and the ability to create miniature systems, the supply is directly provided by a $0.69\ mm^2$ photodiode array, composed of three TEMD7000X01 PIN photodiodes in series. In indoor fluorescent lighting conditions, a single TEMD7000X01 PIN photodiode was measured to have an open circuit voltage of only 0.2 V. Thus, by connecting three devices in series, a sufficiently high supply voltage can be generated for the IC. No power regulation

is used, nor are external filters or capacitors applied. Fig. 16 displays the captured ADC data. Both the raw data without any processing are shown as well as the data after applying an LPF at 100 Hz in processing software.

At room temperature, the total measured power consumption of the system is 3 nW from a 0.6 V supply. A power breakdown, based on simulations, is shown in Table I. To verify the robustness of the system over supply and temperature corners, the power consumption, sampling rate, and IRN are measured in a 0–85 °C temperature range and a 0.5–0.7 V supply range. The power consumption [Fig. 17(a)] ranges from 2 up to 9 nW and shows a gradual increase with temperature. This is caused by the increase of leakage currents and the increase of the generated reference current. The latter effect directly increases the power consumption of the amplifier and also results in a proportionally higher clock frequency [Fig. 17(b)], thereby increasing the power consumption of the ADC. The IRN [Fig. 17(c)] of the full system (amplifier and ADC) is 27 $\mu V_{\rm rms}$ under nominal conditions. As the dominant IRN voltage is coming from the amplifier's input pair, it is proportional to kT/g_m. As g_m is proportional to the bias current I_B in the subthreshold mode, this implies that the IRN voltage is proportional to T/I_B. Normally, this implies that the noise will increase with temperature. However, as explained before, the generated bias current also increases with temperature T, thereby resulting in a relatively stable noise performance over VT variations.

Table II summarizes the performance of this work and gives a comparison to state-of-the-art low-power signal acquisition ICs [3]–[5], an amplifier [11], and ADCs [14], [18]. Compared to the other integrated systems, this work has the lowest power consumption, occupies the smallest chip area, and is the only low-power design verified over supply and temperature corners to validate robustness. Logically, due to fundamental noise-power tradeoffs, the sixfold power reduction comes at the cost of an increased IRN. However, the power efficiency figures of the proposed work (NEF $=$ 2.1 for the amplifier and FoM $= 1.5$ fJ/conversion-step for the ADC) are well in line with state-of-the-art amplifiers and ADCs.

V. Conclusion

This work demonstrated a fully integrated signal acquisition ASIC. With a chip area of 0.20 mm^2 and a power consumption of 3 nW, it enables miniature, long-term sensing applications. The sixfold reduction in power consumption compared to prior art is achieved while providing adequate accuracy and speed to enable, e.g., biopotential sensing applications. At the same time, the IC offers a bandwidth, ADC speed, and ENOB well in line with alternative systems. Despite the low absolute power, state-of-the-art power efficiency in the amplifier (NEF $= 2.1$) and ADC (FoM $= 1.5$ fJ/conversion-step) is achieved. Measurements over supply and temperature corners confirm that, despite the extremely low-power consumption, the circuit shows reliable and predictable behavior.

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