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A 0.3V Rail-to-Rail Three-Stage OTA with High DC Gain and Improved Robustness to PVT Variations

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ABSTRACT This paper presents a novel 0.3V rail-to-rail body-driven three-stage operational transconductance amplifier (OTA). The proposed OTA architecture allows achieving high DC gain in spite of the bulk-driven input. This is due to the doubled body transconductance at the first and third stages, and to a high gain, gate-driven second stage. The bias current in each branch of the OTA is accurately set through gate-driven or bulk-driven current mirrors, thus guaranteeing an outstanding stability of main OTA performance parameters to PVT variations. In the first stage, the input signals drive the bulk terminals of both NMOS and PMOS transistors in a complementary fashion, allowing a rail-to-rail input common mode range (ICMR). The second stage is a gate-driven, complementary pseudo-differential stage with an high DC gain and a local CMFB. The third stage implements the differential-to-single-ended conversion through a body-driven complementary pseudo-differential pair and a gate-driven current mirror. Thanks to the adoption of two fully differential stages with common mode feedback (CMFB) loop, the common-mode rejection ratio (CMRR) in typical conditions is greatly improved with respect to other ultra-low-voltage (ULV) bulk-driven OTAs. The OTA has been fabricated in a commercial 130nm CMOS process from STMicroelectronics. Its area is about $0.002mm^2$, and power consumption is less than 35nW at the supply-voltage of 0.3V. With a load capacitance of 35pF, the OTA exhibits a DC gain and a unity-gain frequency of about 85dB and 10kHz, respectively.

INDEX TERMS bulk-driven OTA, ultra-low voltage, three-stage amplifier, body-biased, local common mode feedback (LCMFB).

I. INTRODUCTION

Recent years have seen a growing interest in sub-0.5V electronics [1], [2], motivated not only by the need to minimize power consumption, but also to allow powering the system by exploiting energy harvested from the environment: energy harvesting systems typically provide DC voltages of a few hundreds milliVolts [3]. Since, for digital circuits, supply voltage lowering results mainly in a speed degradation, operating digital systems at ULV conditions (e. g. supply voltage lower than 0.5V) is still feasible by exploiting the subthreshold operation of CMOS gates and using a reduced clock frequency. The situation is quite different for analog circuits. In fact, the reduction of the supply voltage below 0.5V, combined with the reduced intrinsic gain of MOS transistors implemented in modern deep submicron technologies [4], [5], makes it very hard to meet design goals of analog circuits, and solutions where analog functions are implemented taking advantage of true digital circuits have been proposed in the literature [6], [7].

The operational transconductance amplifier (OTA) is a key building block for analog applications, and the ultra-low voltage (ULV) and ultra-low power (ULP) context makes designing high performance OTAs very hard. In particular, when the supply voltage is reduced to 0.5V or less, the standard design approaches used to design OTAs, such as input transconductor implemented through a conventional differential pair with a tail current generator, and cascoding to increase gain, are no longer applicable, forcing CMOS designers to search for different paradigms. Moreover, the limited supply voltage requires to fully exploit the available dynamic range, thus making solutions with a rail-to-rail input common mode range (ICMR) mandatory.

The absence of the tail current generator makes achieving a stable biasing and a high common mode rejection ratio (CMRR) a very critical task. Body biasing [8] has been proposed in the literature as a substitute for the tail generator, but the reduced supply voltage, together with the limited body transconductance gain, makes it impossible to reach a stable bias point under process, supply voltage and temperature (PVT) variations through the body terminal [9]. This strongly limits the applicability of inverter-based solutions such as [10] and [11] and also those which exploits body-biasing [12]. Most ULV OTAs in the literature exploit body driving (the input signal is applied to the body terminal) [9], [13]–[21], complementary n-type and p-type pseudo-differential transconductors [22] or floating-gate and quasi-floating-gate solutions [23]. CMRR is improved by the use of common mode feedback (CMFB) loops, common mode feedforward (CMFF) [9], [24], by optimizing the topology of differential-to-single-ended converter (D2S) stages [21] or by optimizing the OTA architecture [20]; gain can be improved by exploiting positive feedback [15], [18] or by using additional gain stages [14], [16], [17], [19].

In this paper we present a ULV body-driven three-stage rail-to-rail OTA with high DC gain and CMRR. It features an architecture with two fully differential stages followed by a D2S, to take advantage of CMFB loops to accurately set bias points and allow improved robustness to PVT variations. The OTA has been designed referring to a 130nm CMOS technology from STMicroelectroincs and measured results on the fabricated test chip are presented.

The paper is structured as follows. Section II introduces the OTA architecture and presents the analytical computation of main performance parameters. Section III introduces the design of the OTA in a 130nm CMOS process and the results of the simulations. Section IV presents the results of measurements on the test chip. A comparison against other ULV OTAs taken from the literature is reported in section V and some conclusion are drawn in Section VI.

II. OTA ARCHITECTURE

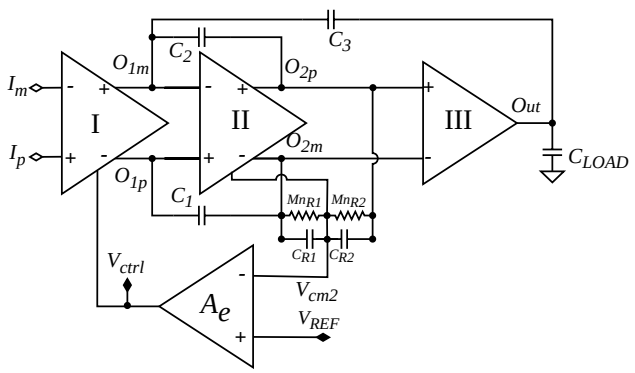

FIGURE 1: Block scheme of the proposed OTA architecture.

The architecture of the proposed OTA is reported in Fig. 1. The first and second stages are fully differential amplifiers with CMFB, whereas the third stage implements a differential to single ended converter (D2S). The detailed schematic of the proposed OTA is shown in Fig. 2. The body-driven complementary pseudo-differential input stage is exploited to double the transconductance gain and allow rail-to-rail ICMR with bias currents accurately set through gate terminals. The second stage is a gate-driven, complementary pseudo-differential stage with an high DC gain and a local CMFB. A further CMFB reads the common mode output voltage of the second stage, and controls the gates of the NMOS devices in the first stage. The third stage implements the differential-to-single-ended conversion through a body-driven complementary pseudo-differential pair and a gate-driven current mirror.

The first stage has to be bulk-driven in order to guarantee a rail-to-rail ICMR, whereas the second stage is gate-driven to enhance the overall DC gain. Since, in the proposed architecture, the third stage has to perform the differential-to-single-ended conversion, we have chosen to implement it as bulk-driven at the input to allow the implementation of a gate-driven current mirror at the output.

A Reverse Nested Miller (RNM) compensation scheme suitable for the proposed architecture in which the D2S is the last stage, and implemented through capacitors C_1, C_2 and C_3 is exploited to guarantee the stability of the OTA with adequate phase margin.

Since the proposed OTA requires to drive independently the bulk terminal of NMOS and PMOS devices, it requires a triple well CMOS process. However, since nowadays most of the CMOS technologies allow the body terminals to be independently driven, we do not consider this point a limitation.

More details about the different OTA stages are given in the following subsections.

A. FIRST STAGE

The first stage of the architecture is composed by transistors $Mp_{1,2}$ and $Mn_{1,2}$ which are body driven and gate biased. More specifically, well defined bias currents are set through the bias voltage Vbg, generated from a reference current injected into a diode-connected PMOS device, and applied to the PMOS devices $Mp_{1,2}$, thus mirroring the reference current (see Fig. 2) in order to gurantee good robustness under PVT variations. The CMFB loop is closed by controlling the gates of MNOS devices $Mn_{1,2}$ in order to set the common mode voltage, reduce the output offset voltage and enhance the CMRR performance of the whole OTA.

The differential gain of the first stage can be expressed as:

$$Av_{d1} = \frac{G_{mb_1}}{G_{o_1}} \cdot \frac{1}{1 + s\,\frac{C_{o_1}}{G_{o_1}}} \tag{1}$$

where

$$G_{mb_1} = g_{mb_{n1,2}} + g_{mb_{p1,2}} \tag{2}$$

$$G_{o_1} = g_{ds_{n1,2}} + g_{ds_{p1,2}} \tag{3}$$

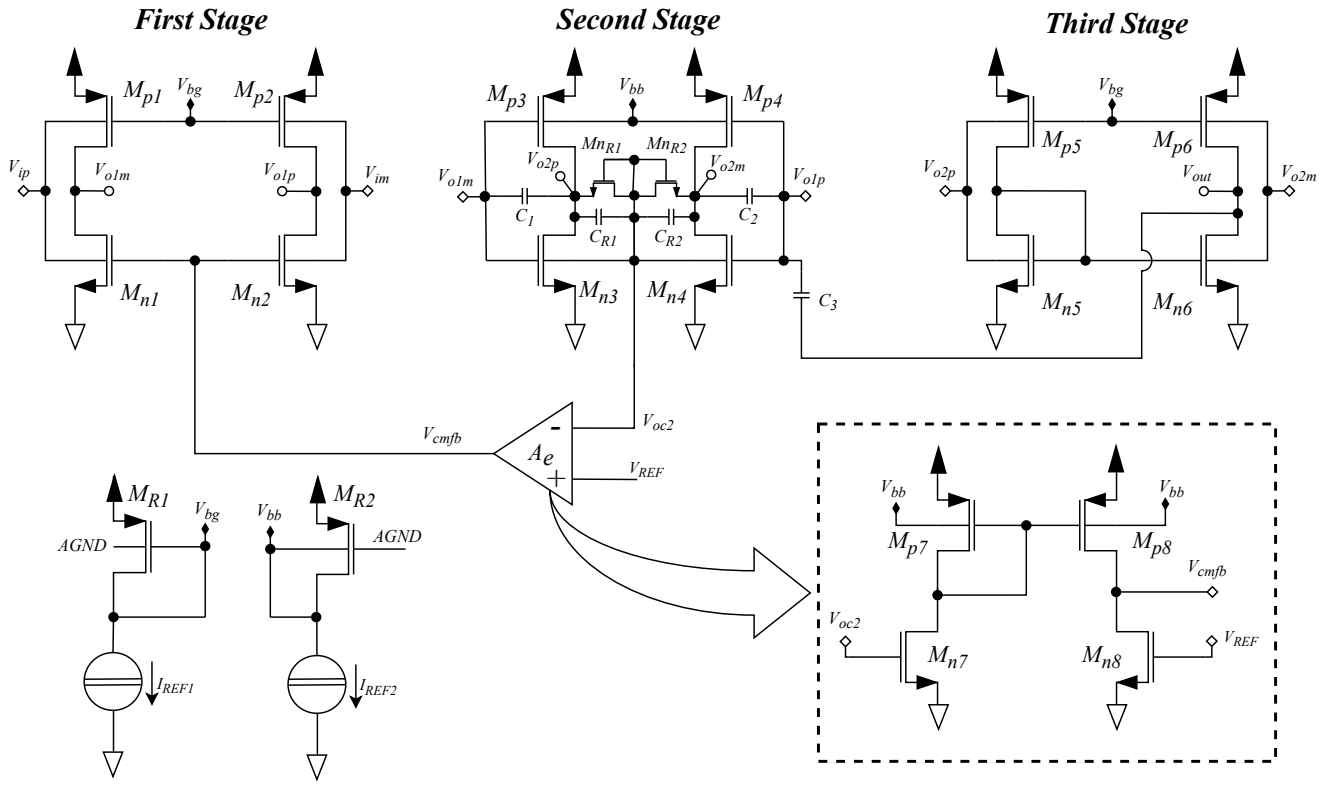

FIGURE 2: Detailed schematic of the proposed OTA.

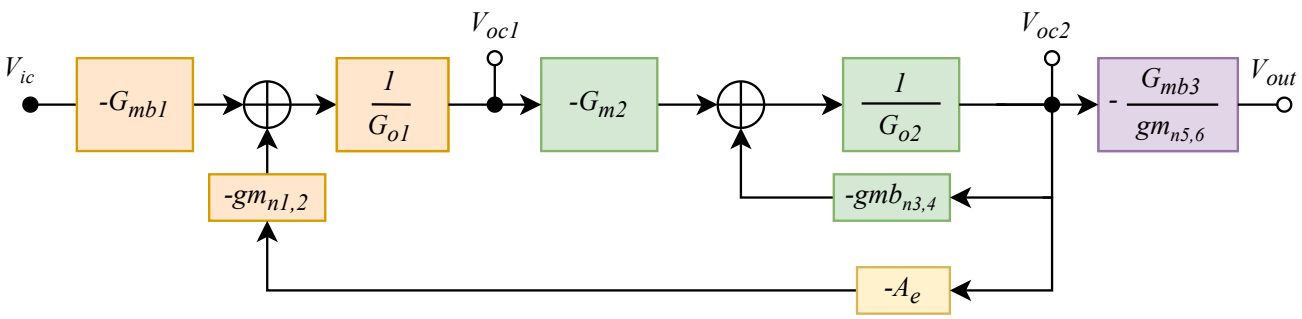

FIGURE 3: Linearized block scheme of the OTA for the common mode gain computation: orange color corresponds to the first stage transistors, green color corresponds to the second stage transistors, purple color corresponds to the third stage common mode rejection. The error amplifier has been represented in yellow color.

and C_{o_1} is the capacitance seen at the output nodes of the first stage, which can be expressed as:

$$C_{o_1} = C_{gd_{n1,2}} + C_{gd_{p1,2}} + C_{in_2} + C_{bd_{n1,2}} + C_{bd_{p1,2}} \quad (4)$$

where C_{in_2} is the input capacitance of the second stage. Usual notation has been used for small signal parameters of MOS transistors.

The common mode gain of the first stage (without considering the effect of the CMFB loop) is given by the following relation:

$$Av_{c1} = \frac{G_{mb_1}}{G_{o_1}} \quad (5)$$

B. SECOND STAGE

The second stage of the OTA is composed by transistors $Mp_{3,4}$ and $Mn_{3,4}$ which are gate driven and body biased in order to boost the gain-bandwidth product of the whole architecture. In addition, a local CMFB (LCMFB) implemented by the two pseudoresistors $M_{N_{R1,2}}$ is exploited to accurately set the output static voltages of the second stage in spite of PVT variations, and at the same time to improve its CMRR performance. In fact, since bias currents of $Mp_{3,4}$ are set through their body terminals, the biasing of the second stage is somewhat sensitive to PVT variations, and the adoption of the LCMFB allows to improve the robustness of the second

stage.

The differential gain of the second stage can be expressed as:

$$Av_{d2} = \frac{G_{m_2}}{G_{o_2} + g_{R_{1,2}}} \cdot \frac{1}{1 + s\,\frac{C_{o_2}}{G_{o_2} + g_{R_{1,2}}}} \quad (6)$$

where

$$G_{m_2} = g_{m_{n3,4}} + g_{m_{p3,4}} \quad (7)$$

$$G_{o_2} = g_{ds_{n3,4}} + g_{ds_{p3,4}} \quad (8)$$

$g_{R_{1,2}}$ is the equivalent conductance of the two pseudresistors $M_{N_{R1,2}}$, and C_{o_2} is the capacitance seen at the output nodes of the second stage, which can be written as:

$$C_{o_2} = C_{gd_{n3,4}} + C_{gd_{p3,4}} + C_{in_3} + C_{bd_{n3,4}} + C_{bd_{p3,4}} + C_{R_{1,2}} \quad (9)$$

where C_{in_3} is the input capacitance of the third stage.

The common mode gain of the second stage (considering only the effect of the LCMFB) can be expressed as follows:

$$Av_{c2} = \frac{G_{m_2}}{G_{o_2} + g_{mb_{n3,4}}} \quad (10)$$

C. THIRD STAGE

The third stage of the OTA is a differential to single-ended converter made up of transistors $Mp_{5,6}$ and $Mn_{5,6}$, which are body driven and gate biased, in order to properly set the bias point and thus attain stable phase margin and gain-bandwidth-product (GBW) under PVT variations. The differential to single-ended conversion is performed by the gate-driven current mirror composed by M_{n_5} and M_{n_6}.

The differential gain of the third stage can be expressed as:

$$Av_{d3} = \frac{G_{mb_3}}{G_{o_3}} \frac{1}{1 + s\,\frac{C_L + C_{o_3}}{G_{o_3}}} \quad (11)$$

where

$$G_{mb_3} = g_{mb_{n5,6}} + g_{mb_{p5,6}} \quad (12)$$

$$G_{o_3} = g_{ds_{n5,6}} + g_{ds_{p5,6}} \quad (13)$$

C_{o_3} is the capacitance seen at the output nodes of the third stage, which can be expressed as:

$$C_{o_3} = C_{gd_{n5,6}} + C_{gd_{p5,6}} + C_{bd_{n5,6}} + C_{bd_{p5,6}} \quad (14)$$

and C_L is the load capacitance at the output node of the OTA. The common mode gain of this stage can be written as:

$$Av_{c_3} = \frac{G_{mb_3}}{G_{o_3}} \cdot \frac{G_{o_3}}{g_{m_{n5,6}} + G_{o_3}} \approx \frac{G_{mb_3}}{g_{m_{n5,6}}} \quad (15)$$

D. ANALYSIS OF THE CMFB LOOPS AND CMRR

The proposed OTA architecture exploits two CMFB loops which both sense the common mode output voltage of the second stage through the pseudoresistors $M_{n_{R1,2}}$.

The LCMFB is closed through the body terminals of $M_{n_{3,4}}$ and is needed to guarantee proper biasing of the second stage when considering the current offset due to threshold voltage variations of PMOS and NMOS devices under process and temperature variations. Its main effect is to reduce the common-mode output impedance of the second stage, thus extending the linear range of the main CMFB, which allows to strongly improve the CMRR of the OTA. In detail, the estimation of the output common mode voltage of the second stage V_{oc2} provided by $M_{n_{R1,2}}$ is sent to the error amplifier Ae, composed by $M_{p_{7,8}}$ and $M_{n_{7,8}}$, which compares V_{oc2} with a reference voltage V_{REF} and then adjusts the gate voltages of $M_{n_{1,2}}$ in order to improve CMRR performance and increase the accuracy of the DC operating point of the second stage under PVT variations. It has to be noted that $M_{n_{R1,2}}$ implement a voltage divider used to extract the common mode voltage at the output of the second stage and provide an estimation of the common-mode voltage which is insensitive to PVT variations.

The error amplifier Ae is implemented through a gate-driven body-biased stage depicted in Fig. 2 whose gain is:

$$A_e = \frac{g_{m_{n7,8}}}{g_{ds_{p7,8}} + g_{ds_{n7,8}}} \quad (16)$$

The linearized block scheme of the OTA architecture adopted for small signal analysis is depicted in Fig. 3, for what concerns the common-mode behavior. Referring to the block scheme in Fig. 3, the common-mode voltage $V_{oc1} = \frac{V_{o1p} + V_{o1m}}{2}$ at the output of the first stage as a function of the input common-mode voltage $V_{ic} = \frac{V_{ip} + V_{im}}{2}$ can be easily computed as:

$$\frac{V_{oc1}}{V_{ic}} = -\frac{G_{mb_1}}{\left(\frac{G_{m2}}{g_{mb_{n3,4}}}\right) g_{m_{n1,2}} A_e} \quad (17)$$

the common-mode voltage $V_{oc2} = \frac{V_{o2p} + V_{o2m}}{2}$ at the output of the second stage as a function of the input common-mode voltage V_{ic} can be expressed as:

$$\frac{V_{oc2}}{V_{ic}} = \frac{Av_{c1} Av_{c2}}{1 + A_e Av_{c2} \left(\frac{g_{m_{n1,2}}}{G_{o_1}}\right)} \quad (18)$$

Finally, the common mode gain of the whole OTA can be expressed at node V_{out} as:

$$A_{V_{C_{tot}}} = \frac{V_{out}}{V_{ic}} \approx -\frac{G_{mb_1} Av_{c3}}{g_{m_{n1,2}} A_e} \quad (19)$$

In conclusion, by considering the gain of the error amplifier expressed in Eq. 16 the common mode gain of the architecture can be derived:

$$A_{V_{C_{tot}}} \approx -\frac{G_{mb_1}}{g_{m_{n1,2}}} \cdot \frac{G_{mb_3}}{g_{m_{n5,6}}} \cdot \frac{g_{ds_{n7,8}} + g_{ds_{p7,8}}}{g_{m_{n7,8}}} \quad (20)$$

The differential gain of the OTA can be derived by multiplying the differential gains of the three-stages as follows:

$$A_{V_{D_{tot}}} = \prod_{i=1}^{3} A_{V_{D_i}} \approx \frac{G_{mb_1}}{G_{o_1}} \cdot \frac{G_{m_2}}{G_{o_2} + g_{R_{1,2}}} \cdot \frac{G_{mb_3}}{G_{o_3}} \quad (21)$$

Finally, Eq. 20 and Eq. 21 can be used to derive the expression of CMRR according to its definition:

$$CMRR = \frac{A_{V_{D_{tot}}}}{A_{V_{C_{tot}}}} \approx \frac{g_{m_{n_{1,2}}}}{G_{o_1}} \cdot \frac{G_{m_2}}{G_{o_2} + g_{R_{1,2}}} \cdot \frac{g_{m_{n_{5,6}}}}{G_{o_3}} \cdot A_e \quad (22)$$

From Eq. 22 it is evident that the proposed OTA exhibits a very high CMRR (in the order of A_v^4) in typical conditions. However, it has to be noted that this result has been obtained without considering the effect of mismatches, which can result in a strong degradation of CMRR performance.

E. ANALYSIS OF OUTPUT OFFSET UNDER MISMATCH VARIATIONS

In this section we analyze the output offset voltage of the proposed OTA considering the current offset due to threshold voltage variations of PMOS and NMOS devices under process and temperature variations. In detail, the block scheme adopted for the computation of the output offset voltage is depicted in Fig. 4. The three-stages are highlighted in different colors: the first stage is denoted in orange, the second stage in green and finally, the third stage in purple. For each stage we consider that the currents drawn by the $NMOS$ and $PMOS$ transistors in each branch, due to process and temperature variations, are not perfectly equal to each other and this generates a DC offset current. This offset current, multiplied by the output resistance of the $i-th$ stage, produces a DC offset voltage (i. e. a variation of the static output voltage with respect to the analog ground). In the following of this analysis, we denote the output offset current of each stage with I_{off_i}.

Then, referring to the block scheme of Fig. 4 the output offset voltage of the whole OTA can be computed as:

$$V_{oDC} \approx \frac{I_{off_3}}{G_{o_3}} - \frac{I_{off_2}}{Av_{x_1}} \cdot \frac{Av_{x_3}}{A_e G_{m2}} + \frac{I_{off_1} \cdot Av_{x_3}}{A_e g_{m_{n_{1,2}}}} \quad (23)$$

where

$$Av_{x_1} = \frac{g_{m_{n_{1,2}}}}{G_{o_1}} \quad (24)$$

$$Av_{x_3} = \frac{g_{m_{n_{5,6}}}}{G_{mb_3}} \quad (25)$$

Now, expressing the offset currents and the DC output voltage in terms of their mean value and standard deviation as follows:

$$I_{off_i} = \mu_{I_i} + \sigma_{I_i}, i = 1, 2, 3 \quad (26)$$

$$V_{oDC} = \mu_V + \sigma_V \quad (27)$$

and assuming both μ_{I_i} and μ_V approximately equal to 0, we can compute the standard deviation of the DC output voltage as follows:

$$\sigma_V^2 = \frac{Av_{x_3}^2}{A_e^2 Av_{x_1}^2} \cdot \left(\frac{\sigma_{I_1}^2}{G_{o_1}^2} + \frac{\sigma_{I_2}^2}{G_{m2}^2}\right) + \frac{\sigma_{I_3}^2}{G_{o_3}^2} \quad (28)$$

By looking at Eq. 28, it can be observed that, if compared with the solution presented in [16], the proposed OTA architecture allows to set the static node voltages and DC bias points with higher accuracy and less dependence on mismatch variations. In fact, since the offset voltage of the first and second stages are rejected by feedback loops, the bias points are stable under mismatch variations, resulting in very stable GBW and P_D.

III. OTA DESIGN AND SIMULATION RESULTS

The proposed three-stage OTA has been designed and implemented in a 130nm CMOS process from STMicroelectronics. Table 1 reports the dimensions and bias currents of the transistors implementing the architecture in Fig. 2. The bias voltages V_{bg} and V_{bb} in Fig. 2 are both set at 150mV, and the reference voltage V_{REF} is 150mV too. Compensation capacitors C_1, C_2 and C_3 are set to 100fF, 100fF and 1.5pF respectively, whereas C_{R1} and C_{R2} are 40fF. The design has been carried out within the Cadence Virtuoso environment for a nominal supply voltage V_{DD} of 0.3V and assuming a load capacitance of 35pF at the output.

Transistor	Stage	Width [μm]	Length [μm]	I_{bias} [nA]
$M_{n1,2}$	1	0.375	3	5
$M_{p1,2}$	1	4.465	1	5
$M_{n3,4}$	2	0.375	3	5
$M_{p3,4}$	2	4.465	1	5
$M_{n5,6}$	3	3	3	40
$M_{p5,6}$	3	35.72	1	40
$M_{n7,8}$	3	0.375	3	40
$M_{p7,8}$	3	4.465	1	40
$M_{nR1,2}$	3	0.15	1.5	-

TABLE 1: Transistors' sizing and bias currents

The differential transfer function (magnitude and phase) of the OTA is reported in Fig. 5, showing a phase margin of about 58.27° and a gain-bandwidth product of about 10kHz.

Fig. 6 reports the CMRR frequency response in typical conditions showing a low frequency value in excess of 136dB. However, it has to be noted that this good result is obtained without considering the effect of mismatches which, as will be shown in the following of this section, strongly impact CMRR performance.

Fig. 7 shows the DC transfer characteristic of the proposed OTA in unity-gain configuration, highlighting the rail-to-rail ICMR and the high accuracy of the voltage gain.

The input referred noise of the proposed OTA is reported in Fig. 8: the white noise at 1 kHz is about 2.86 $\mu V/\sqrt{Hz}$.

The transient response of the OTA in unity-gain configuration to a rail-to-rail input step is depicted in Fig. 9.

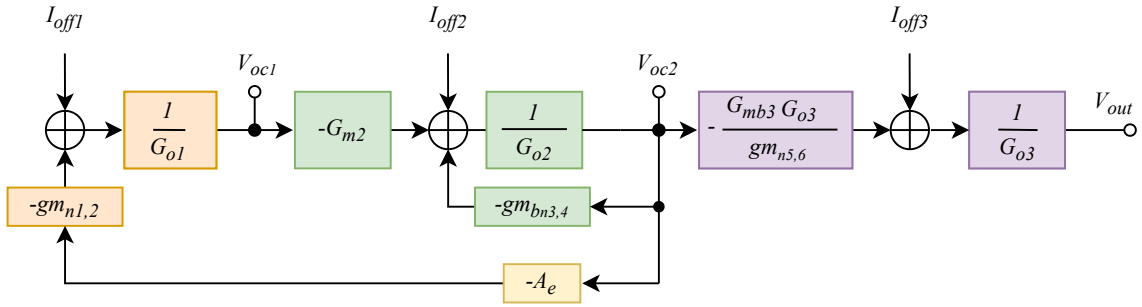

FIGURE 4: Block scheme for the computation of the output offset voltage of the proposed OTA: I_{off_i} denotes the $i-th$ stage offset current given by mismatch variations between $NMOS$ and $PMOS$.

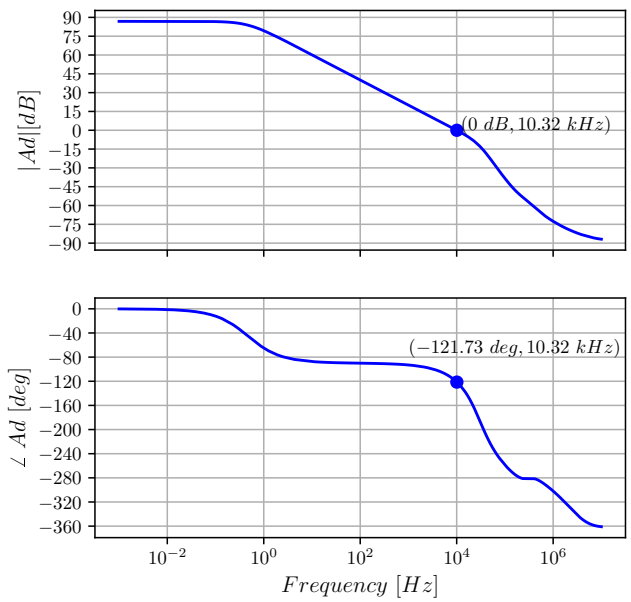

FIGURE 5: Magnitude and Phase of the differential gain of the proposed three-stage OTA.

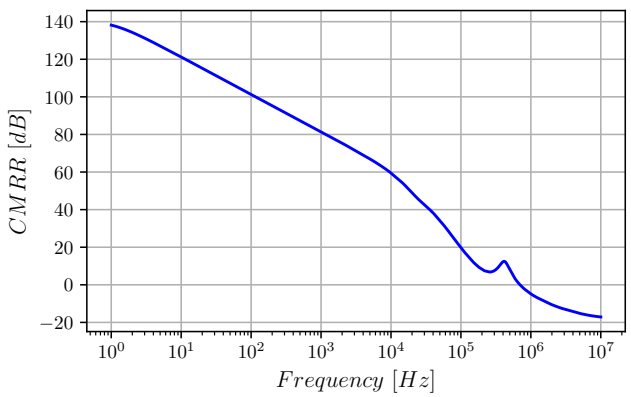

FIGURE 6: CMRR of the proposed three-stage OTA.

The amplifier with respect to an input step of amplitude of 220 mV shows positive and negative slew rate (SR_+ and

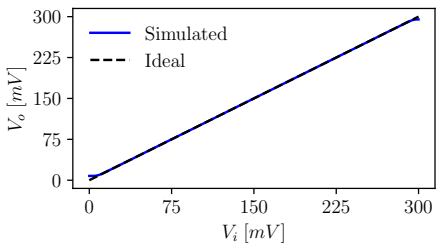

FIGURE 7: DC transfer characteristic of the proposed OTA in unity-gain configuration.

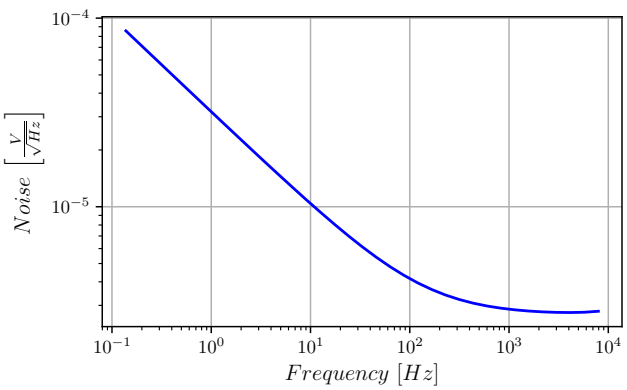

FIGURE 8: Input referred noise of the proposed three-stage OTA.

SR_-) equal to about 2.5 V/ms and 5 V/ms respectively, highlighting an average slew rate of about 3.75 V/ms.

Sinusoidal inputs at different amplitudes and with a frequency of 100 Hz have been used to excite the OTA in unity-gain configuration and evaluate the total harmonic distortion (THD). The OTA exhibits a very good THD (0.2%) for an input signal amplitude of about 100mV. THD is good also for higher amplitudes, in fact it is about (0.36%) for an input amplitude as high as 220mV (i. e. about the 75% of the rail-to-rail swing).

Extensive parametric and Monte Carlo simulations have been carried out in order to assess the robustness of the

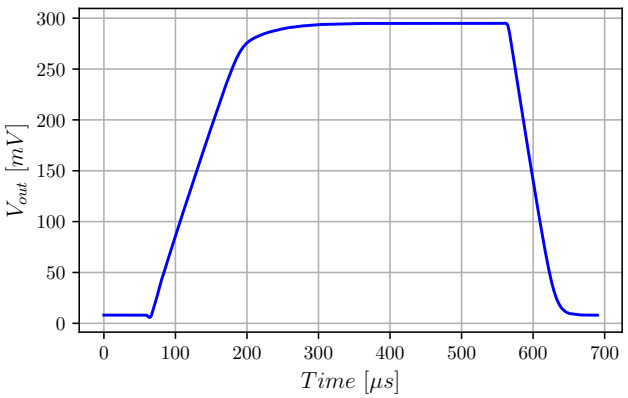

FIGURE 9: Transient response of the OTA in unity-gain configuration to a rail-to-rail input step.

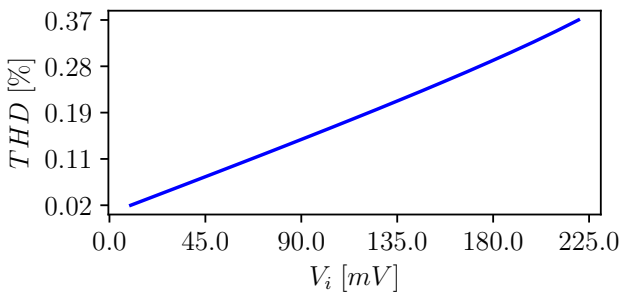

FIGURE 10: Total Harmonic Distortion in percentage vs input signal amplitude at a frequency of 100Hz.

amplifier to PVT and mismatch variations, referring both to open-loop and closed-loop simulation testbenches.

Main OTA performance parameters have been evaluated in the different process corners and considering a +/-10% variation of the supply voltage and a temperature range from 0 to 80 °C, and results are summarized in Tables 2 and 3 respectively. Both small signal and large signal performance of the proposed OTA resulted to be very robust with respect to PVT variations. The analysis in Table 2, reports also the offset voltage of the output of each stage, denoted as $Offset_i$ and, as it can be observed, in the whole range of variations they result very stable (offset voltages are all very close to 0). This behavior is due to the explicit bias reference voltage in the error amplifier circuit of the CMFB and also to the local CMFB of the second stage.

Table 4 summarizes the results of 200 mismatch Monte Carlo iterations, showing how most of the OTA performance parameters are only slightly sensitive to mismatch variations. This is not true for CMRR and output offset voltage which are the most sensitive parameters. In particular the mean value of the CMRR under mismatch variations is much lower than the nominal value, in which al signal paths are assumed identical to each other. However, it has to be noted that we have used relatively small transistors to keep the area low, and that the mean value of the CMRR under mismatch variations can be improved by increasing the area of MOS transistors according to the Pelgrom law [25].

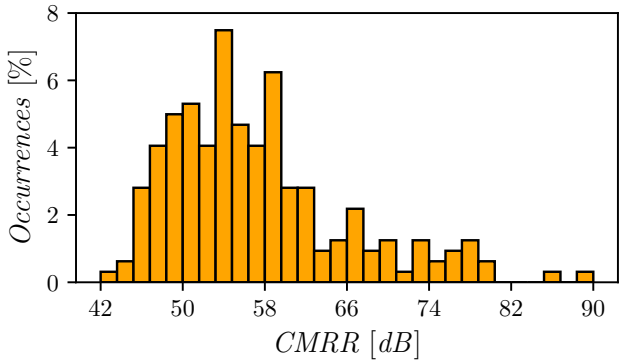

FIGURE 11: Histrogram of the CMRR over 200 mismatch Monte Carlo Iterations.

Fig. 11 shows the histrogram of the CMRR obtained from 200 mismatch Monte Carlo Iterations and confirms the strong impact of mismatch variations at ULV conditions.

IV. MEASURED RESULTS

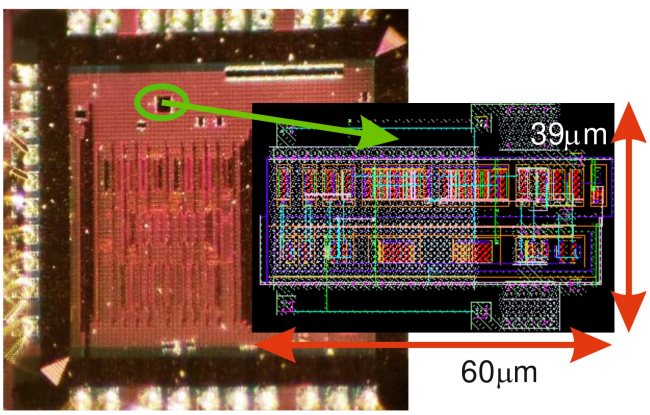

FIGURE 12: Chip microphotograph.

The microphotograph of the 130nm fabricated test-chip and the detail with the layout of the proposed three-stage OTA are reported in Fig. 12. The area footprint of the proposed OTA is about 60x39 μm^2.

The measured frequency response ot the three-stage OTA in unity-gain configuration is reported in Fig. 13. The measured GBW is 9.8KHz and results in very good agreement with the simulated value. Fig. 14 reports the measured transient response to a 220mV input step. The measured SR_+ and SR_- are 2.5 V/ms and 5 V/ms respectively, and are in good agreement with simulations.

V. COMPARISON WITH LITERATURE

The main performance parameters of the proposed OTA are reported in Table 5 and compared with other ULV OTAs

	Nominal	FF	SS	FS	SF
Av_D $[dB]$	86.83	85.67	87.71	85.37	87.63
GBW $[kHz]$	10.32	10.2	10.44	10.41	10.24
$m\varphi$ $[deg]$	58.27	62.08	49.53	61.41	55.88
Av_c $[dB]$	-49.68	-32.38	-34.13	-37.15	-41.2
$CMRR$ $[dB]$	136.51	118.05	121.84	122.55	128.83
$PSRR$ $[dB]$	100.22	93.44	106.45	95.23	115.68
P_D $[nW]$	33.73n	38.39n	31.09n	38.68n	30.81n
Offset$_1$ $[mV]$	-5.74	-11.06	2.36	-16.66	9.45
Offset$_2$ $[mV]$	-9.029m	-3.743m	-14.94m	-13.59m	-5.152m
Offset$_3$ $[uV]$	-478.2m	-1.759	425.4m	-1.739	362.9
SR_+ $[V/ms]$	2.315	2.263	2.317	2.418	2.173
SR_- $[V/ms]$	5.135	4.854	5.5	5.261	5.029
SR_{avg} $[V/ms]$	3.725	3.559	3.909	3.839	3.601

TABLE 2: Performance of the OTA in the different process corners

	Nominal	Voltage		Temperature	
V_{DD} $[mV]$	300	270	330	300	300
T $[C]$	27	27	27	0	80
Av_D $[dB]$	86.83	81.85	90.83	88.02	82.73
GBW $[kHz]$	10.32	10.31	10.28	10.15	10.14
$m\varphi$ $[deg]$	58.27	51.16	62.32	50.07	63.35
Av_c $[dB]$	-49.68	-39.85	-35.75	-35.11	-28.05
$CMRR$ $[dB]$	136.51	121.70	126.58	123.13	110.78
$PSRR$ $[dB]$	100.22	107.47	100.98	105.14	83.03
P_D $[nW]$	33.73	27.31	42.12	30.75	42.54
Offset$_1$ $[mV]$	-5.73	1.26	-10.88	-5.606m	-5.606m
Offset$_2$ $[mV]$	-9.03	-8.19	-10.02	-19.87	3.992
Offset$_3$ $[mV]$	-478.2u	486.2u	-831.3u	-6.59	-6.58
SR_+ $[V/ms]$	2.315	2.064	2.516	2.297	2.185
SR_- $[V/ms]$	5.135	4.927	4.741	5.581	4.647
SR_{avg} $[V/ms]$	3.725	3.496	3.628	3.939	3.416

TABLE 3: Performance of the OTA under supply voltage and temperature variations

	Nominal	μ	σ
A_d [dB]	86.11	85.81	0.64
GBW [kHz]	10.32	10.81	1.12
$m\varphi$ [deg]	58.27	58.05	2.21
SR_{avg} [V/ms]	3.74	3.36	0.45
$CMRR$ [dB]	136.11	57.80	8.73
$PSRR$ [dB]	100.22	46.59	7.85
P_D [nW]	30.00	30.12	4.63
Offset$_1$ $[mV]$	-5.73	-5.71	2.05
Offset$_2$ $[mV]$	-9.03	-6.11	7.46
Offset$_3$ $[mV]$	-478.2u	0.05	11.82

TABLE 4: Monte Carlo mismatch simulations.

taken from the literature. The proposed three-stage OTA results in better performance in terms of FOM_S, linearity and also Silicon area with respect to [16] which was the most performant three-stage OTA. Furthermore, we want to remark that the proposed architecture results in lower area footprint, with respect to both two-stage and three-stage OTAs in the comparison table.

VI. CONCLUSION

In this work we have presented a 0.3V ULV three-stage OTA with high DC gain and rail-to-rail ICMR. The three-stage OTA occupies an area of about $0.002mm^2$ and its power consumption is around 30nW at the supply voltage of 0.3V. With a load capacitance of 35pF, the OTA exhibits a DC gain and a unity-gain frequency of about 85dB and 10kHz, respectively. The OTA performances are remarkably stable with respect to PVT variations and mismatches. Results reported in tables 2 and 3 show that the variation of GBW with PVT is less than 3%, and in general highlight the very good robustness of the proposed solution to PVT variations. Compared with the state of the art, the proposed OTA exhibits very good overall performance being the most compact between the body-driven three-stage OTAs.

	This Work	[26]	[14]	[27]*	[17]	[16]	[28]	[11]	[15]
Year	2023	2022	2015	2021	2020	2020	2020	2019	2018
Tech [nm]	130	180	65	130	65	180	180	130	180
V_{DD} [V]	0.3	0.4	0.35	0.3	0.25	0.3	0.3	0.3	0.3
A_d [dB]	86.83	60	43	40.80	70	98.1	64.7	49.8	65.8
C_L [pF]	35	15	3	40	15	30	30	2	20
GBW [kHz]	10.32	7	3.6k	18.65	9.5	3.1	2.96	9100	2.78
mφ [°]	58.27	60.2	56	51.93	89.9	54	52	76	61
SRavg [V/ms]	3.74	79	5.6k	21.60	2	9.1	4.15	3.8	7.12
THD [%]	0.2	-	0.6	1.4	-	0.49	1	-	1
% input swing	73	-	90	80	-	83.33	85	-	93.33
CMRR [dB]	57.80 ‡	85.40	46	67.49	62.5	60 ‡	110	-	72
PSRR [dB]	46.59 ‡	76.30	35	45	38	61	56	-	62
IRN [μV/$\sqrt{\text{Hz}}$]	2.86	0.31	0.93	2.12	-	1.8	1.6	0.035	1.85
@freq [Hz]	10k	1k	10k	1k	-	-	-	100k	36
Pd [nW]	33.73	24	17k	73	26	13	12.6	1800	15.4
Mode	BD	BD	GD	BD	BD	BD	BD	GD	BD
FOM_S $[MHz\ pF/mW]$	10.70k	4.38k	635.29	10.20k	5.48k	7.15k	7.05k	10.11k	3.61k
FOM_L $[V\ pF/\mu W]$	3.88k	49.38k	988.24	11.82k	1.15k	21.00k	9.88k	4.67k	9.25k
$Area$ $[\mu m^2]$	2340	7900	5000	3600	2000	9800	8500	-	8200

*Simulated; ‡Given by Monte Carlo Simulations
BD=Body driven; GD=Gate driven; DIG=Digital

TABLE 5: Comparison with the literature.

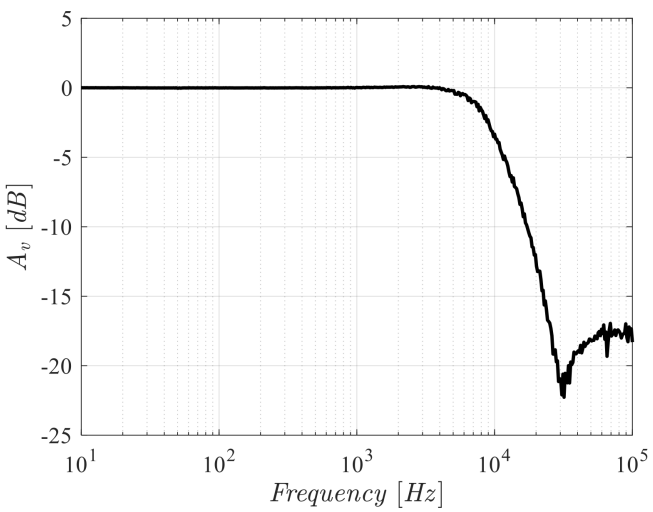

FIGURE 13: Measured closed-loop AC response (GBW = 9.8 kHz)

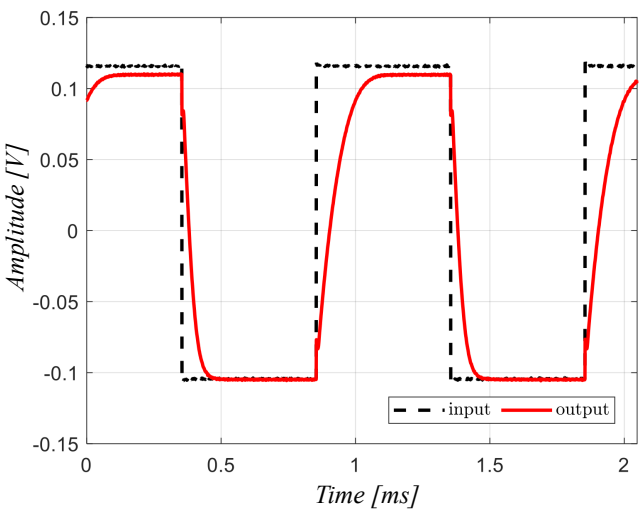

FIGURE 14: Measured transient step response (SR_+ = 2.5 V/ms, SR_- = 5 V/ms.

REFERENCES

[1] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec. 2005.

[2] F. Khateb, S. B. A. Dabbous, and S. Vlassis, "A survey of non-conventional techniques for low-voltage low-power analog circuit design," *Radioengineering*, vol. 22, no. 2, pp. 415–427, Jun. 2013.

[3] M. Grossi, "Energy harvesting strategies for wireless sensor networks and mobile devices: A review," *Electronics*, vol. 10, no. 6, p. 661, Mar. 2021.

[4] P. R. Kinget, "Scaling analog circuits into deep nanoscale CMOS: Obstacles and ways to overcome them," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, Sep. 2015, pp. 1–8.

[5] B. Xu, S. Li, N. Sun, and D. Z. Pan, "A scaling compatible, synthesis friendly VCO-based delta-sigma ADC design and synthesis methodology," in *2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC)*. IEEE, Jun. 2017, pp. 1–6.

[6] S. Weaver, B. Hershberg, and U.-K. Moon, "Digitally synthesized stochastic flash ADC using only standard digital cells," *IEEE Trans. Circ. Syst. I*, vol. 61, no. 1, pp. 84–91, Jan. 2014.

[7] P. Toledo, R. Rubino, F. Musolino, and P. Crovetti, "Re-thinking analog integrated circuits in digital terms: A new design concept for the IoT era," *IEEE Trans. Circuits Syst. II*, vol. 68, no. 3, pp. 816–822, Mar. 2021.

[8] A. D. Grasso and S. Pennisi, "Ultra-low power amplifiers for IoT nodes," in *2018 25th IEEE International Conference on Electronics, Circuits and*

Systems (ICECS). IEEE, Dec. 2018, pp. 497–500.

[9] F. Centurelli, R. Della Sala, G. Scotti, and A. Trifiletti, "A 0.3 V, rail-to-rail, ultralow-power, non-tailed, body-driven, sub-threshold amplifier," *Appl. Sci.*, vol. 11, no. 6, p. 2528, Mar. 2021.

[10] J. Liu, B. Park, M. Guzman, A. Fahmy, T. Kim, and N. Maghari, "A fully synthesized 77-dB SFDR reprogrammable SRMC filter using digital standard cells," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 26, no. 6, pp. 1126–1138, Jun. 2018.

[11] L. Lv, X. Zhou, Z. Qiao, and Q. Li, "Inverter-based subthreshold amplifier techniques and their application in 0.3-V $\Delta\Sigma$ -modulators," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1436–1445, May 2019.

[12] H. Faraji Baghtash, "A 0.4 V, body-driven, fully differential, tail-less OTA based on current push-pull," *Microelectron. J.*, vol. 99, p. 104768, May 2020.

[13] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process," *IEEE Trans. Circ. Syst. I*, vol. 61, no. 6, pp. 1609–1617, Jun. 2014.

[14] O. Abdelfattah, G. W. Roberts, I. Shih, and Y.-C. Shih, "An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail-to-rail input range," *IEEE Trans. Circ. Syst. I*, vol. 62, no. 10, pp. 2380–2390, Oct. 2015.

[15] T. Kulej and F. Khateb, "Design and implementation of sub 0.5-V OTAs in 0.18-μm CMOS," *Int. J. Circuit Theory Appl.*, vol. 46, no. 6, pp. 1129–1143, Jun. 2018.

[16] ——, "A 0.3-V 98-dB rail-to-rail OTA in 0.18 μ m CMOS," *IEEE Access*, vol. 8, pp. 27 459–27 467, Feb. 2020.

[17] K.-C. Woo and B.-D. Yang, "A 0.25-V rail-to-rail three-stage OTA with an enhanced DC gain," *IEEE Trans. Circuits Syst. II*, vol. 67, no. 7, pp. 1179–1183, Jul. 2020.

[18] N. Deo, T. Sharan, and T. Dubey, "Subthreshold biased enhanced bulk-driven double recycling current mirror OTA," *Analog Integr. Circ. Sig. Process.*, vol. 105, no. 2, pp. 229–242, Nov. 2020.

[19] S. Dong, W. Wang, and X. Tong, "A 0.25-V 90 dB PVT-stabilized four-stage OTA with linear Q-factor modulation and fast slew-rate enhancement for ultra-low supply ADCs," *AEU Int. J. Electron. Commun.*, vol. 144, p. 154044, Feb. 2022.

[20] F. Centurelli, R. Della Sala, P. Monsurró, G. Scotti, and A. Trifiletti, "A tree-based architecture for high-performance ultra-low-voltage amplifiers," *J. Low Power Electron. Appl.*, vol. 12, no. 1, p. 12, Feb. 2022.

[21] R. Della Sala, F. Centurelli, and G. Scotti, "Enabling ULV fully synthesizable analog circuits: the BA cell, a standard-cell-based building block for analog design," *IEEE Trans. Circuits Syst. II*, p. 1, Aug. 2022.

[22] Z. Qin, A. Tanaka, N. Takaya, and H. Yoshizawa, "0.5-V 70-nW rail-to-rail operational amplifier using a cross-coupled output stage," *IEEE Trans. Circuits Syst. II*, vol. 63, no. 11, pp. 1009–1013, Nov. 2016.

[23] J. M. A. Miguel, A. J. Lopez-Martin, L. Acosta, J. Ramirez-Angulo, and R. G. Carvajal, "Using floating gate and quasi-floating gate techniques for rail-to-rail tunable CMOS transconductor design," *IEEE Trans. Circ. Syst. I*, vol. 58, no. 7, pp. 1604–1614, Jul. 2011.

[24] A. N. Mohieldin, E. Sanchez-Sinencio, and J. Silva-Martinez, "A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 663–668, Apr. 2003.

[25] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of mos transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[26] M. Akbari, S. M. Hussein, Y. Hashim, and K.-T. Tang, "0.4-V Tail-Less Quasi-Two-Stage OTA Using a Novel Self-Biasing Transconductance Cell," *IEEE Trans. Circ. Syst. I*, vol. 69, no. 7, pp. 2805–2818, Mar. 2022.

[27] F. Centurelli, R. Della Sala, P. Monsurró, G. Scotti, and A. Trifiletti, "A 0.3 V rail-to-rail ultra-low-power OTA with improved bandwidth and slew rate," *J. Low Power Electron. Appl.*, vol. 11, no. 2, p. 19, Apr. 2021.

[28] T. Kulej and F. Khateb, "A compact 0.3-V class AB bulk-driven OTA," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 28, no. 1, pp. 224–232, Jan. 2019.

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