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Research Article

A 0.45 W 18% PAE E-Band Power Amplifier in 100 nm InGaAs pHEMT Technology

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This paper describes a fully integrated power amplifier (PA) in 100 nm InGaAs pHEMT process for E-band point-to-point communications. The device size and biasing conditions are optimized to enhance the overall performance at millimeter-wave frequencies. The complete PA consists of two unit PAs and each unit PA has four stages to improve the gain while ensuring stability from dc to the operating frequencies. A 4-way zero-degree combiner (in the unit PA) and a 2-way $\lambda/2$ combiner are used to boost the output power. Occupying 5 mm^2, the proposed PA achieves an output power of 0.45 W with 17.9% PAE at 74 GHz.

1. Introduction

There is an increasing need of E-band technology for future 5G network infrastructure, such as wireless backhaul. In wireless backhaul systems, highly directional antennas are employed at both transmitter and receiver sides to compensate for the path loss [1, 2]. For example, FCC Part 101 Rules [3] require a minimum antenna gain of 43 dBi to ensure the E-band radio equipment transmitting "pencil beams" to ease interference analysis and spatial coordination of links. Nevertheless, for a multi-Gbps link exceeding multikilometer distance, a watt-level power amplifier (PA) is required to ensure 99.99% weather availability worldwide [1, 2]. Such output power (P_{OUT}) requirement assigns new task for the fully integrated power amplifiers (PAs) at millimeter-wave (mm-Wave) frequencies.

Although the ever-increasing speed of MOS transistors provides new opportunities to mm-Wave designers, the low breakdown voltage limits the output power of E-band CMOS PAs to about 0.1 W [2, 4, 5]. The work in [6] demonstrated an E-band SiGe PA with 27.3 dBm P_{OUT}, but it may suffer additional loss in the packaging due to the placement of the output pads at the center of the die. Therefore, watt-level E-band PAs still remain in the domain of compound semiconductors. At E-band, GaN PAs [7] deliver more than 1 W P_{OUT} due to the high breakdown voltage while InP PAs [6] achieve PAE as high as 40% thanks to the high f_T/f_{MAX}. Nevertheless, GaAs technology [8–10] has the advantages of relatively low cost, high yield, and easy foundry access, offering an attractive alternative for E-band applications.

In this paper, we report a fully integrated E-band PA in 100 nm InGaAs pHEMT technology. Circuit optimizations have been applied to active device, unit PA, layout floorplan, and power combining structures to enhance the gain, output power, efficiency, and stability. The proposed 5 mm^2 PA demonstrates a measured power gain of 20.6 dB and an output power of 26.5 dBm with 17.9% PAE. Section 2 details the circuit optimizations regarding the transistor biasing, amplifier stage, and power combining structure. Section 3 shows the measurement results with the conclusion given in Section 4.

2. Design Considerations and Circuit Implementation

The power amplifier prototype was designed in a commercial 100 nm InGaAs pHEMT process (f_T/f_{MAX} = 130/200 GHz) with a breakdown voltage of 8 V and saturated output power density of about 600 mW/mm at a normal supply voltage of 4 V. The wafer thickness is 50 μm. In this work, the PA

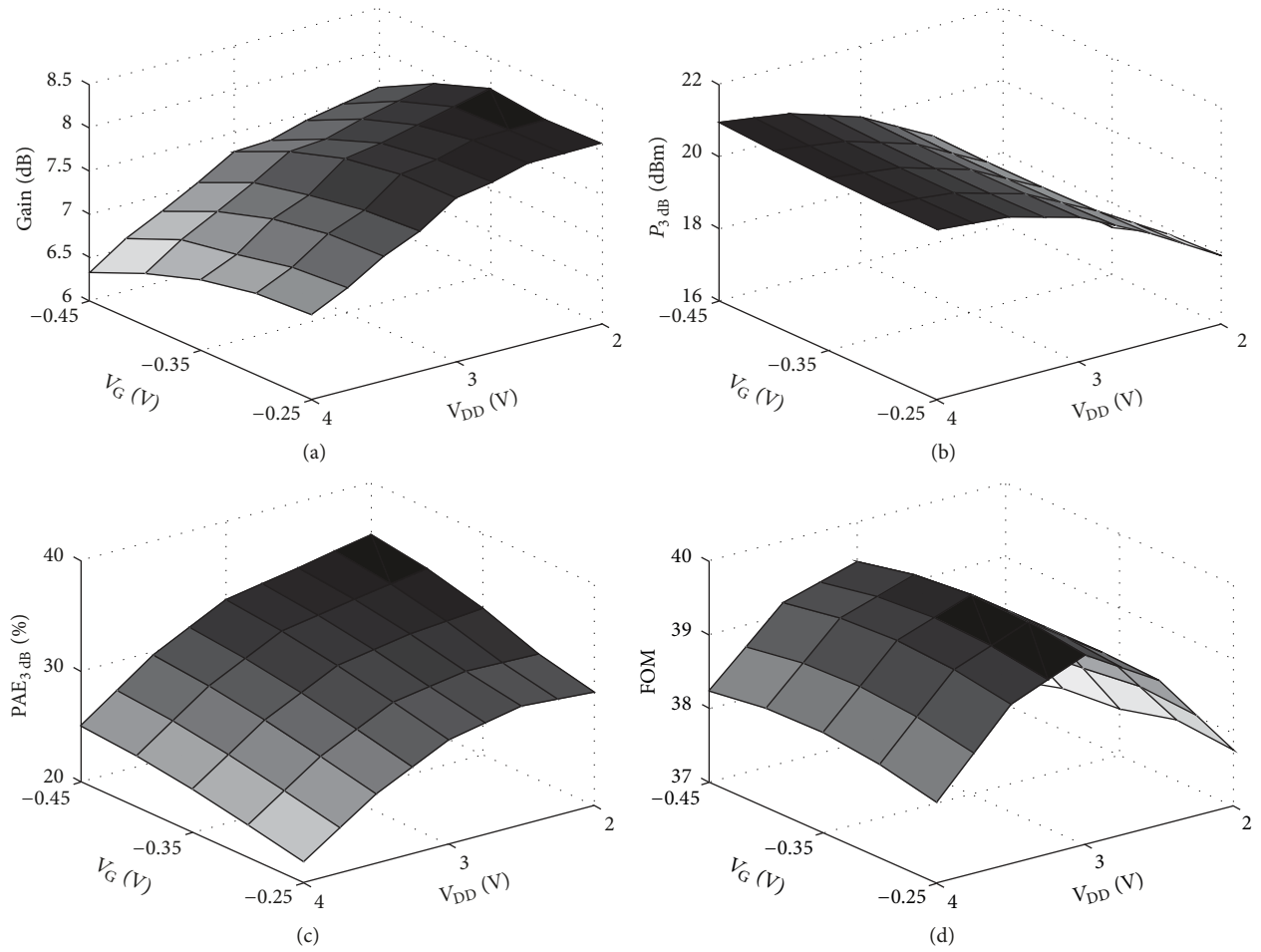


FIGURE 1: Single-stage PA metrics versus transistor biasing at 75 GHz: (a) gain, (b) $P_{3\,dB}$, (c) $PAE_{3\,dB}$, and (d) FOM = Gain (dB) + $P_{3\,dB}$ (dBm) + 10 log[$PAE_{3\,dB}$ (%)].

simulations were performed in ADS based on the PDK models while all the passive devices were characterized with ADS momentum.

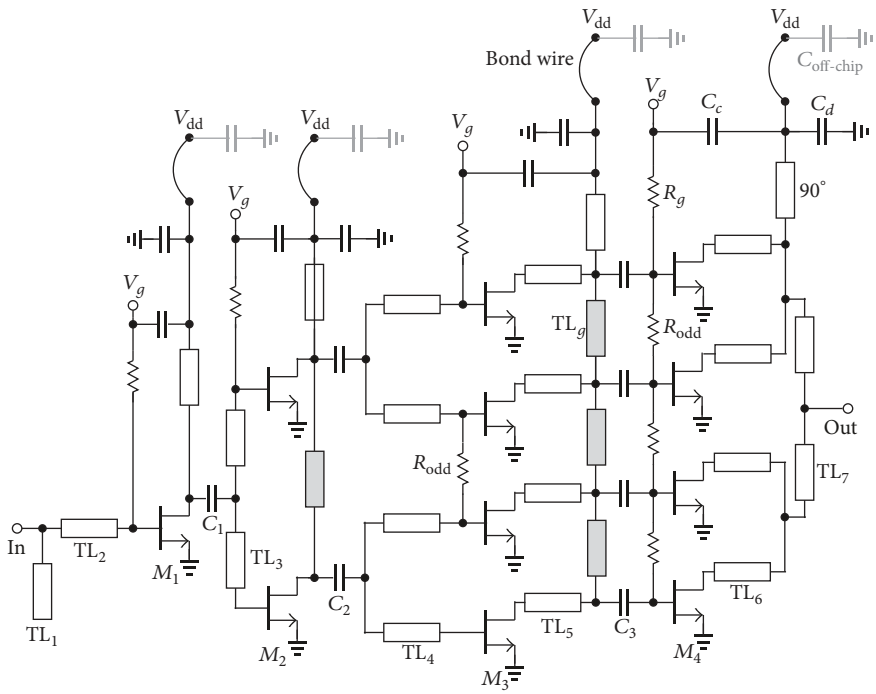
2.1. Transistor Design: Optimum Biasing. In this work, the transistor's biasing voltages are optimized based on the following PA figure-of-merit (FOM), given by

$$\begin{aligned} \text{FOM} = {} & \text{Gain (dB)} + P_{3\,\text{dB}}\,(\text{dBm}) \\ & + 10\log\left[\text{PAE}_{3\,\text{dB}}\,(\%)\right], \end{aligned} \tag{1}$$

where gain, $P_{3\,dB}$, and $PAE_{3\,dB}$ represent the power gain under power match, the 3 dB compressed output power ($P_{3\,dB}$), and the PAE at $P_{3\,dB}$ ($PAE_{3\,dB}$), respectively. Figure 1 shows the simulated power gain, $P_{3\,dB}$, $PAE_{3\,dB}$, and the calculated FOM versus different gate voltage (V_G) and drain voltage (V_{DD}) at 75 GHz. In the design, the device size of 50 μm × 4 (i.e., 50 μm finger width, four fingers) is selected to balance the power gain and output power. The ideal lossless input and output matching circuits are retuned for each biasing condition for fair comparison. From Figure 1, it is obvious that the PA has increased gain at a supply voltage of 2 V and it shows enhanced output power at 4 V. As the PA operates at a large fraction of f_T/f_{MAX}, the limited power gain has a direct impact on the PAE. As a result, $PAE_{3\,dB}$ peaks at V_{DD} of 2 V and V_G of −0.45 V despite the fact that the PA achieves 2 dB more $P_{3\,dB}$ at V_{DD} of 4 V. Such issue becomes even severe after including the loss of matching circuits. In this design, we chose the biasing points based on the FOM which equals the sum of the power gain, $P_{3\,dB}$, and $PAE_{3\,dB}$. Figure 1(d) shows that the FOM peaks at V_{DD} of 3 V and V_G of −0.35 V, giving the power gain, $P_{3\,dB}$, and $PAE_{3\,dB}$ of 7.8 dB, 19.5 dBm, and 31.6%, respectively, at 75 GHz.

Besides, an important feature for the 50 × 4 μm transistor under such biasing configuration is that the gain match and power match can be nearly achieved simultaneously, which significantly reduces the design efforts. Note that though 25 × 4 μm transistor shows relatively high maximum small-signal gain, it is potentially unstable at E-band and shows 3 dB lower P_{OUT} than 50 μm one which will complicate the power combining network for the same P_{OUT} requirement.

2.2. Unit PA Design: Gain, Power, and Stability. Using the optimum device size and bias configurations, a fully integrated unit PA is designed, as shown in Figure 2, where the



M_1	M_2	M_3	M_4	C_1	C_2	C_3
50 μm × 2	50 μm × 2	50 μm × 2	50 μm × 4	46fF	80fF	87fF
TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7
36 Ω, 48°	36 Ω, 26°	95 Ω, 32°	65 Ω, 15°	95 Ω, 12°	36 Ω, 40°	30 Ω, 25°

Figure 2: Simplified schematic of the E-band unit power amplifier.

details of the device parameters are also summarized. The unit PA consists of four stages to achieve more than 20 dB power gain and thus relax the input power requirement. To provide sufficient driving power and in order not to saturate prior to the output stage, the total transistor width of three driver stages is scaled down by a factor of two progressively. A 4-way zero-degree transmission-line (T-line) combiner [11] is employed to sum up P_{OUT} of the four 50 μm × 4 devices in the PA output stage. Compared to Wilkinson combiner, the zero-degree combiner significantly reduces the chip area and insertion loss while transforming the 100 Ω load to the optimum load impedance of each 50 μm × 4 device. The port isolation is not a major constraint here as all the combiner inputs have no phase difference. The 350 μm $\lambda/4$ T-lines are used as RF choke to feed the supply and the T-lines in grey (TL_g) are used to distribute the supply networks for the amplifier stages at lower side. Both TL_g and R_{odd} (see Figure 2) can help to reduce the gain of internal loops and thus eliminate potential oscillations. The capacitor C_d provides a short to ground in the range of operating frequencies. Extensive EM simulations have been performed on the complete passive circuits to take into account the mutual couplings between all the passive components. The simulated $P_{5\,dB}$ and $PAE_{5\,dB}$ for the unit PA equal 24.9 dBm and 22%, respectively. Note that, at $P_{5\,dB}$, the PA output stage is compressed by roughly 3 dB while the three driver stages are compressed by 2 dB. As the power gains of both driver stages and output stage are very limited, such design methodology ensures that the PA output stage can be driven into saturation while three driver stages consume relatively low dc power [12].

As the transistor has much higher power gain at low frequencies, the stability there becomes a big concern. Simulation predicts that the unit PA is potentially unstable in the range of 25 GHz. To tackle this, C_c is introduced at each stage to close the loop and thereby significantly reduce the power gain at low frequencies where the $\lambda/4$ dc-feeding T-lines show relatively low impedance and C_d shows high impedance. Consequently, the unit PA is unconditionally stable from dc to the operating frequencies and the in-band performance is not degraded at all.

2.3. Power Enhancement: Half-Wavelength T-Line Combiner. To further enhance the output power, the complete PA combines P_{OUT} of two unit PAs using $\lambda/2$ T-line power combiner, shown in Figure 3. A characteristic impedance (Z_o) of 70 Ω is chosen to balance the insertion loss and bandwidth. In this case, compared to Wilkinson and zero-degree combiners [11], the $\lambda/2$ T-line combiner is compact and straightforward to implement and has relatively broad bandwidth. More importantly, it is not sensitive to the process variations while covering a distance as long as 700 μm between the outputs of the two unit PAs. Including output GSG pads, the insertion loss of the $\lambda/2$ T-line combiner is 0.68–0.71 dB at 75 GHz for

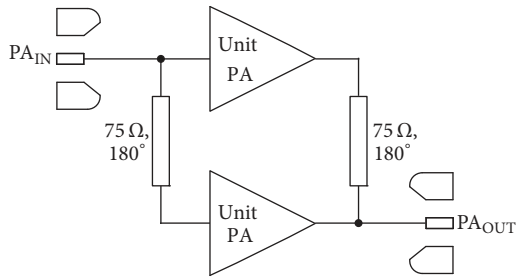


Figure 3: Power splitting and combining topologies based on $\lambda/2$ T-lines.

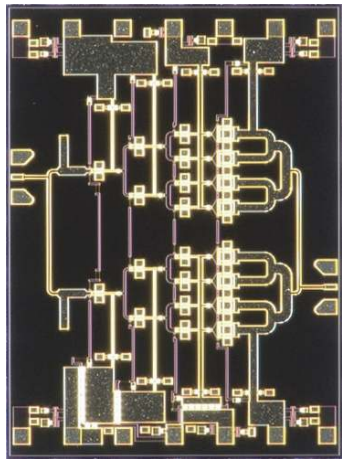


Figure 4: Chip micrograph.

a ±20% variation in Z_o. To compensate 180° phase difference, a $\lambda/2$ T-line power divider is used at the input.

3. Measurement Results

The PA prototype is fabricated in a 100 nm InGaAs pHEMT process. The chip micrograph is shown in Figure 4. Including RF and dc pads, the chip occupies an area of 5 mm^2. Measurements are performed on a high-frequency probe station. The input and output RF pads are accessed by GSG probes while dc pads are wire-bonded to a PCB. The supply voltage for the PA is 3 V.

Figure 5 shows the measured S-parameters. The PA achieves a peak S_{21} of 20.8 dB at 74 GHz with the 3 dB bandwidth of 7.5 GHz. Thanks to the optimum transistor sizing and biasing, ensuring simultaneous gain match and power match, S_{22} is better than −10 dB from 71.5 to 78.5 GHz. S_{11} is better than −10 dB from 71 to 77 GHz while S_{12} is smaller than −48 dB from 60 to 90 GHz. The PA is unconditionally stable in the measured frequencies. In addition, the output spectrum is carefully checked from dc to 90 GHz and no oscillation appears at the PA output. The large-signal behavior of the PA at 74 GHz is shown in Figure 6. The PA achieves a measured $P_{1\,\mathrm{dB}}$, $P_{3\,\mathrm{dB}}$, and $P_{5\,\mathrm{dB}}$ of 23.8, 25.5, and 26.5 dBm, respectively. $\mathrm{PAE}_{5\,\mathrm{dB}}$ is 17.9%. From 71 to 79 GHz, the measured output power is more than 25 dBm (see Figure 5). The measured and simulated results are in good agreement.

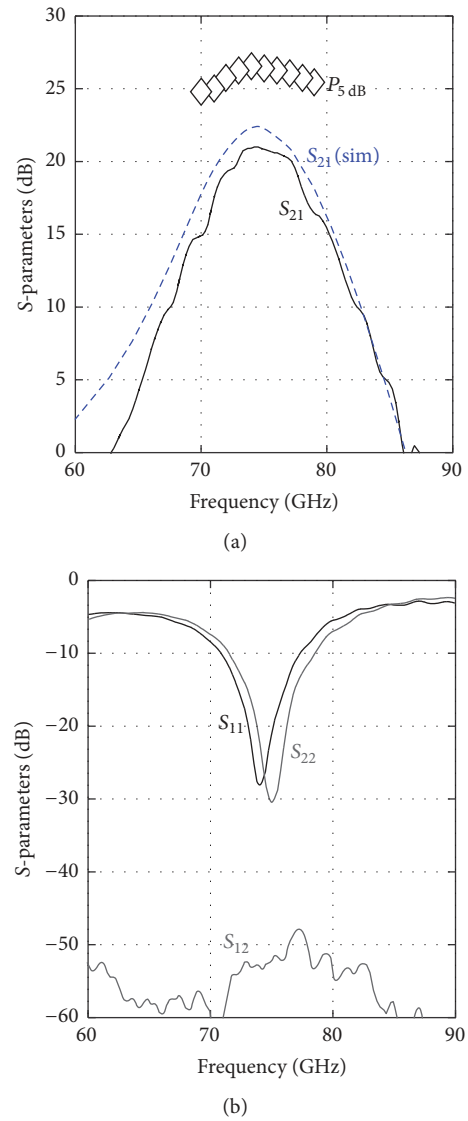


Figure 5: (a) Measured S_{21}, $P_{5\,\mathrm{dB}}$, and simulated S_{21}; (b) measured S_{11}, S_{12}, and S_{22}.

The 2 dB difference in gain can be attributed to the process variation and mutual couplings between multiple stages. The inaccurate modelling of back vias could be another issue as ADS momentum is a 2.5D electromagnetic (EM) simulator.

Table 1 compares the PA prototype to the state-of-the-art E-band PAs in GaAs, InP, SiGe, and CMOS. Albeit different technologies used, it can be seen that high output power will lead to relatively low efficiency owing to the loss in the power combining network. The work [6] in 250 nm InP with f_T/f_{MAX} of 400/700 GHz shows an impressive PAE. Thanks to the proposed design techniques, this PA achieves both high output power and high efficiency in 100 nm InGaAs pHEMT, competing well with prior-arts at E-band.

4. Conclusion

An E-band PA has been implemented in 100 nm InGaAs pHEMT process. To enhance the single-stage amplifier

Table 1: Performance summary and comparison.

	Technology	V_{DD} (V)	Frequency (GHz)	Gain (dB)	$P_{5\,dB}$ (dBm)	$PAE_{5\,dB}$ (%)
This work	100 nm GaAs	3.0	74	20.8	26.5	17.9
[8]	100 nm GaAs	4.0	83	15.0/18.7[1]	28.5/26.5[1]	N/A/15.0[1]
[9]	100 nm GaAs	3.5	81	25.0	20.0[2]	N/A
[10]	100 nm GaAs	4.0	76	15.0	23.0[2]	8.0[2]
[7]	140 nm GaN	14.0	93.5	16.3	33.3	19.0
[13]	250 nm InP	2.5	76	15.5	26.4	26.9
[14]	250 nm InP	2.5	81	22.0	21.1	40.0
[6]	90 nm SiGe	1.8	76	19.3	25.0[3]	9.0[3]
[15]	130 nm SiGe	2.5	84	27.0	18.0[2]	9.0[2]
[2]	40 nm CMOS	0.9	78	18.1	20.3	22.3
[4]	40 nm CMOS	1.8	73	25.3	21.5	16.5
[5]	65 nm CMOS	1.0	79	24.2	19.0	18.5

[1] $P_{4\,dB}$ and $PAE_{4\,dB}$. [2] P_{SAT} and PAE_{SAT}. [3] Graphically estimated.

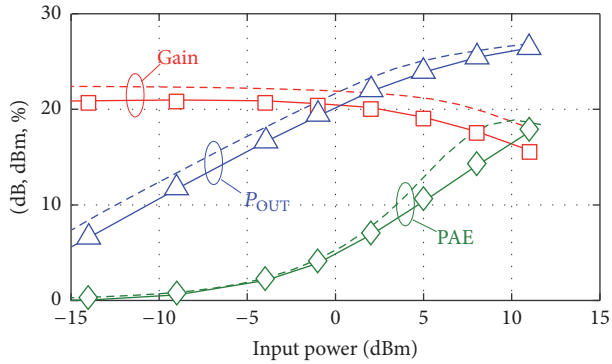


Figure 6: Measured and simulated (dashed) gain, output power, and PAE versus input power at 74 GHz.

performance, device size and biasing conditions are fine tuned. A 4-way zero-degree combiner and a 2-way $\lambda/2$ combiner are used to improve the output power. Attention has been paid to the PA stability in order to ensure no oscillations appearing from dc to the operating frequencies. The 5 mm^2 PA achieves an output power of 0.45 W with 17.9% PAE at 74 GHz. For future work, improvement can be done to reduce the insertion loss of the output combiner and thus further enhance the output power and efficiency. A highly efficient 16-way power combiner can also be investigated to double the output power. At E-band, the GaAs PA outperforms the CMOS PA regarding the output power while it achieves low cost, high yield, and easy foundry access when compared to InP and GaN PAs. Therefore, GaAs PA provides attractive solutions for future long-haul point-to-point communications at E-band.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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