A 0.5-to-2.5Gb/s Reference-less Half-Rate Digital CDR with Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance

Rajesh Inti, *Student Member, IEEE,* Amr Elshazly, *Student Member, IEEE,* Wenjing Yin, *Student Member, IEEE,* Pavan Kumar Hanumolu, *Member, IEEE*

Abstract

A reference-less highly digital half-rate clock and data recovery (CDR) circuit with improved tolerance to input duty cycle error is presented. Using a chain of frequency dividers, the proposed frequency detector produces a known sub-harmonic tone from the incoming random data. A digital frequency-locked loop uses the extracted tone, and drives the oscillator to any sub-rate of the input data frequency. The early/late outputs of a conventional half-rate bang-bang phase detector are used to determine the duty-cycle error in the incoming random data and adjust the oscillator clock phases to maximize receiver timing margins. Fabricated in 0.13μm CMOS technology, the prototype digital CDR operates without any errors from 0.5Gb/s to 2.5Gb/s. At 2Gb/s, the prototype consumes 6.1mW power from a 1.2V supply. The proposed clock-phase calibration is capable of correcting upto $\pm$20% of input data duty-cycle error.

Corresponding Author:
Rajesh Inti
School of EECS
Oregon State University
Corvallis, OR 97331
(541) 286-0372 / rajesh.inti@gmail.com

A 0.5-to-2.5Gb/s Reference-less Half-Rate Digital CDR with Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance

I. Introduction

Clock and data recovery (CDR) is a critical task in all serial communication systems. CDR circuits are employed in a wide range of applications including optical transceivers, chip-to-chip interconnects and backplane communications. The main objective of the CDR is to recover the data from the serial input bit stream in an error-free, power and cost-efficient manner. CDRs with wide frequency acquisition range offer flexibility in optical communication networks, help reduce link power through activity-based rate adaptation, and minimize cost with a single-chip multi-standard solution. Extracting the bit rate from the incoming random data stream is the main challenge in implementing such reference-less CDRs.

In this paper, we present a reference-less half-rate CDR that uses a sub-harmonic extraction method to achieve unlimited frequency acquisition range. This technique is capable of locking the CDR to within 40ppm of any sub-rate of the data (making it applicable for any sub-rate CDR architecture), while being immune to undesirable harmonic locking. This CDR also integrates a calibration loop to improve robustness to input duty-cycle error.

The paper is organized as follows. Section II provides a brief overview of conventional reference-based and reference-less CDR architectures. The proposed CDR architecture is outlined in Section III and the two important contributions of the design – a) reference-less frequency acquisition and b) clock phase calibration in the presence of input data duty-cycle error are presented. Details of the reference-less frequency acquisition technique are described in Section IV. Section V describes the origins of input data duty-cycle error and a clock phase calibration technique for optimal sampling of the incoming random data stream. Circuit design details of the important building blocks of the CDR are presented in Section VI. Section VII summarizes

the measurement results from the test chip.

II. Conventional Clock and Data Recovery Circuit Architectures

A conventional reference-based clock and data recovery circuit is shown in Fig. 1. It consists of a frequency-locked loop denoted as FLL and a phase-locked loop denoted as PLL. A reference clock generated by a crystal oscillator is used in the FLL to drive the VCO frequency towards the desired data rate. After the initial frequency acquisition, the PLL achieves phase lock and the VCO clock is driven to the center of the incoming data eye. Two separate loop filters, $\mathrm{LP_{FLL}}$ and $\mathrm{LP_{PLL}}$, independently set the loop dynamics of the FLL and PLL, respectively. While a reference-based CDR simplifies the design, the need for a crystal oscillator incurs additional cost. Furthermore, the CDR operating range is limited to only a few discrete frequencies dictated by the divider ratio and available crystal frequencies. A reference-less CDR obviates the need for an additional clock source and is capable of operating continuously over a wide range of frequencies.

The block diagram of a reference-less CDR is shown in Fig. 2. In this architecture, the FLL drives the VCO towards frequency lock by directly extracting the frequency error from the incoming random data $\mathrm{D_{IN}}$. Consequently, this architecture can operate continuously over a wide range of data rates. The biggest challenge in implementing such a reference-less CDR is the design of a frequency detector that is capable of extracting any error between VCO frequency and the input data rate. In practice, the CDR's frequency acquisition range is typically limited by the frequency detector. For instance, the detection range of a commonly used rotational frequency detector is limited to about 50% of the data rate [1], [2]. Additionally, none of the conventional architectures are amenable for sub-rate (e.g. half-rate) operation [2]–[9]. In this paper, we present a frequency detector that has unlimited detection range and is also suitable for sub-rate CDR operation.

Analog loop filters used in both reference-based and reference-less CDRs also pose several implementation difficulties. Very large capacitors in the order of nano farads are needed to meet the low jitter transfer bandwidth and small peaking requirements mandated by standards such as OC-48. Such capacitors when implemented on chip consume a large area, are PVT sensitive and when implemented using high density MOSCAPs are prone to leakage. Consequently, external capacitors are often used to overcome these issues [6]. In this work, we seek to use a fully

integrated digital loop filter (DLF) to overcome the drawbacks of analog loop filter.

III. Proposed Reference-less Half-rate CDR Architecture

The proposed digital CDR architecture is shown in Fig. 3 [10]. It is composed of a frequency locking loop (FLL), a phase-locking loop (PLL), and a data duty-cycle correction loop (DCCL). The FLL consisting of a frequency detector (FD), an accumulator (ACC), and a $\Delta\Sigma$ digital-to-analog converter (DAC) drives the digitally controlled oscillator (DCO) towards frequency lock. When the frequency error is within the PLL's pull-in range, it acquires phase lock. Because both the FLL and the PLL are driven by the incoming data, they can operate simultaneously, hence obviating the need for a lock detector. However, to prevent any interaction between the two loops, the FLL bandwidth is made much smaller than that of the PLL.

The digital PLL consists of a half-rate bang-bang phase detector (BBPD), a digital loop filter (DLF) to drive the DCO. The DLF is designed by transforming the analog loop filter into digital domain as shown in Fig. 4 [11]. In conventional analog implementations, loop filter is a simple series connected resistor-capacitor network with the voltage across the resistor and the capacitor implementing the proportional and integral control, respectively. In the digital loop filter, proportional and integral control paths are implemented separately and the summing of the two control signals is performed in analog domain. This topology eliminates the need for one adder and reduces the dithering jitter by minimizing latency in the proportional path [12]. The bang-bang phase detector compares input data edges and the DCO clock phases and generates two pairs of early/late (E/L) decisions. The (E/L) signals drive the DCO through a 5-level current-mode DAC (+2I,+I,0,-I,-2I) and implement the proportional control. The integral path consists of an accumulator followed by a high-resolution DAC. The circuit complexity of a high-resolution DAC is relaxed by using a low-resolution DAC driven by a digital $\Delta\Sigma$ modulator. The highly digital loop filter is PVT insensitive and is fully synthesized in our design. The E/L data are decimated by a factor of 16 before feeding to a low frequency accumulator.

The duty-cycle error in the transmit clock of a half-rate transmitter manifests itself as unequal widths of the transmitted even/odd data eyes. Sampling this incoming data with equally spaced clock phases (0.5UI in a half-rate receiver) reduces receiver timing margin. To alleviate this, the digital DCCL estimates the input data duty-cycle error and calibrates the DCO clock phases for optimal sampling of both the even and odd data bits. At start up, the early/late decisions of a

conventional half-rate bang-bang phase detector are analyzed to deduce information about the *sign* of incoming random data duty-cycle error. The DCCL utilizes a very low bandwidth Type-I loop to adjust the delay on each of the 4 clock phases I/Q/Ib/Qb and improves timing margin.

IV. Proposed Frequency Detector

A conventional rotational frequency detector (RFD) and its variants reported in [2]–[4], [6] rely on *sampling* the oscillator clock phase with the incoming random data to determine the frequency error. This sampling phenomenon causes nulls in the RFD transfer characteristic as shown in Fig. 5, and limits the acquisition range to about $\pm 50\%$ of the data rate. Further, RFD based frequency acquisition loops require a full-rate clock with I/Q phases rendering this frequency detector to be power hungry and useless for sub-rate CDR topologies. In this work, we propose a frequency detector which extracts a low frequency sub-harmonic clock from the incoming data rate. Using the extracted tone as a reference in a digital FLL locks the oscillator frequency to the data rate. The proposed FLL can be used to implement any sub-rate CDR architecture.

Before presenting the proposed frequency detection scheme, it is instructive to evaluate the transition probabilities of alternating and random data patterns. As shown in Fig. 6 for alternating data, the probability of both $1\rightarrow0$ and $0\rightarrow1$ transitions is equal to 0.5. Being a clock pattern, a $1\rightarrow1$ or a $0\rightarrow0$ transition never occurs and the associated probability is therefore 0. On the other hand, in a random data pattern, all the four possible transitions are equally likely, with a probability of 0.25. An important observation is to note that, compared to the alternating data case, the probability of $1\rightarrow0$ and $0\rightarrow1$ transitions is exactly halved. We use this fact along with a digital accumulator to implement a frequency detector with unlimited acquisition range.

To understand how the process of accumulation helps in frequency extraction, consider the case of a 10-bit counter clocked by 2 different inputs - alternating data and random data. Since the counter counts only on the positive edge, the time taken to count from 1 to 1024 is 2048 unit intervals (UI). In other words, when clocked with alternating data counter roll-over happens every 2048UI, as shown in Fig. 7. Now consider the case in which the same counter is clocked with random data. Because the transition density in random data compared to alternating data is exactly halved as discussed earlier, the accumulation rate is also halved. As a result, the counter roll-over happens every 4096UI, as shown in Fig. 8. Deviation in the transition density from

the ideal value of 0.25 in the random data leads to a proportional error in the elapsed time to reach a count of 1024. As shown later, this error will introduce a fixed offset at the output of the proposed frequency detector.

A closer look at the counter output in Fig. 9 reveals that the most significant bit (MSB) toggles every 2048UI. In view of this, the 9 least significant bits of the counter output are discarded and the most significant bit, referred to as the *extracted sub-harmonic* henceforth, is used as the reference clock in the FLL for frequency locking. The counter is implemented as a cascade of 10 divide-by-2 stages as shown in Fig. 10. This realization is not only simple but also consumes little power. The simplicity of this structure makes it very useful for sub-harmonic extraction even at higher data rates also.

Despite the fact that random data has spectral nulls at all integer multiples of $\mathrm{F_B}$, passing it through a chain of dividers extracts a sub-harmonic of $\mathrm{F_B}$. This counter intuitive result can be better understood by reexamining the frequency detector behavior in the frequency domain. After passing the random data through one divide-by-2 stage, the resulting output PSD is given by the expression $\mathrm{S_{x_{div2}}}(\omega) \approx \frac{4\mathrm{F_B}}{\omega^2}\Big(\frac{1}{4} - \frac{1}{8}\cos(\frac{2\omega}{\mathrm{F_B}}) - \frac{1}{8}\cos(\frac{3\omega}{\mathrm{F_B}}) - \frac{1}{16}\cos(\frac{4\omega}{\mathrm{F_B}})\Big)$. The plot of this expression is shown in Fig. 11 (The methodology for deriving the expressions for the spectral density of the NRZ random data and the output of the first divide-by-2 stage is derived in the Appendix). Plotting this reveals that there is an increase in power at $\frac{\mathrm{F_B}}{8}$ frequency. Adding another divide-by-2 stage, the output of the effective divide-by-4 stage now peaks at $\frac{\mathrm{F_B}}{16}$. We make an important observation that each divide-by-2 stage causes a 6dB increase in the output PSD peak.

Following the same line of argument, a divide-by-1024 stage shapes the input random data PSD to a tone at $\frac{\mathrm{F_B}}{4096}$, as shown in Fig. 12. Intuitively, a 2^{10} divider acts as an asynchronous modulo-2^{10} counter with its output toggling whenever the number of low-to-high data transitions reaches 2^{10}. Therefore, for binary random data with equal low-to-high and high-to-low transitions, the average frequency of the divider output is equal to $\frac{0.5\mathrm{F_B}}{2^{10+1}}$. Having discussed the proposed sub-harmonic extraction scheme in detail, the implementation details of the frequency locking loop (FLL) are presented next.

The block diagram of the FLL is shown in Fig. 13. A conventional counting type frequency detector is used in this implementation. Frequency error is determined by finding the difference

between the number of VCO periods in adjacent reference periods. The VCO clock is divided by 16 before feeding it into the 14-bit counter to relax counter speed requirements. Being a half-rate CDR architecture, the FLL must frequency lock the DCO to $\frac{\mathrm{F_B}}{2}$. Because extracted reference clock is $\frac{\mathrm{F_B}}{4096}$, under locked condition, there will be $\frac{4096}{32} = 128$ divided DCO clock periods in adjacent periods of the reference clock. Deviation of the counter output from 128 is the measure of frequency error. Two registers are used to perform the 1-z^{-1} operation and the resulting frequency error signal is fed to the digital loop filter. The digital loop filter is composed of a digital accumulator whose output drives the DCO.

V. Improving tolerance to input duty-cycle error

Input duty-cycle error in a half-rate CDR reduces the timing margins and degrades it performance. Figure 14 illustrates the origins of the data duty-cycle error. When the transmitter is clocked with a 50% duty-cycle clock, the resulting transmit output eye is symmetric and both the odd and even eyes have the same width. But in the presence of a duty-cycle error in the transmit clock, the transmitter output inherits the clock's duty-cycle error. This manifests itself as an asymmetric transmitter eye as shown in the bottom half of Fig. 14.

When the asymmetric eye is fed to the CDR, the steady state sampling points are sub optimal as depicted in Fig. 15. Note that the four phases, I/Q/Ib/Qb are equally spaced as they are generated by a ring oscillator with nominally identical delay stages. In this work, we seek to calibrate each of the individual phases to maximize timing and voltage margins as shown in the bottom half of Fig. 15. The amount of phase shift required in the wake of input data duty-cycle error is best understood with an example. Consider the case where input data eye has α UI duty-cycle error as shown in Fig. 16 i.e. odd eye is α UI larger than the even eye. Under this condition, the clock phases are separated by 0.5 UI while the desired phase spacing must be as shown in column 3 of the table in Fig. 16. The new phase spacing guarantees that both Q and Qb phases are positioned at the center of the odd and even eyes at 0.5(1+α) UI and 1.5+0.5α UI, respectively. Hence, to ensure optimal sampling, Q/Qb and Ib need to shifted by 0.5α UI and α UI, respectively.

Figure 17 shows the details of the calibration scheme that drives the quadrature phases to optimal sampling positions. In the presence of an input duty-cycle error, there are 4-possible lock points in a half-rate CDR. The two edge sampling clocks I/Ib can lock to either the smaller

or the larger eye, creating 4 different locking scenarios. In cases 1 and 2, phase I is locked to the edge while in cases 3 and 4, phase Ib is locked to the edge. While it is possible to adjust the phase spacing of each of the 4 phases independently, it is cumbersome and requires a complicated algorithm to perform the calibration. The calibration logic can be simplified by forcing the CDR to lock to only 2 of the 4 possibilities, as discussed next.

Consider the case in which the early/late decisions corresponding to the even data input are ignored, as shown in Fig. 18 . Because the phase error information corresponding to only the odd data bit is used, phase I always locks to the data edge, thus eliminating locking scenarios 3 and 4. We also note that in case 1, clock phases (Q/Ib/Qb) are always early while in case 2 the clocks (Q/Ib/Qb) are always late. This information of being *always* early or *always* late can be obtained by observing the unused even E/L pair. In other words, $(\text{E/L})_{\text{EVEN}}$ decisions indicate the sign of the duty-cycle error.

The block diagram of the data duty-cycle estimator is shown in Fig. 19. At start up, the CDR is locked only with the $(\text{E/L})_{\text{ODD}}$ decisions of the half-rate bang-bang phase detector. The $(\text{E/L})_{\text{EVEN}}$ signals are decimated by 16 and accumulated using a low speed accumulator. The direction of accumulation of the $(\text{E-L})_{\text{EVEN}}$ signal is indicative of the sign of the duty-cycle error. Simulation results for locking scenarios 1 and 2 are shown in Fig. 20. In the left half of the figure, the $(\text{E-L})_{\text{EVEN}}$ signal accumulates with a positive slope, indicative of an always early condition and the in the right half of the figure, the signal accumulates with a negative slope which is indicative of an always late condition. The slope detector block implemented as an accumulator followed by a first order differentiation, $1\text{-}z^{-1}$, determines the *sign* of the slope of accumulation. The sign of the duty-cycle error, $\widehat{D_E}$, is fed to an accumulator whose output control the digital-to-delay converters (DDC). Simulation results showing the convergence of the clock-phase calibration algorithm are shown in Fig. 21. Circuit implementation details of the DDC are presented in Section VI.

VI. Circuit Design

The half-rate bang-bang phase detector is implemented using a conventional Alexander phase detector [13]. Improved sense-amplifier flip-flops are used as data and edge samplers [14]. To ease speed requirements in the digital integral path, the early/late samples are decimated by a factor of 16. The decimator is realized as a cascade of 4 decimate-by-2 stages. Each decimate-

by-2 stage operates on consecutive early and late samples and performs a *signed* arithmetic subtraction and truncates the result to a 3 valued signal [-1,0,+1] [12], [15]. All the other digital circuit blocks are fully synthesized using standard cells. The design details of the analog building blocks namely the digitally controlled oscillator and the linear digital-to-delay conversion cells used in the duty cycle correction loop are presented next.

A. Digitally Controlled Oscillator (DCO)

The schematic of the DCO is shown in Fig. 22. It is composed of a 4-phase current-controlled ring oscillator and has three separate control ports. The FLL, proportional, and the integral control words denoted as $\mathrm{D_{FLL}}$, $\mathrm{D_{PROP}}$, and $\mathrm{D_{INT}}$, respectively, tune the oscillator frequency independently. The two pairs of early/late signals generated by the half-rate bang-bang phase detector constitute $\mathrm{D_{PROP}}$ and a 5-level DAC converts it into current. $\mathrm{D_{FLL}}$ and $\mathrm{D_{INT}}$ are the outputs of the respective accumulators in the FLL and the digital integral paths (see Fig. 3). Two 14-bit DACs convert $\mathrm{D_{FLL}}$ and $\mathrm{D_{INT}}$ into analog voltages which control the oscillator tuning currents. The schematic of the DAC is shown in Fig. 23. A second order digital delta-sigma modulator truncates the 14-bit input to 4 bits and drives a thermometer-coded 15-level current-mode DAC (IDAC). The output current is converted into voltage by the load resistor and a second-order low pass post filter suppresses the shaped high frequency quantization error.

The simulated FLL-path tuning curve of the DCO is shown in Fig. 24. The FLL path is capable of tuning the DCO to frequencies ranging between 90 MHz to 1.7 GHz. After initial frequency acquisition, the PLL integral path accounts for drift in DCO frequency. Around 1.25 GHz, the PLL integral path is capable of tracking frequency variations of about $\pm$35 MHz as shown in Fig. 25.

B. Linear Digital-to-Delay Conversion

As explained in Section V and illustrated in Fig. 3, the duty-cycle error estimator controls a bank of digital-to-delay conversion cells (DDC) to calibrate the edge and data sampling clock phase. A simple way to implement the DDC is by using a conventional current-starved inverter as shown in Fig. 26. Since the delay is inversely proportional to the control current, a DDC implemented by digitally scaling the current exhibits 1/x non-linearity. Two important issues arise from this non-linear control behavior. First, the large DDC gain at smaller inputs makes

achieving good resolution challenging. Second, implementing αUI and 0.5αUI delays needed in Q/Qb and Ib paths, respectively, by scaling the input digital control word becomes impossible. In view of these drawbacks, we propose a DDC architecture that seeks to eliminate this non-linearity.

Figure 27 shows the proposed linear digital-to-delay converter. By pre-warping the control current by a 1/x function, the non-linearity is eliminated. To this end, a digitally controlled resistor is used to make the charging current vary inversely with the input digital control word, $\mathrm{I_C} \propto 1/\mathrm{D_C}$, thus linearizing the DDC transfer curve. The delay range can be adjusted by using an appropriate reference voltage, V_{REF}, and is chosen to cover up to $\pm 20\%$ input data duty-cycle error. The simulated delay characteristics of the DDC shown in Fig. 28 illustrate the linear behavior and range variation with V_{REF}. Compared to the conventional DDC, the proposed DDC exhibits superior linearity without compromising the tunable delay range.

The schematics of all the 4 delay cells used to phase shift clocks, I/Q/Ib/Qb, are shown in Fig. 29. Since the CDR locks phase I to the data edge, no calibration is needed for this phase, thus $\mathrm{D_C}$ is set to zero. As discussed earlier, another requirement of the clock phase calibration circuit was that the gain on clock phase Q/Qb be exactly half compared to that of Ib. Owing to the linear transfer characteristics of the proposed DDC, the desired gain scaling is achieved by bit-shifting the control word to the individual cells. Consequently, the control code to Q/Qb and phases Ib is equal to $\mathrm{D_C}$ and $2\mathrm{D_C}$, respectively.

VII. Measured Results

The prototype digital CDR was implemented in a 1.2V 0.13μm CMOS process. High-speed differential current-mode logic buffers are used to drive the on-chip recovered half-rate data and clock for measurement purposes. The die micrograph is shown in Fig. 30 and the active area is 0.39 mm^2. The die was packaged in a TQFP48 package and tested using four-layer printed circuit board. The input PRBS sequences of varying lengths were generated using a arbitrary waveform generator (Tektronix AWG7000). Agilent E4440 spectrum analyzer and Tektronix Communication Signal Analyzer CSA8200 are used to analyze the spectral and jitter properties of the recovered clock.

A 2Gb/s random data is fed to the CDR and the measured power spectral density (PSD) plots at the output of the first three divide-by-2 stages is shown in Fig. 31. Passing the input data

whose PSD has spectral nulls at all integer multiples of 2GHz through a divide-by-2 stage causes the PSD to peak at $\frac{F_B}{8}$, i.e 250 MHz and the PSD of the next two divide-by-2 stages peak at 125 and 62.5 MHz respectively. This spectral peaking measurement is consistent with the theoretical predictions from Appendix.

The dependence of the proposed frequency detector accuracy on input data transitions is characterized by measuring the frequency error with different input PRBS sequences and the results are presented in Fig. 32. The deviation of the transition density in PRBS patterns from the ideal value of 0.25 causes a frequency offset in the FLL. For a 2^N-1 long PRBS sequence, the frequency offset is given by

$$\text{Theoretical Offset [ppm]} \approx \frac{10^6}{2^N} \tag{1}$$

This expression matches closely with the measured frequency offset as shown in Fig. 32. Scrambling the input data with a polynomial, $p(x)=1+x^{18}+x^{23}$, brings the transition density to be closer to 0.25 and improves the accuracy to better than 100ppm, irrespective of the input sequence periodicity. The measured FLL and PLL clocks spectrums for PRBS10 and PRBS15 patterns are shown in Fig. 33. As discussed previously, the imbalance in PRBS10 and PRBS15 patterns leads to an FLL offset of 1000ppm and 100ppm, respectively.

The measurement in Fig. 34 shows the edge sampling clocks before and after calibration. Because of the 20% input data duty-cycle error, the width of the odd and even eyes are 600ps and 400ps, respectively. Under this condition, the edge sampling clock, Ib, is nominally at 500ps before calibration. After calibration, Ib phase is phase shifted by about 100ps, thus bringing it very close to the edge transition of the smaller eye as desired. The distortion in the clock waveforms is caused by the multiplexer used to bring out multiple high speed signals.

The recovered clock jitter for a 2Gb/s PRBS10 pattern with 300mVpp differential swing is shown in Fig 35. The long term accumulated jitter of the recovered clock is 5.4ps,rms and 44ps,pk-pk. The measured BER is less than 10^{-12}.

Table I shows the performance summary of the CDR. The CDR implemented in a 0.13μm CMOS process operates with supply voltage ranging from 0.8 to 1.2V. At 0.8V, the achieved data rate range is 0.2 to 1Gb/s and at 1.2V it operates between 0.5 to 2.5Gb/s. When operating at 2Gb/s, the power in the FLL and PLL loops is 1.2 and 4.9mW, respectively. This CDR achieves a figure-of-merit of 3.05 mW/Gbps. Table II compares the performance of the digital CDR with

other state-of-the-art designs in the literature. This work demonstrates a fully integrated, low power digital reference-less CDR with unlimited frequency acquisition range.

VIII. Conclusions

A reference-less highly digital half rate clock and data recovery (CDR) circuit with improved tolerance to input duty cycle error is presented. Using a chain of frequency dividers, the proposed frequency detector shapes the PSD of the input random data and produces a known sub-harmonic tone. A digital frequency-locked loop uses the extracted tone, and drives the oscillator to any sub-rate of the input data frequency. In contrast to conventional frequency detectors, the proposed architecture is well suited to any reference-less sub-rate CDR. The accuracy of the proposed scheme is degraded by the deviation in the input transition density from the ideal value of 0.25, but can be easily improved by scrambling the input data before feeding to the frequency detector.

The early/late outputs of a conventional half-rate bang-bang phase detector are used to determine the duty-cycle error in the incoming half-rate random data and to adjust the oscillator clock phases to maximize receiver timing margins. Fabricated in 0.13μm CMOS technology, the prototype digital CDR operates with out any errors from 0.5Gb/s to 2.5Gb/s. At 2Gb/s, the prototype consumes 6.1mW power from a 1.2V supply. The proposed clock-phase calibration is capable of correcting upto $\pm 20\%$ of input data duty-cycle error.

IX. Acknowledgements

This work was partially supported by National Science Foundation (NSF) under CAREER EECS-0954969 and a research grant from Intel. The authors thank Dongbu HiTek for IC fabrication and Ganesh Balamurugan of Intel for help with testing.

Appendix

Random NRZ data signal, $x(t)$, can be synthesized by passing a train of impulses, $p(nT_{\mathrm{B}})$, through an integrator as illustrated in Fig. 36. The impulse takes one of three possible values, +1, -1, and 0, corresponding to positive, negative, and no transitions in the random data. Mathematically,

$$x(t) = \int_{-\infty}^{\infty} p(nT_B)\, dt.$$

The power spectral density (PSD) of x(t), $p(nT_{\mathrm{B}})$ denoted as $S_x(\omega)$ and $S_p(\omega)$ are related as follows,

$$S_x(\omega) = \frac{4S_p(\omega)}{\omega^2} \tag{2}$$

Using the Wiener-Khinchin theorem [18], $S_p(\omega)$ can be calculated as,

$$S_p(\omega) = \frac{1}{T_B}\sum_{n=-\infty}^{\infty} R_p[n]e^{-j\omega nT_B}, \text{ where } \; R_p[n] = \mathrm{E}\left[\, p(k)p(k-n) \,\right] \tag{3}$$

Because the autocorrelation function of a real valued signal $p(nT_{\mathrm{B}})$ is an even function ($R_p[n] = R_p[-n]$), the above expression can be rewritten as,

$$S_p(\omega) = \frac{1}{T_B}\left(R_0 + 2\sum_{n=1}^{\infty} R_p[n]\cos(n\omega T_B)\right) \tag{4}$$

Combining Eq. 2 and Eq. 4 we get the PSD of the NRZ data to be,

$$\boxed{S_x(\omega) = \frac{4S_p(\omega)}{\omega^2} = \frac{4F_B}{\omega^2}\left(R_p[0] + 2\sum_{n=1}^{\infty} R_p[n]\cos(n\omega T_B)\right)} \tag{5}$$

Using Eq. (5), $S_x(\omega)$ can be determined by evaluating the autocorrelation function $R_p[n]$. Recognizing that $p(nT_{\mathrm{B}})$ can take only one of three values, -1, 0, +1 with probabilities of $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{1}{4}$, respectively, the autocorrelation function can be calculated as follows:

$$\begin{aligned}
R_p[0] &= \mathrm{E}\left[\, p(k)p(k) \,\right] \\
&= (-1\times -1)P(p=-1) + (0\times 0)P(p=0) + (+1\times +1)P(p=+1) \\
&= \frac{1}{4} + 0 + \frac{1}{4} = \frac{1}{2} \\
R_p[1] &= \mathrm{E}\left[\, p(k)p(k+1) \,\right] \\
&= (-1\times -1)P(p_{k,k+1}=-1,-1) + (-1\times +1)P(p_{k,k+1}=-1,+1) \\
&\quad + (+1\times -1)P(p_{k,k+1}=+1,-1) + (+1\times +1)P(p_{k,k+1}=+1,+1)
\end{aligned}$$

Note that though there are 9 different consecutive bit combinations that affect $R_p[1]$, p(k) being 0 removes 5 terms ([0,+1],[0,0],[0,-1],[+1,0],[-1,0]). Also, the associated probabilities of $P(p_{k,k+1}=-1,-1) = P(p_{k,k+1}=+1,+1)$ = 0 for NRZ random data, since two transitions of the same type cannot happen in consecutive bit periods. Thus,

$$\begin{aligned}
R_p[1] &= (-1\times +1)P(p_{k,k+1}=-1,+1) + (+1\times -1)P(p_{k,k+1}=+1,-1) \\
&= -(\frac{1}{2}\times\frac{1}{4}) - (\frac{1}{2}\times\frac{1}{4}) = -\frac{1}{4}
\end{aligned}$$

For n≥2, the amplitudes of p(k) and p(k+2) become independent, yielding $R_p[n]$ = 0, when n≥2. Substituting $R_p[0]$ = $\frac{1}{2}$ and $R_p[1]$ = $-\frac{1}{4}$ into Eq. (5), yields

$$S_x(\omega) = \frac{4F_B}{\omega^2}\left(\frac{1}{2} + (2 \times -\frac{1}{4})\cos(\omega T_B)\right) = \frac{4F_B}{\omega^2}\left(\frac{1}{2} - \frac{1}{2}\cos(\omega T_B)\right) = T_B \operatorname{sinc}^2(\frac{\omega T_B}{2}) \quad (6)$$

The signal $p(nT_{\mathrm{B}})$ when passed through a divide-by-2 circuit results in halving the number of 1→0 and 0→1 transitions. As a result, -1, 0, +1 occur with probabilities of $\frac{1}{8}$, $\frac{3}{4}$, and $\frac{1}{8}$, respectively. Using the modified probabilities, the autocorrelation and the PSD of the divide-by-2 stage output, $x_{div2}(t)$, can be found to be,

$$R_p[0] = \frac{1}{4},\ R_p[1] = 0,\ R_p[2] = -\frac{1}{16},\ R_p[3] = -\frac{1}{16},\ R_p[4] = -\frac{1}{32}\cdots$$

$$S_{x_{div2}}(\omega) \approx \frac{4F_B}{\omega^2}\left(\frac{1}{4} - \frac{1}{8}\cos(2\omega T_B) - \frac{1}{8}\cos(3\omega T_B) - \frac{1}{16}\cos(4\omega T_B)\right) \quad (7)$$

Plotting expressions (6, 7) for a 2Gb/s NRZ random input stream, the peaking at 250MHz and 125MHz at output of each of the divide-by-2 stage is revealed.

REFERENCES

[1] D. Messerschmitt, "Frequency detectors for PLL acquisition in timing and carrier recovery," *IEEE Transactions on Communications*, vol. 27, no. 9, pp. 1288-1295, Sep., 1979.

[2] L. DeVito, J. Newton, R. Croughwell, J. Bulzacchelli, F. Benkley, "A 52MHz and 155MHz clock-recovery PLL," *ISSCC Dig. Tech. Papers*, pp. 142-306, Feb., 1991.

[3] H. Ransijn and P. O'Connor, "A PLL-based 2.5-Gb/s GaAs clock and data regenerator IC", *IEEE J. Solid-State Circuits*, vol. 27, pp. 1345-1353, Oct. 1991.

[4] A. Pottbacker, U. Langmann and H. Schreiber, "A Si bipolar phase and frequency detector IC for clock extraction up to 8 Gb/s", *IEEE J. Solid-State Circuits*, vol. 27, pp. 1747-1751, Dec. 1992.

[5] B. Razavi, "A 2.5-Gb/s 15-mW clock recovery circuit", *IEEE J. Solid-State Circuits*, vol. 31, pp. 472-480, Apr. 1996.

[6] D. Dalton, K. Chai, E. Evans, M. Ferriss, D. Hitchcox, P. Murray, S. Selvanayagam, P. Shepherd, and L. DeVito, "A 12.5-Mb/s to 2.7-Gb/s continuous-Rate CDR with automatic frequency acquisition and data-rate read back," *ISSCC Dig. Tech. Papers*, pp. 230-231, Feb., 2005.

[7] R. Yang, K. Chao, S. Hwu, C. Liang and S. Liu, "A 155.52 Mbps to 3.125 Gbps continuous-rate clock and data recovery circuit", *IEEE J. Solid-State Circuits*, vol. 41, pp. 1380-1390, Jun. 2006.

[8] M. Perrott, Y. Huang, R. Baird, B. Garlepp, L. Zhang, and J. Hein, "A 2.5 Gb/s multi-rate 0.25μm CMOS CDR utilizing a hybrid analog/digital loop filter," *ISSCC Dig. Tech. Papers*, pp. 328-329, Feb., 2006.

[9] J. Lee and K. Wu, "A 20Gb/s full-rate linear CDR circuit with automatic frequency acquisition," *ISSCC Dig. Tech. Papers*, pp. 336-337, Feb., 2009.

[10] R. Inti, W. Yin, A. Elshazly and P. Hanumolu, "A 0.5-to-2.5 Gb/s reference-less half-rate digital CDR with unlimited frequency acquisition range and improved input duty-cycle error tolerance," *ISSCC Dig. Tech. Papers*, pp. 228-229, Feb., 2011.

[11] V. Kratyuk, P. Hanumolu, U. Moon, K. Mayaram, "A design procedure for all-digital phase-locked loops based on a charge-pump phase-locked-loop analogy," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 247-251, Mar., 2007.

[12] P. Hanumolu, M. Kim, G. Wei and U. Moon, "A 1.6 Gbps digital clock and data recovery circuit", *Proc. Custom Int. Circuits Conf.*, pp. 603-606, Sept. 2006.

[13] J. Alexander, "Clock recovery from random binary signals", *Electronic Letters*, vol. 41, pp. 541-542, Oct. 1975.

[14] B. Nikolic and V. Oklobdzija and V. Stojanovic and W. Jia and J. Chiu and M. Leung, "Improved sense-amplifier-based flip-flop: design and measurements", *IEEE J. Solid-State Circuits*, vol. 35, pp. 876-884, Jun. 2000.

[15] J. Sonntag and J. Stonick, "A digital clock and data recovery architecture for multi-gigabit/s binary links", *IEEE J. Solid-State Circuits*, vol. 41, pp. 1867-1875, Dec. 2006.

[16] D. H. Oh, D. S. Kim, S. Kim, D. K. Jeong, and W. Kim, "A 2.8 Gb/s all-digital CDR with a 10b monotonic DCO," *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb., 2007.

[17] S. Lee and Y. Kim H. Ha and Y. Seo and H. Park and J. Sim, "A 650Mb/s-to-8Gb/s referenceless CDR circuit with automatic acquisition of data rate," *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb., 2009.

[18] B. P. Lathi, "Modern digital and analog communication systems", *Oxford University Press*, 1995.

LIST OF FIGURES

LIST OF TABLES

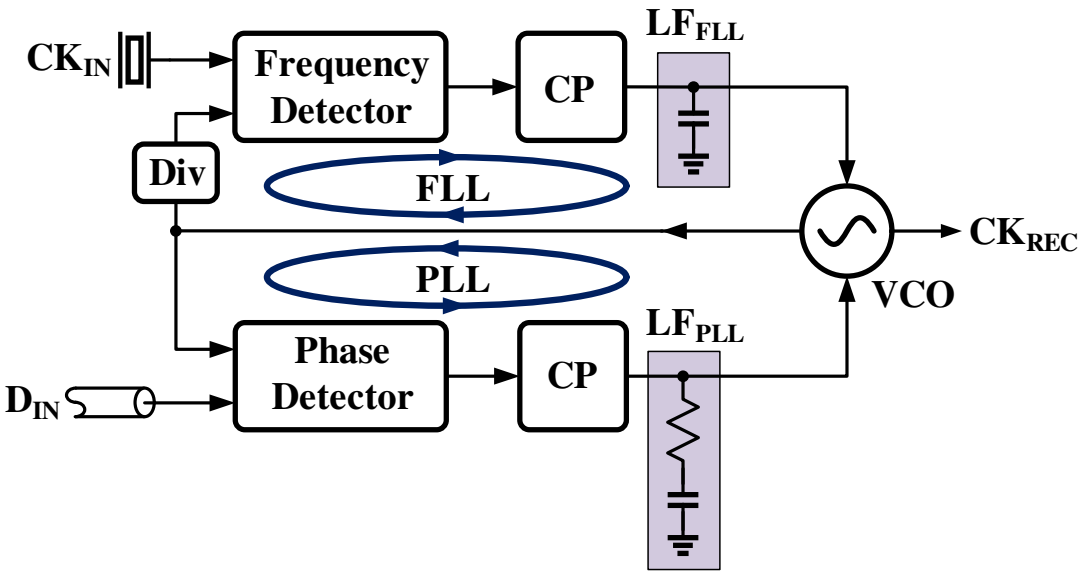


Fig. 1: Block diagram of a conventional CDR using a reference clock.

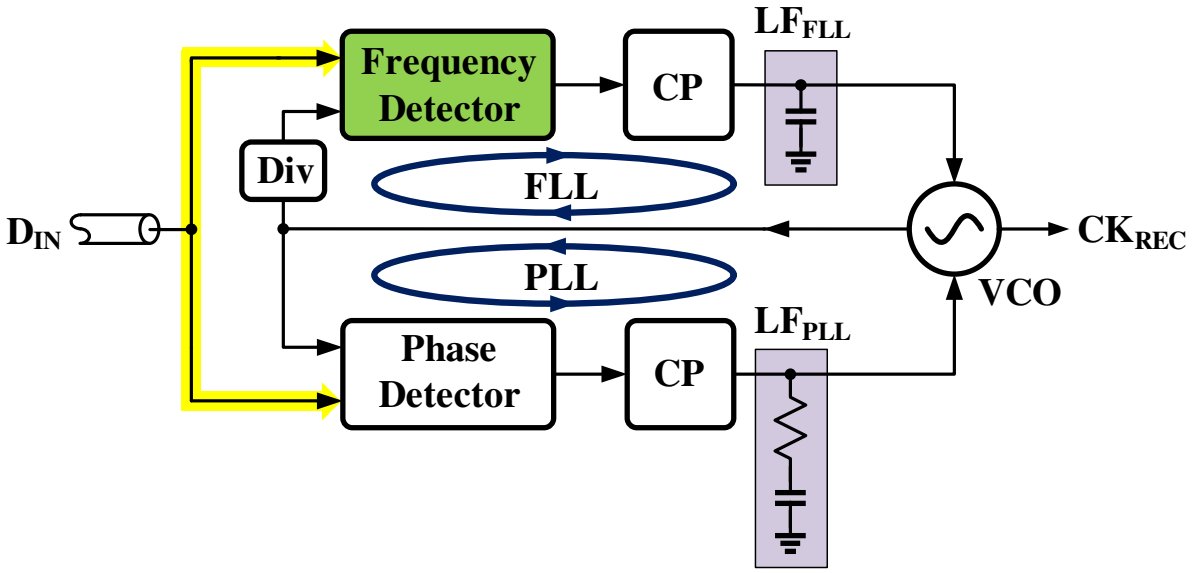


Fig. 2: Block diagram of a reference-less CDR.

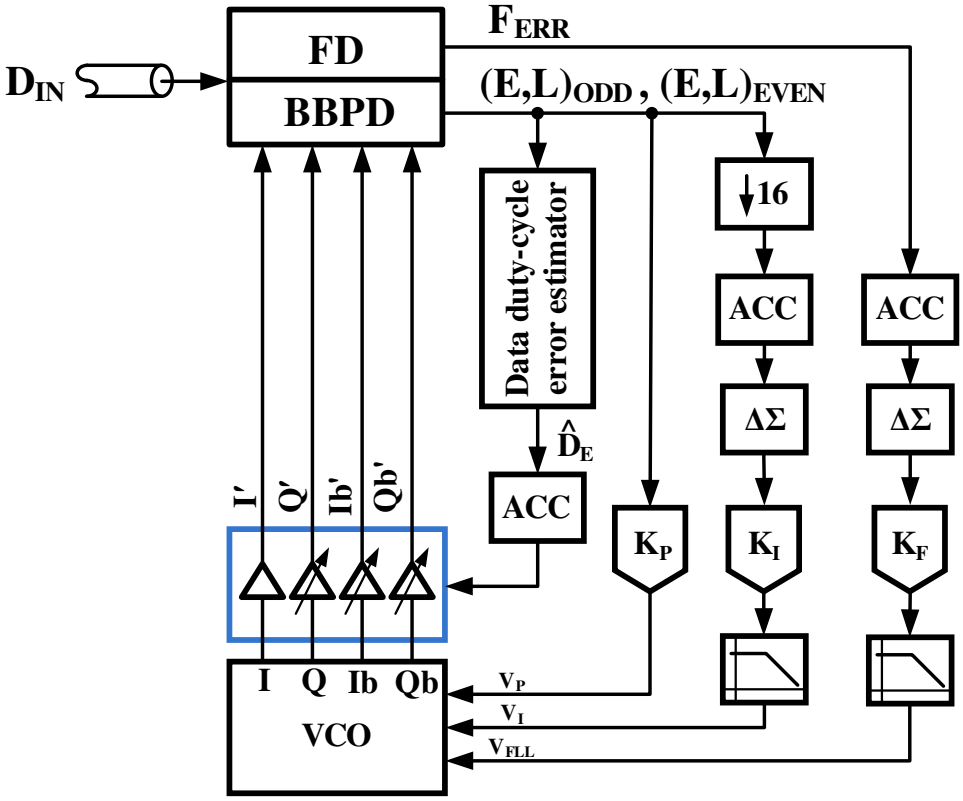


Fig. 3: Proposed CDR architecture.

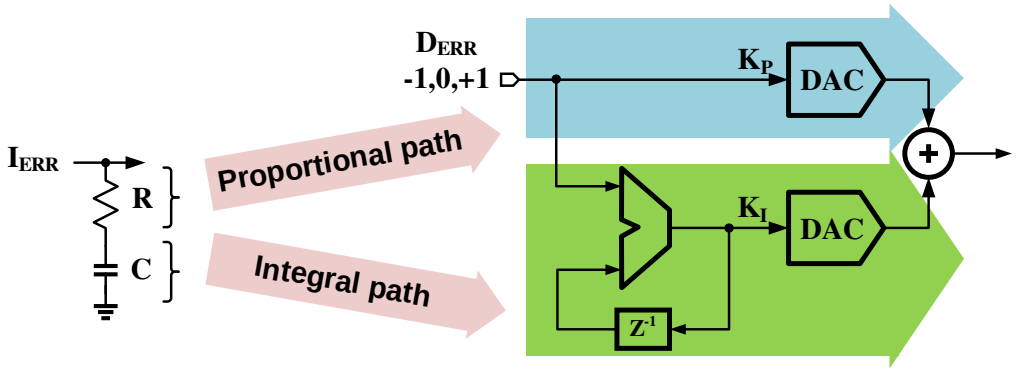


Fig. 4: Digital loop filter implementation.

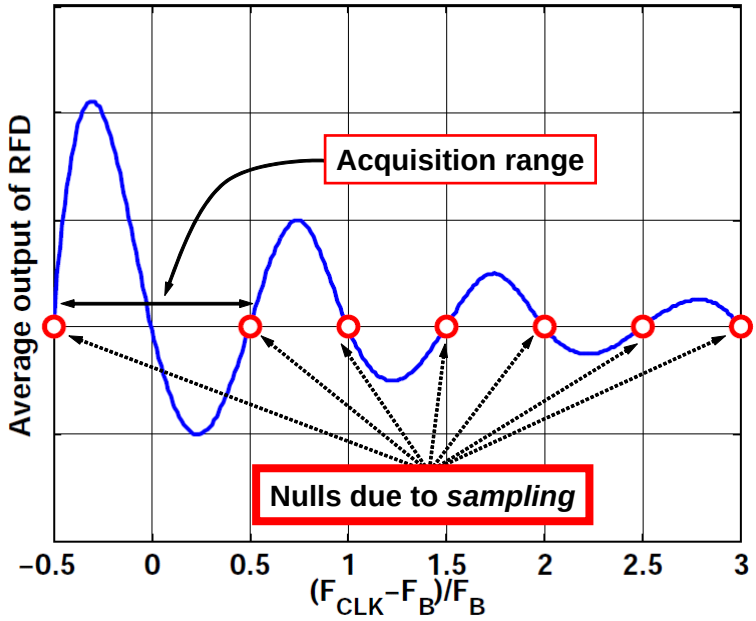
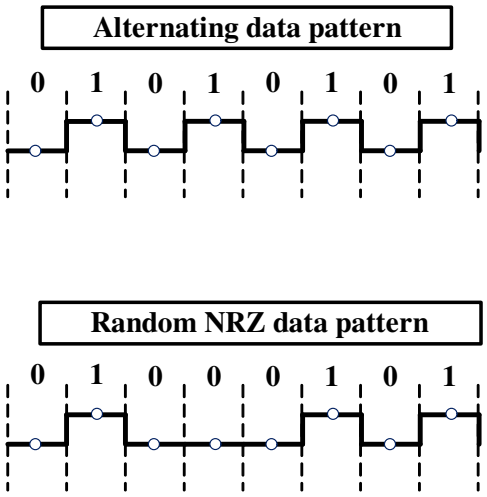


Fig. 5: RFD transfer characteristic.



Probability of Transition	Alternating Data	NRZ Random Data
0 → 0	0	0.25
0 → 1	0.5	0.25
1 → 0	0.5	0.25
1 → 1	0	0.25

Fig. 6: Transition density in alternating and random data patterns.

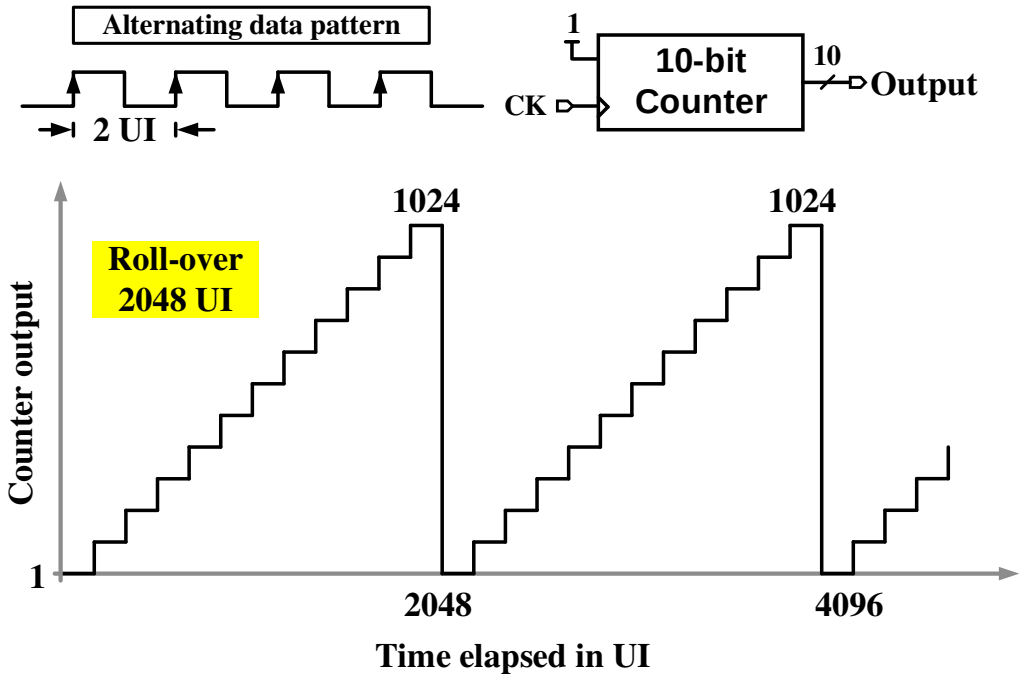


Fig. 7: 10-bit counter output clocked with alternating data.

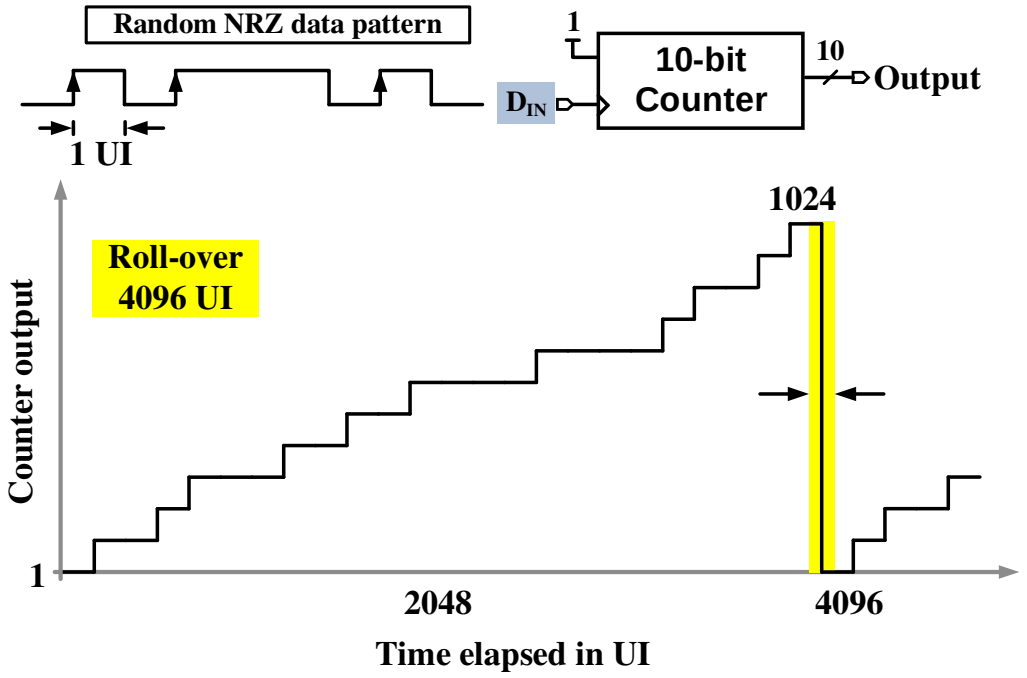


Fig. 8: 10-bit counter output clocked with random data.

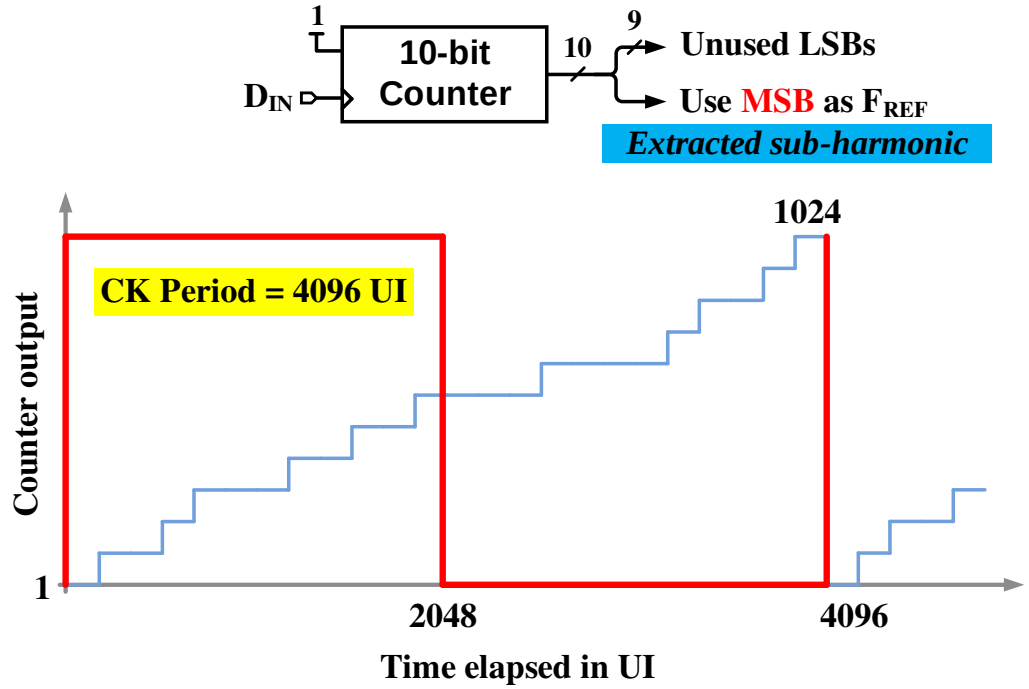


Fig. 9: MSB of the 10-bit counter output.

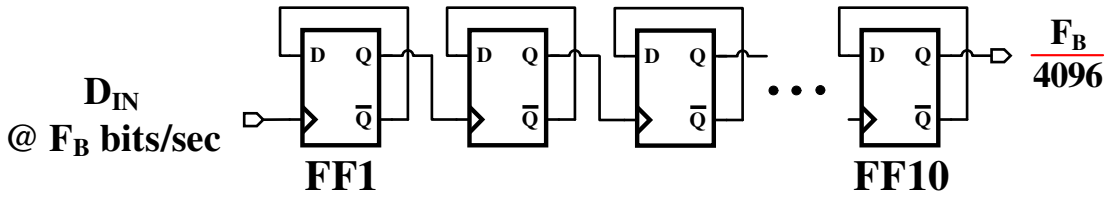


Fig. 10: Implementation of the high-speed 10-bit counter.

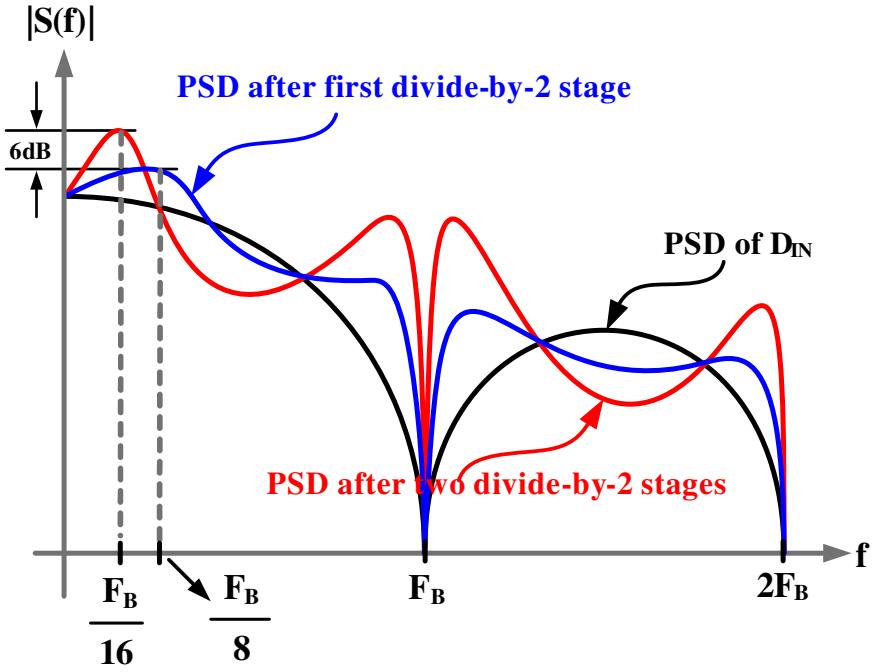


Fig. 11: PSD at the output of the first three divide-by-2 stages.

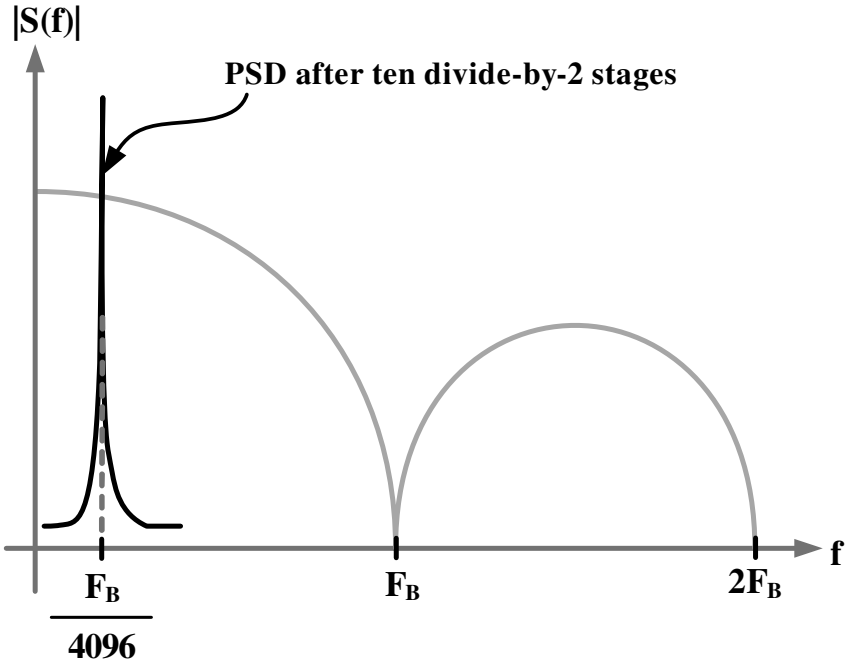


Fig. 12: PSD after ten divide-by-2 stages.

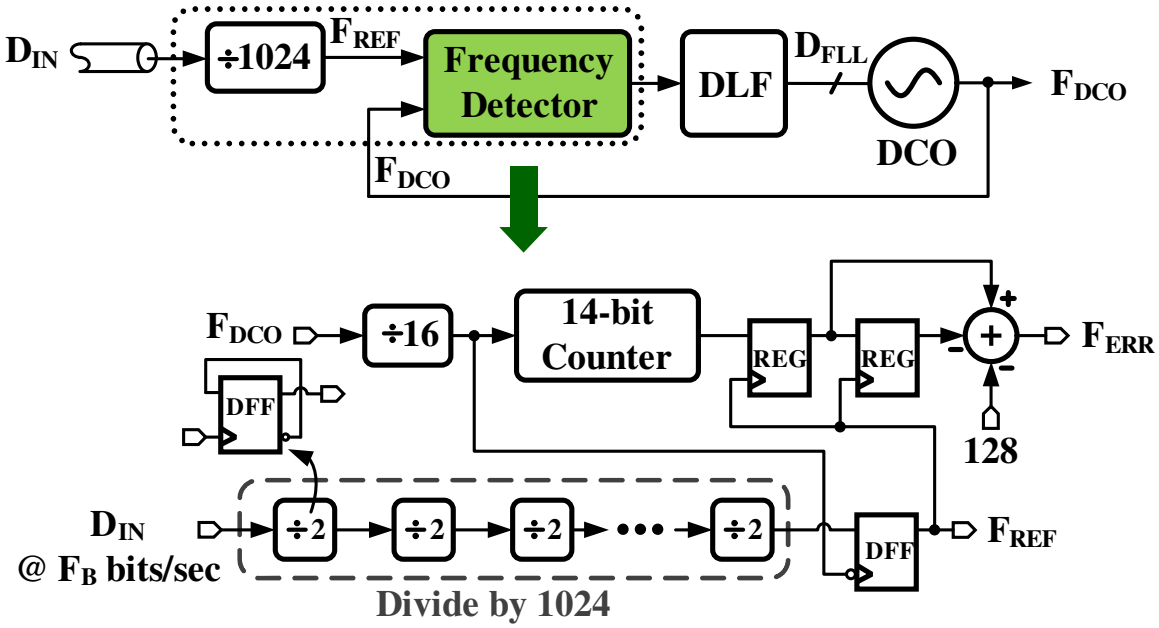


Fig. 13: Block diagram of the FLL and the schematic of the frequency detector.

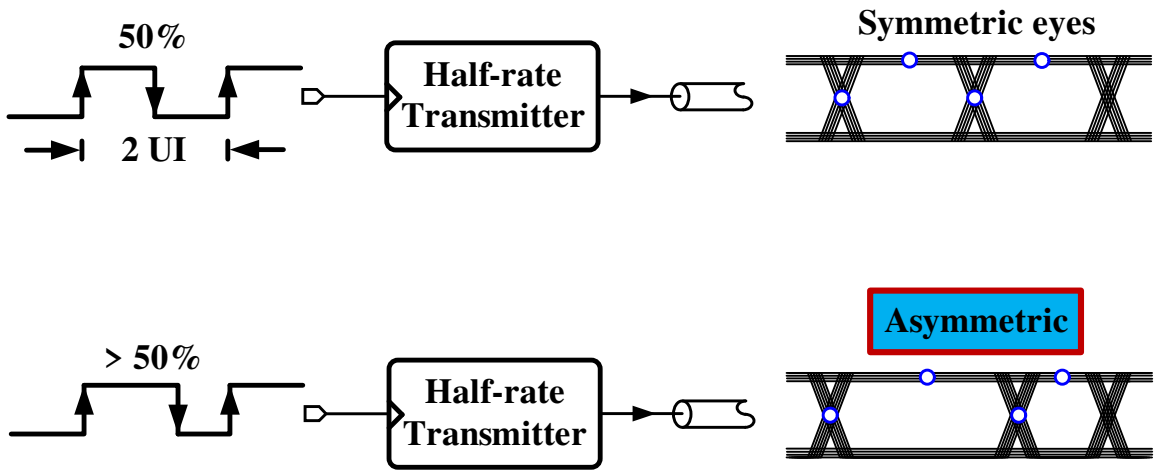


Fig. 14: Origin of duty-cycle error : Half-rate transmitter with and without clock duty-cycle error.

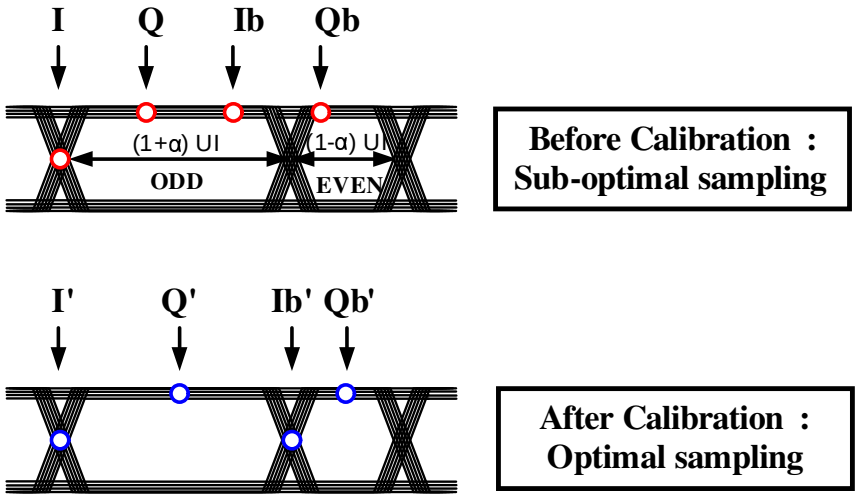
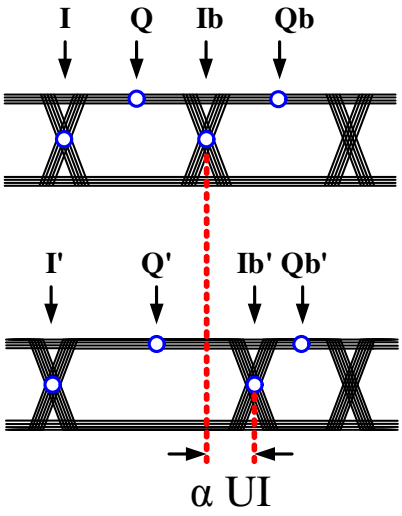


Fig. 15: Data/Edge sampling clocks before and after calibration in the presence of data duty-cycle error.



Clock Phase	Symmetric	Asymmetric	Phase shift (UI)
I	0	0	0
Q	0.5	0.5(1+α)	0.5α
Ib	1	1+α	α
Qb	1.5	1.5+0.5α	0.5α

Fig. 16: Required phase shift on sampling clocks I,Q,Ib,Qb with input data duty-cycle error = α UI.

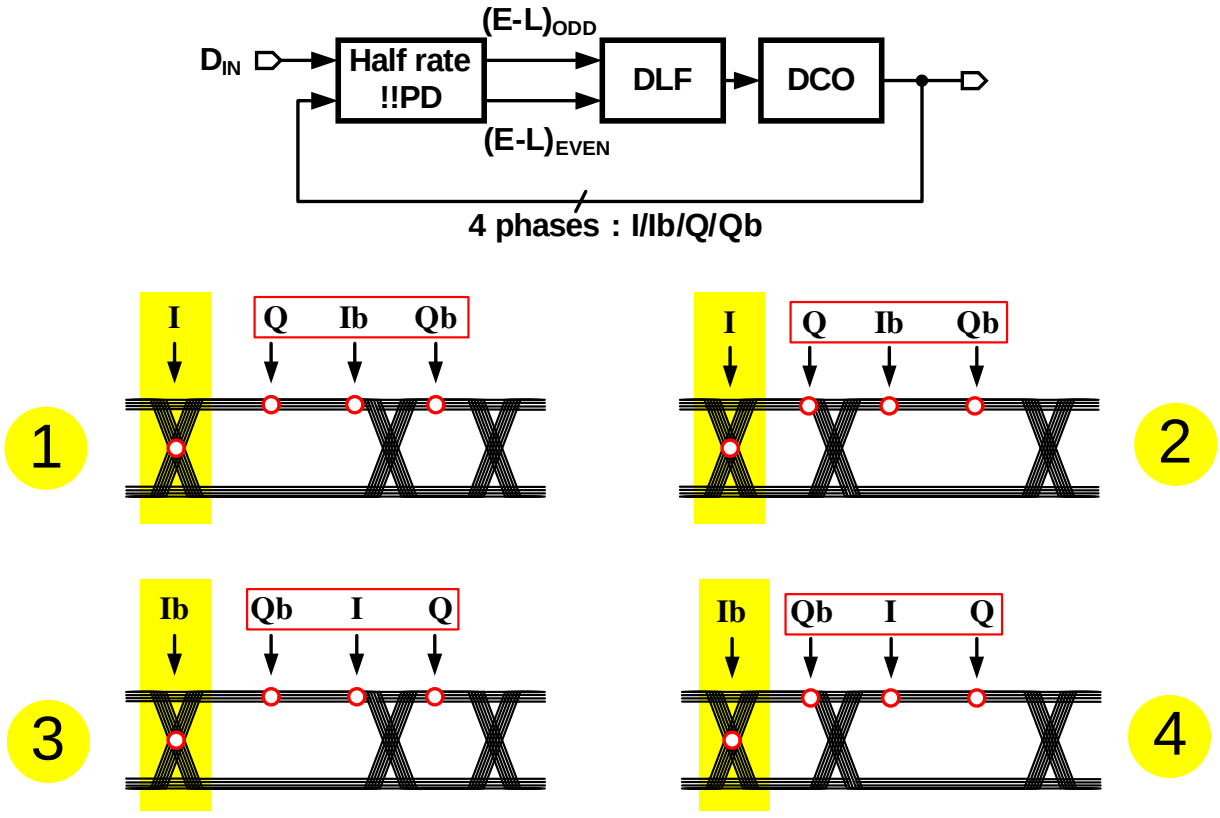


Fig. 17: Possible locking scenarios in a half-rate CDR.

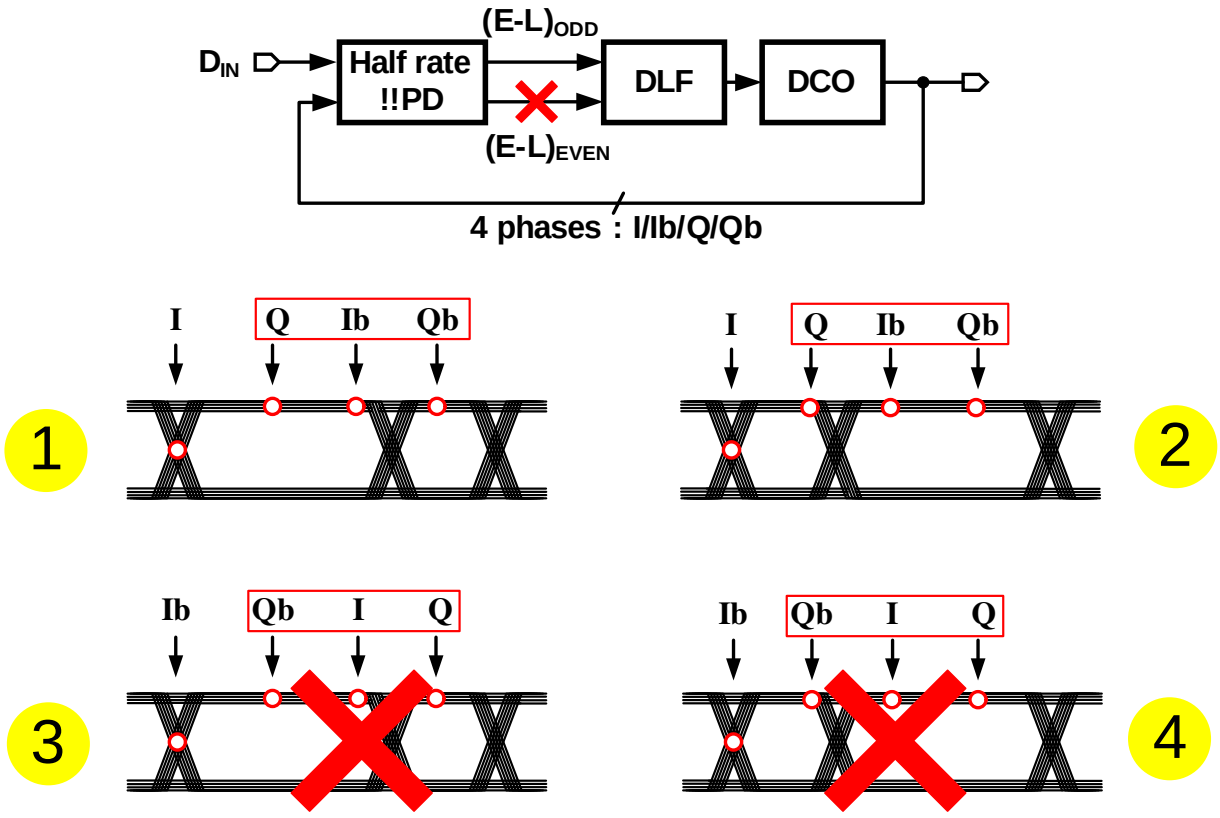


Fig. 18: Re-configured CDR to reduce the number of lock points.

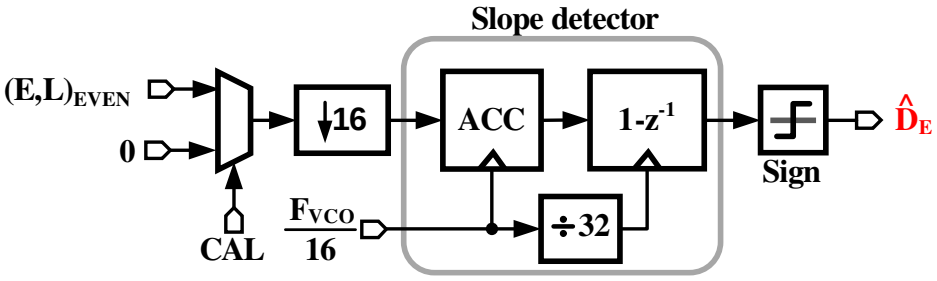


Fig. 19: Data duty-cycle estimator

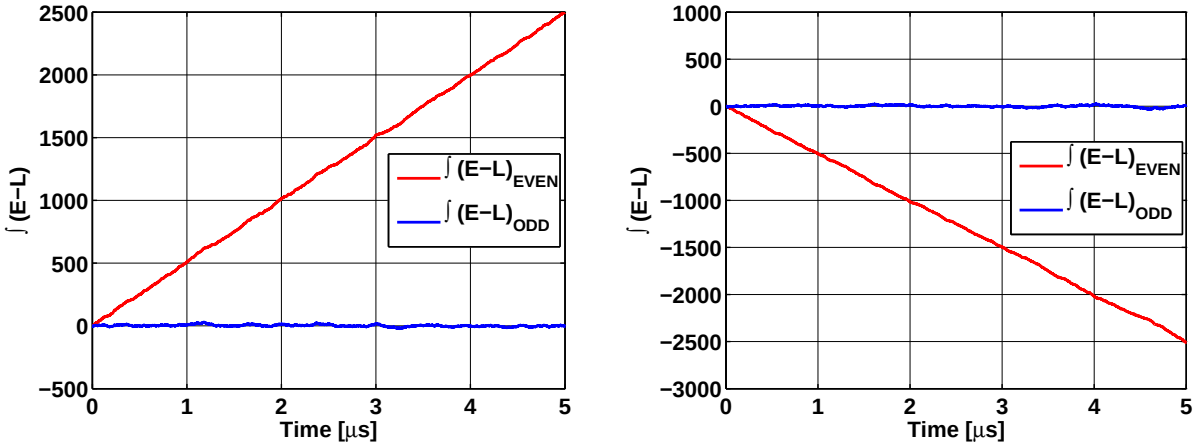


Fig. 20: Simulation results demonstrating that slope of accumulation of $(\text{E-L})_{\text{EVEN}}$ is indicative of the sign of the input data duty-cycle error when $(\text{E,L})_{\text{EVEN}}$ corresponds to a (a) *always early* and (b) *always late* case.

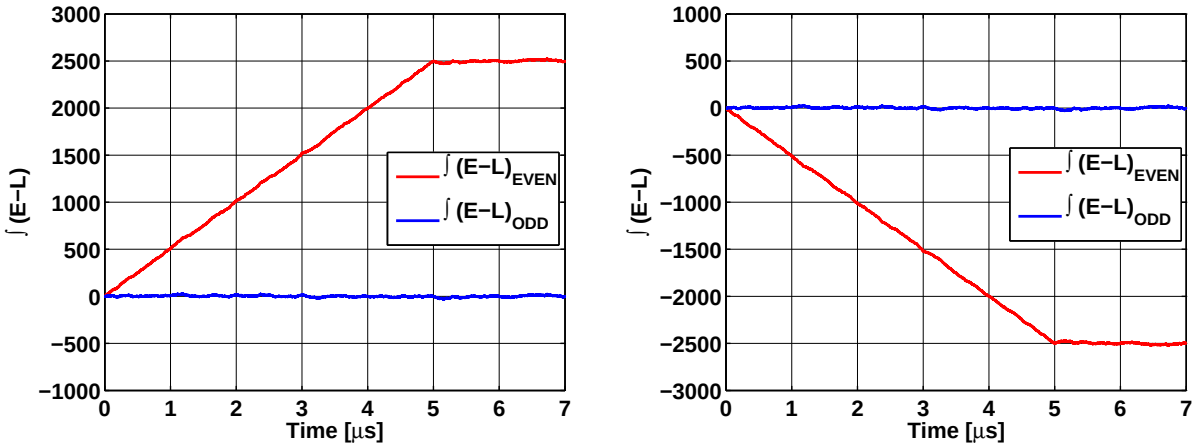


Fig. 21: Convergence of the clock-phase calibration algorithm.

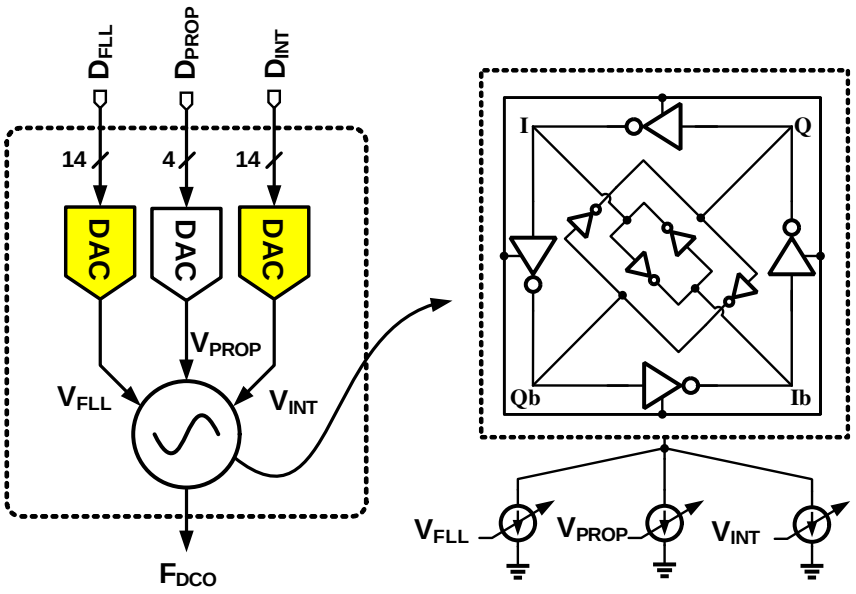


Fig. 22: Digitally controlled oscillator (DCO).

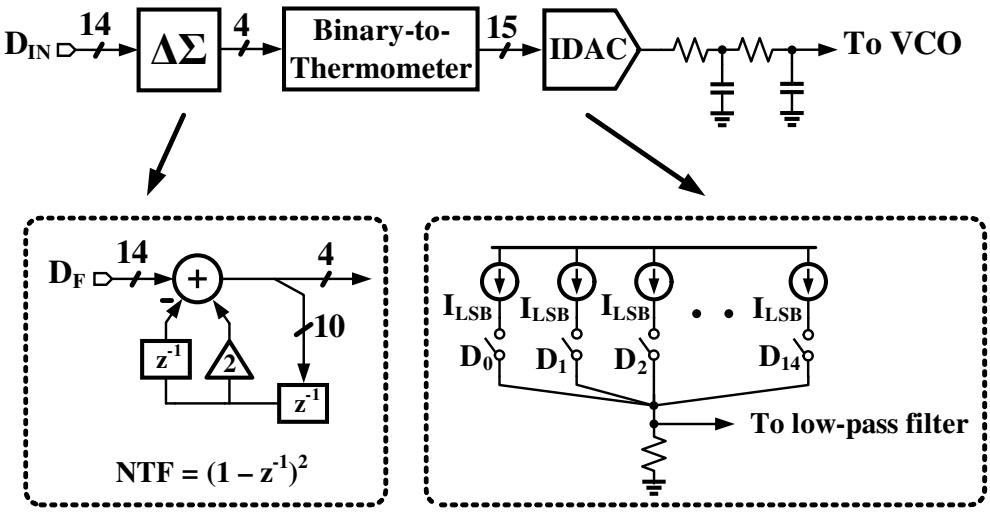


Fig. 23: $\Delta\Sigma$ DAC in both FLL and PLL paths.

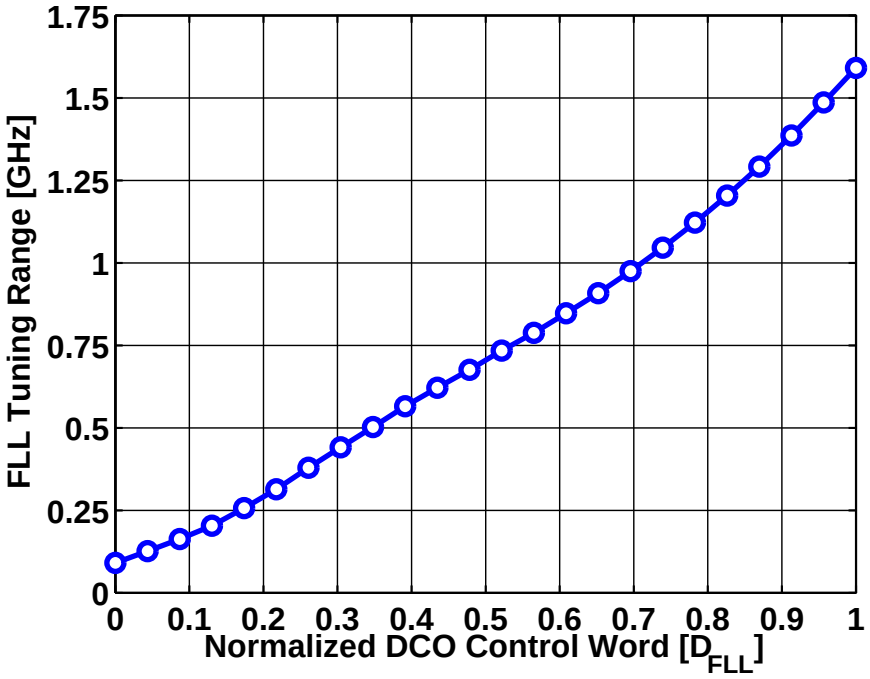


Fig. 24: FLL controlled tuning curve of the DCO.

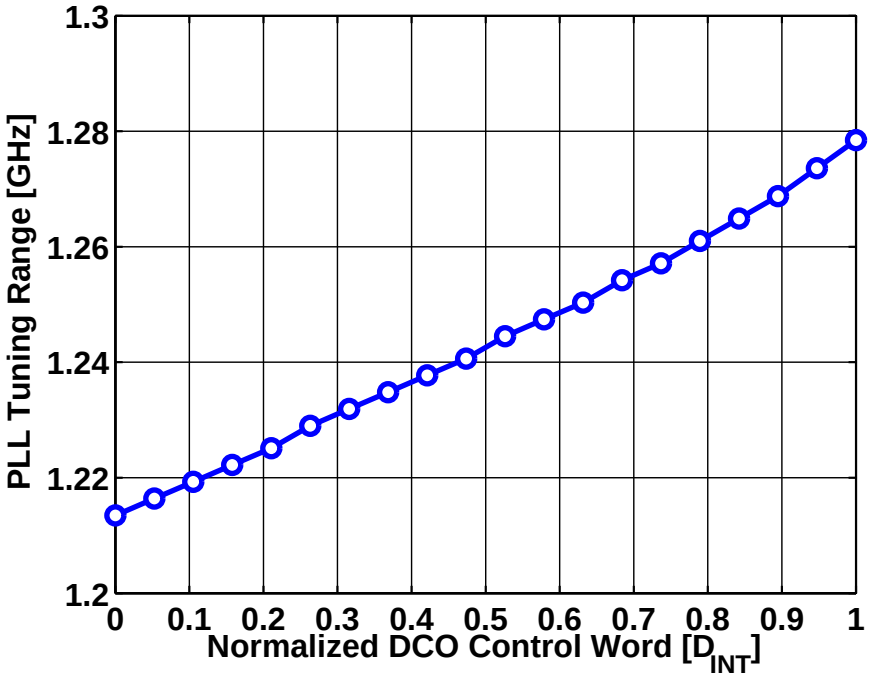


Fig. 25: Digital integral path (in PLL) controlled tuning curve of the DCO.

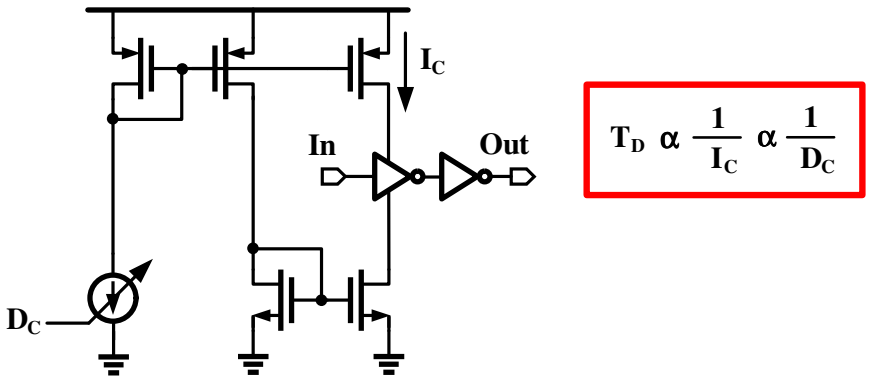


Fig. 26: Conventional digital-to-delay converter (DDC).

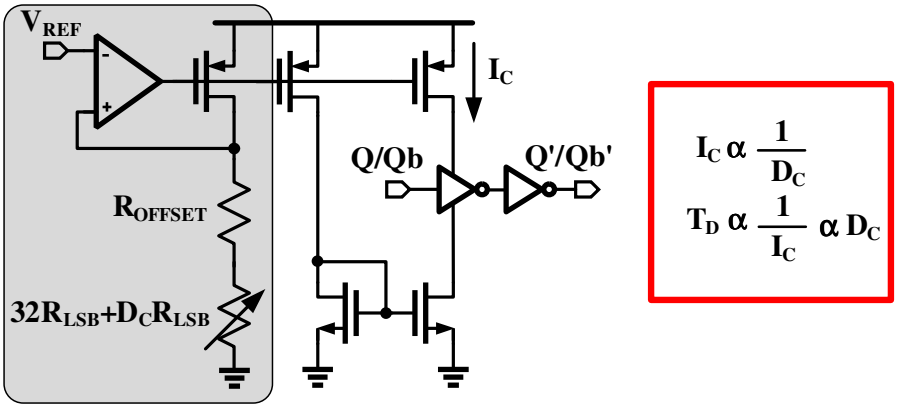


Fig. 27: *Linearized* digital-to-delay converter (DDC).

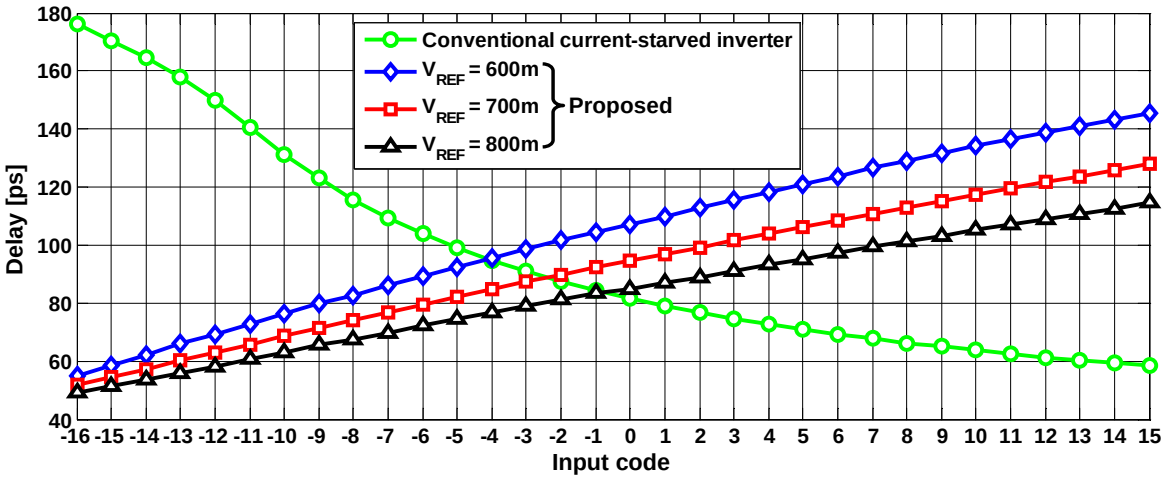


Fig. 28: Simulated DDC characteristic.

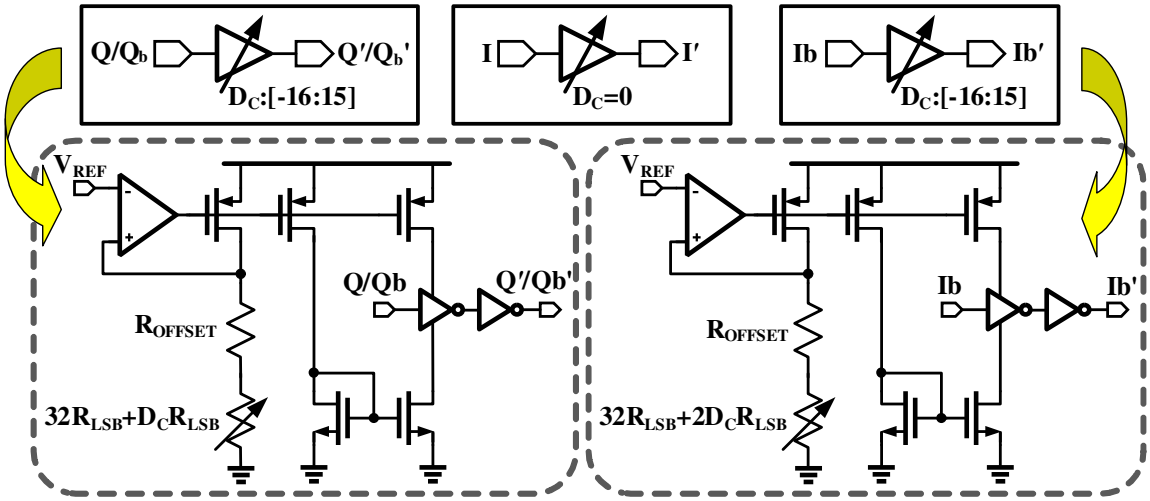


Fig. 29: Schematic of all the 4 DDCs used to phase shift I/Q/Ib/Qb.

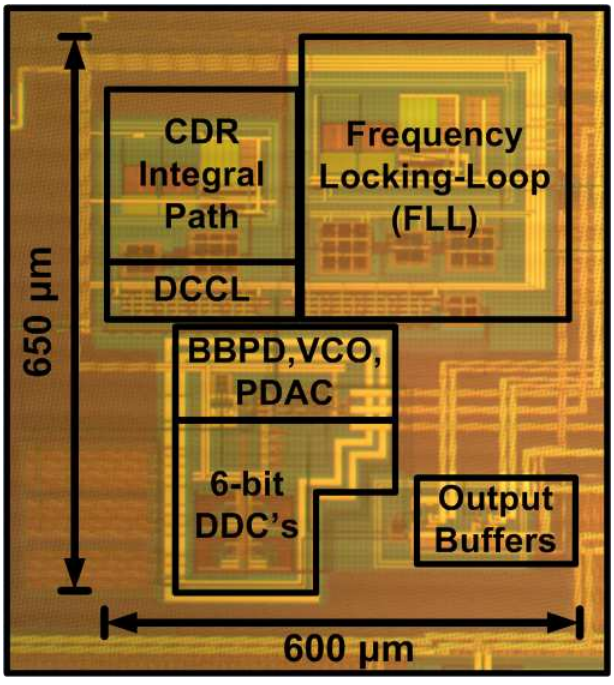


Fig. 30: Die micrograph.

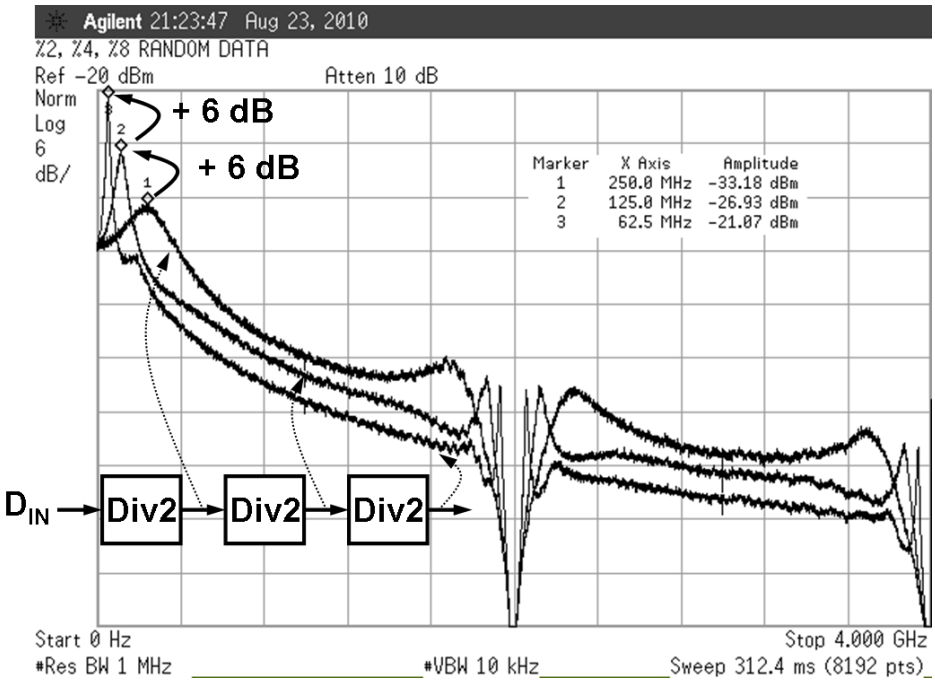


Fig. 31: Measured PSD's of first three divide-by-2 stages with 2Gb/s random data.

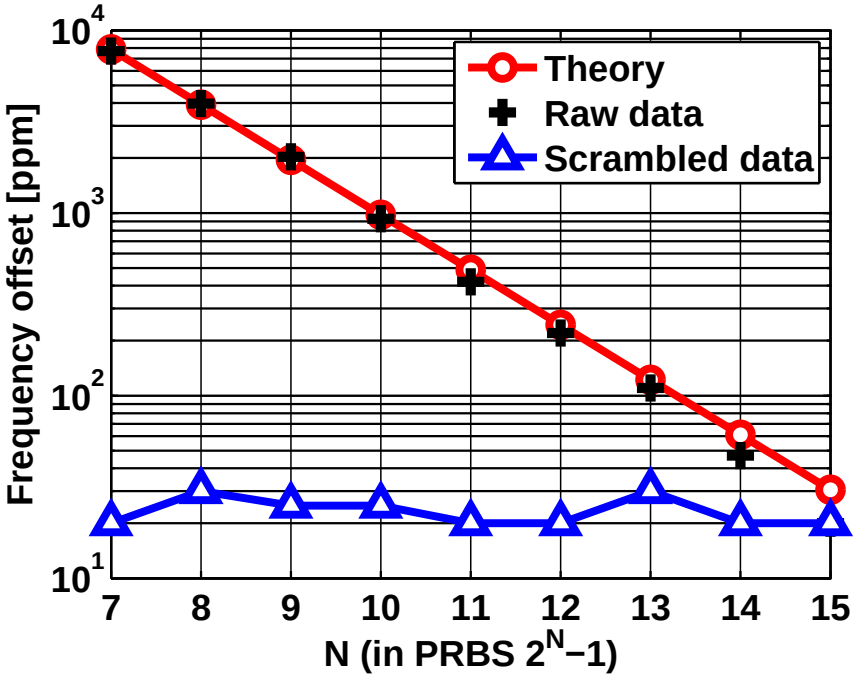


Fig. 32: Measured FLL offset with different input PRBS pattern.

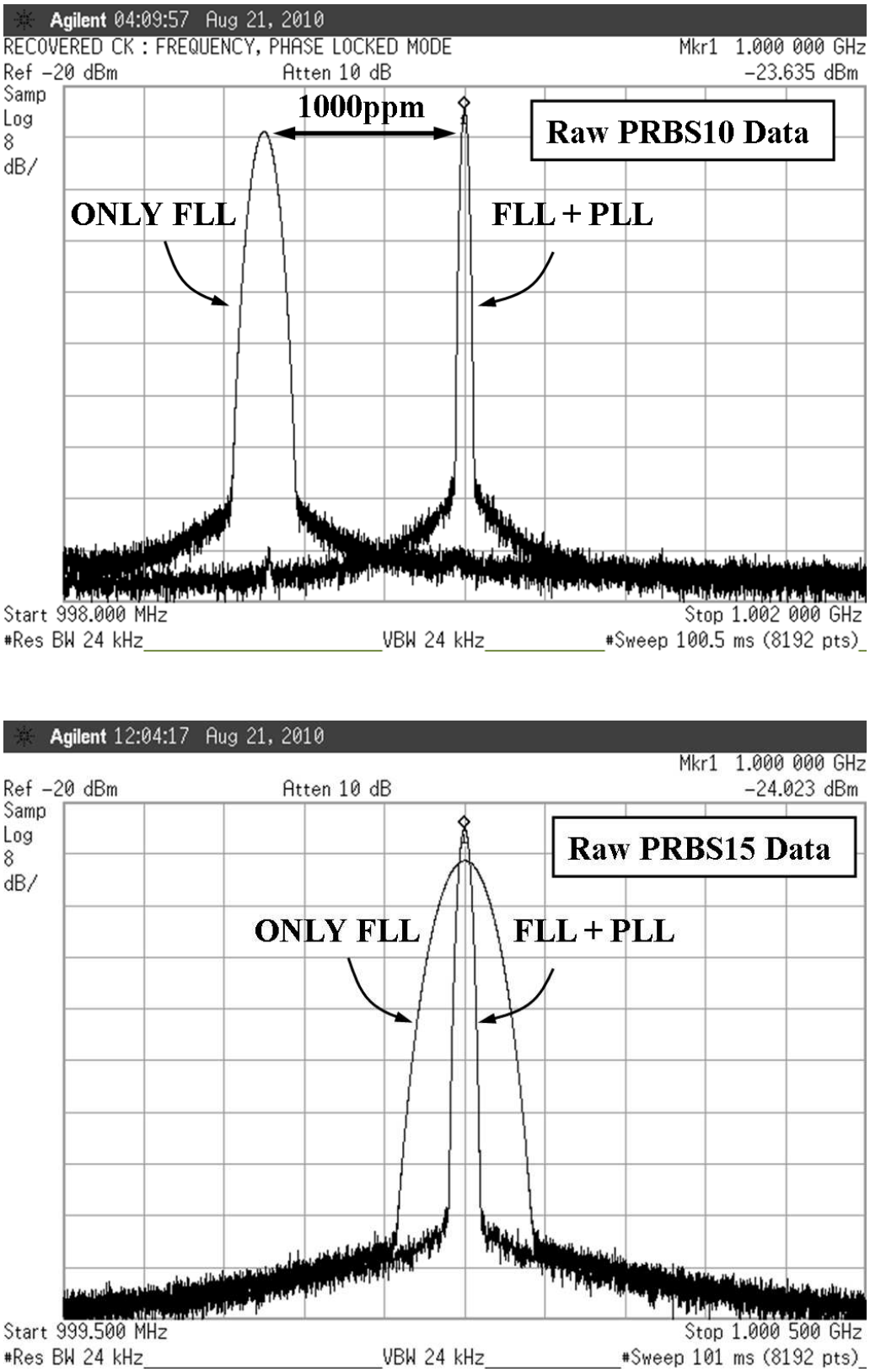


Fig. 33: FLL/PLL clock spectrums with PRBS10 and PRBS15 input patterns.

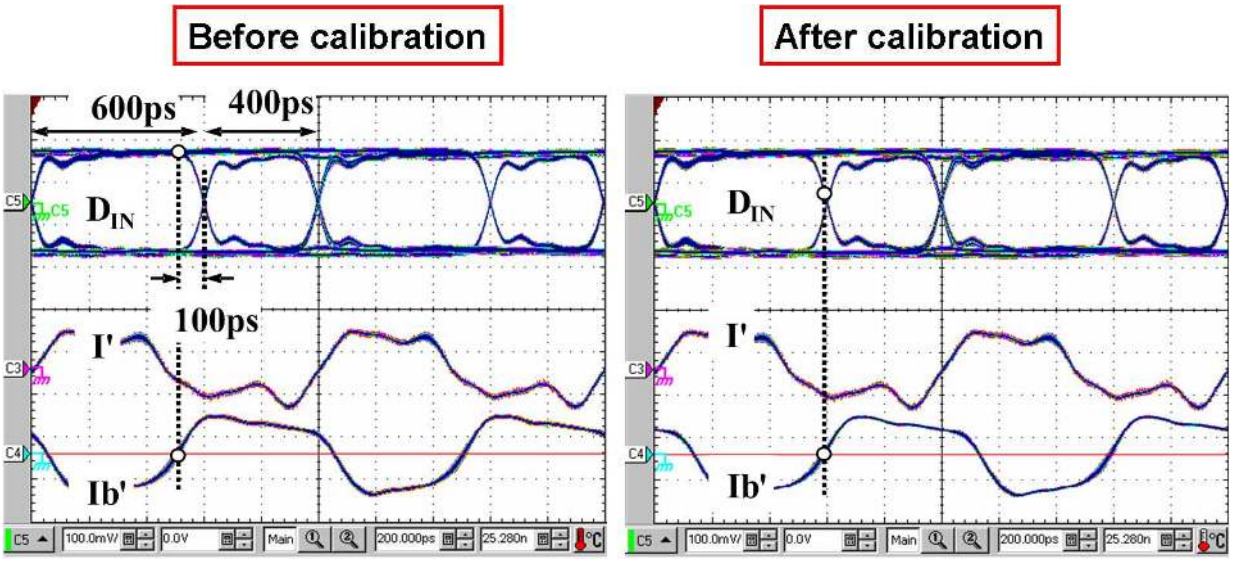


Fig. 34: Edge sampling clock phases I/Ib before and after calibration with 20% duty-cycle error.

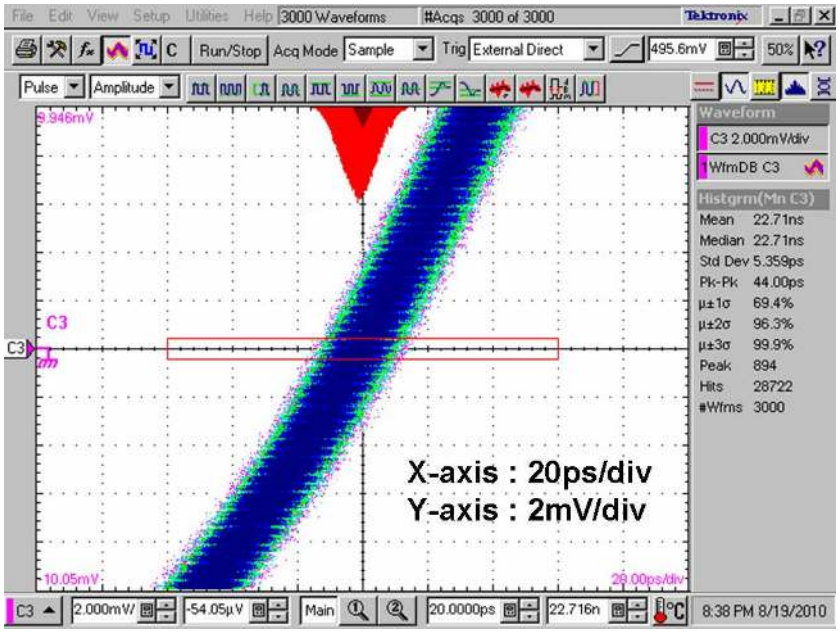


Fig. 35: Recovered clock jitter with a PRBS10 input pattern.

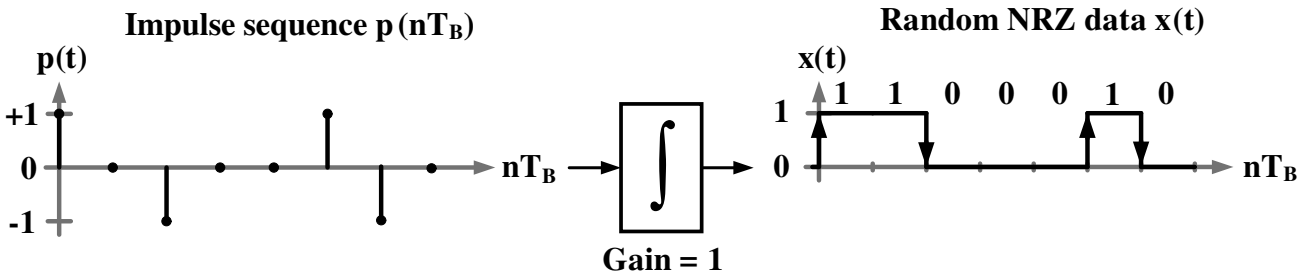


Fig. 36: Random NRZ data stream ”1100010” generated from impulse stream p(t).

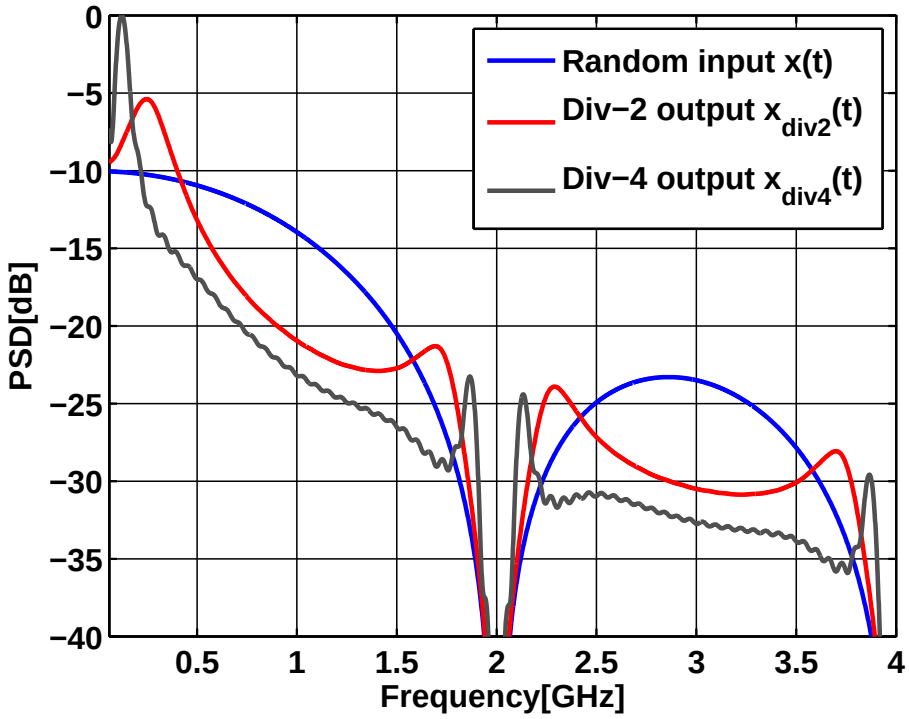


Fig. 37: PSD of the first two divider stages for a 2 Gb/s random input data.

TABLE I: Digital CDR Performance Summary

Technology	0.13μm CMOS
Supply voltage	1.2V
Data rate @ V_{DD}=1.2V	0.5Gb/s-2.5Gb/s
Data rate @ V_{DD}=0.8V	0.2Gb/s-1.0Gb/s
At 2Gb/s	
BER	$< 10^{-12}$
Jitter (PRBS10)	5.4ps,rms
	44ps,pk-pk
Power	6.1mW
FOM	3.05mW/Gb/s
Die area	0.39mm^2

TABLE II: Performance Comparison

	ISSCC05 [6]	ISSCC09 [17]	ISSCC06 [8]	JSSC06 [7]	ISSCC07 [16]	This Work
Technology	0.13μm	65nm	0.25μm	0.25μm	0.13μm	0.13μm
Supply voltage [V]	3.3	1.2	2.5	1.8	1.2	0.8/1.2
Architecture	Full-rate	Full-rate	Full-rate	Full-rate	Full-rate	Half-rate
Filter	Analog	Analog	Digital	Analog	Digital	Digital
Acquisition	Reference-less	Reference-less	Reference-less	Reference-less	Reference	Reference-less
Jitter [ps_{rms}/ps_{pp}]	N/A	9.7/53.3	1.2/N/A	6.4/48.9	7.2/47.2	5.4/44
Power	775.5mW @ 2.5Gb/s	20.6mW @ 0.65Gb/s	425mW @ 2.5Gb/s	95mW @ 3.125Gb/s	13.2mW @ 2.5Gb/s	6.1mW @ 2Gb/s
Power FOM [mW/Gb/s]	310.2	31.7	170	30.4	4.72	3.05