19.6 A 0.5-to-480MHz Self-Referenced CMOS Clock Generator with 90ppm Total Frequency Error and Spread-Spectrum Capability

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The quartz crystal (XTAL) oscillator is one of the last components in electronic systems that has yet to be integrated. Consequently, integrating crystal oscillators (XOs) has become a research target for the developers of MEMS microresonators. Recent and representative examples of MEMS oscillators include [1] and [2]. Unfortunately, MEMS microresonators introduce certain challenges including limited power-handling capability [2]. The limitations of MEMS have resulted in recent work, e.g., [3] and [4], exploring the limits of compensated CMOS oscillators as an alternative solution. The advent of RF CMOS circuits and associated advances in CMOS process technology have enabled the development of low-noise integrated *LC* oscillators (LCOs) [5], which are suitable for replacing XOs in USB applications [3]. This work demonstrates a self-referenced CMOS LCO, or CMOS harmonic oscillator (CHO), that exhibits 90ppm total frequency error over process, bias and temperature, thus making it suitable for replacing XOs in many applications. Additionally, the clock generator can be configured to produce a number of different output frequencies, has 1/4 of the frequency error of the oscillator in [3] and includes a direct modulation technique enabling SSCG.

Figure 19.6.1 illustrates the CHO, which exhibits a self-oscillation frequency of 960MHz. A 13b binary-weighted array of MiM capacitors and ring-transistor switches enables the oscillation frequency to be trimmed ±6% with 15ppm resolution. The trimming coefficient is determined during test via an on-chip frequency-locked loop (FLL), in which deep counters for the CHO and a precision reference clock discriminate the frequency error and update the CHO trimming coefficient, as described in [3]. The FLL is controlled by on-chip logic that converges to the optimal trimming coefficient within 100ms by using a binary search algorithm. Additionally, the thin-film capacitor array enables direct modulation of the CHO frequency via a frequency-divided image of itself, thus permitting SSCG without a modulating PLL. The spread rate and depth are controlled digitally by the divide ratio utilized to generate the modulating clock and the capacitor array step size, respectively. The TC of the CHO, which is nearly linear and negative due to the coil loss [3], is compensated via a programmable 6b accumulation-mode MOS (A-MOS) varactor array. When compensation is enabled, the appropriate varactors are connected to a positive linear temperature-dependent voltage, $v_{ctrl}(T)$, and the remaining varactors are connected to the 2.5V power supply. Amplitude control (AC) and common-mode control (CMC) loops minimize frequency drift due to bias variation and device degradation. Long-term frequency drift, or aging, can originate from oxide breakdown and hot carrier mechanisms. Addressing these mechanisms, the AC loop limits the maximum voltage excursion across the passive and active devices, and the CMC loop prevents frequency drift due to device threshold voltage shift induced by hot carriers trapped in the gate oxide. As shown in Fig. 19.6.1, the AC loop and the CMC loop modulate the bias current in the CHO via a pMOS tail source and nMOS tail sink, respectively. Control loop convergence is ensured as the bandwidth of the CMC loop is an order-of-magnitude greater than that of the AC loop. The control loops are referenced to programmable and temperature-independent voltages, v_{ac} and v_{cmc}, respectively.

The output clock is derived from the CHO via frequency division. The chip-level functional schematic is shown in Fig. 19.6.2. It includes a multi-path configurable divider matrix capable of synthesizing frequencies that are integer fractions of the reference frequency. Supported divide ratios range from 2 to 2000 and are used to generate the output signal as well as the modulating signal for SSCG. The CHO, which is buffered by a differential to single-ended (D2S) converter, and the divider matrix are biased from an internal 2.5V rail, while the configurable output drivers are biased from the external 3.3V supply. The 2.5V rail is derived from the 3.3V supply via a band-gap referenced LDO as shown in Fig. 19.6.2. Temperature-dependent current generators, I_{CTAT} and I_{PTAT}, drive the input of a transimpedance amplifier and are used to generate the linear temperature-dependent compensation voltage, $v_{ctrl}(T)$, for the CHO while the programmable feedback resistor enables the temperature dependence of $v_{ctrl}(T)$ to be controlled precisely. The digital section includes an I²C interface, the FLL, the SSCG logic and a controller for a 96b multi-time programmable (MTP) NVM. Trimming and configuration coefficients are stored in the NVM and are loaded at power on reset.

The clock generator was trimmed and configured to 24MHz via the I²C interface, corresponding to a frequency division ratio of 40 from the 960MHz CHO. This frequency was selected to compare performance to a 4-pin XO and a 1*x* ring-VCO PLL mated to a 24MHz XTAL. Figure 19.6.3 illustrates the SSB phase noise PSD for all 3 implementations, which were measured using a spectrum analyzer with a -140dBc/Hz noise floor. Despite significant differences in the *Q* of the resonant networks, the CHO is within 11dB of the XO for all frequency offsets from the carrier greater than 1kHz and within 6dB of the XO at offsets greater than 100kHz. The 1*x* PLL tracks the XO within the PLL loop bandwidth, but exceeds the CHO phase noise for large offsets by over 20dB, where the output phase-noise path tracks the ring VCO. In Fig. 19.6.4, the period jitter of the 1*x* PLL is the worst at 9.9ps$_{rms}$. The CHO exhibits the best period jitter at 6.5ps$_{rms}$, though this performance is due to differences in output buffer drive strength and the associated rise time between the CHO and XO implementations. As shown in Fig. 19.6.4, the XO rise time is slower than the other implementations. Figure 19.6.5 shows the total frequency error of all 3 implementations where the error of the CHO-referenced clock generator is +90ppm to -30ppm including supply variation of ±10% and temperature variation from 0 to 70°C. The nominal frequency trim was executed by the FLL at 35°C and is in error by 5ppm. In comparison, the CMOS implementation in [4] exhibits 3100 and 8400ppm frequency error due to supply and temperature respectively. The MEMS-referenced approach in [1] exhibits 39 or 334ppm frequency error over temperature, depending on the compensation technique.

SSCG is achieved without the use of a spreading PLL; instead, the thin-film capacitor array is directly modulated at a rate derived from the CHO itself. Figure 19.6.6 illustrates a 12.2dB power reduction at the 7th harmonic of the clock configured to 24MHz where the modulation rate is 30kHz and spread depth is 1%, or 240kHz. A die micrograph of the clock generator is shown in Fig. 19.6.7. It occupies 2.25mm² in a dual gate (DG) 0.25μm, 1P4M process technology that includes MiM and 2μm last-metal options. Unloaded, the clock generator dissipates 49.5mW when the divider matrix is configured to output 24MHz. In comparison, the XO and 1*x* ring-VCO PLL at the same frequency dissipate 23.1mW and 62.7mW, respectively.

References:

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[2] Y-W. Lin, S. Lee, S-S. Li et al., "60-MHz Wine-Glass Micromechanical-Disk Reference Oscillator," *ISSCC Dig. Tech. Papers*, pp. 322-323, 2004.
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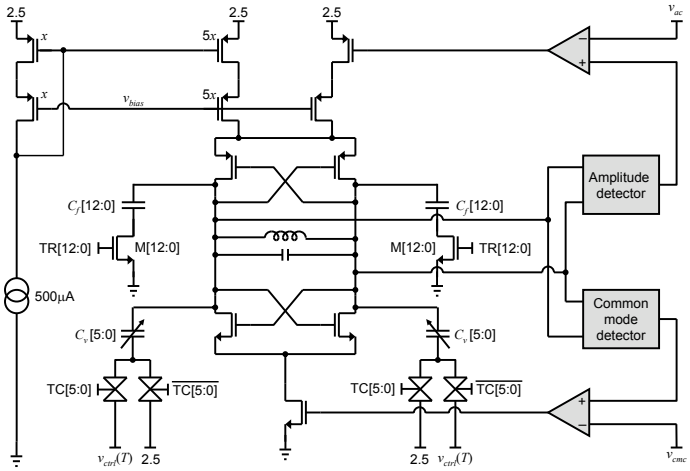

Figure 19.6.1: Schematic of the CHO illustrating the 13b fixed capacitor array for frequency trimming and SSCG, C_f[12:0], the varactor temperature compensation array, C_v[5:0], and amplitude and common-mode control loops.

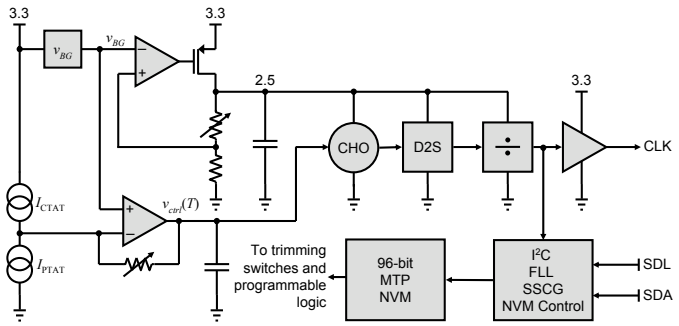

Figure 19.6.2: CHO-referenced clock generator chip-level functional schematic.

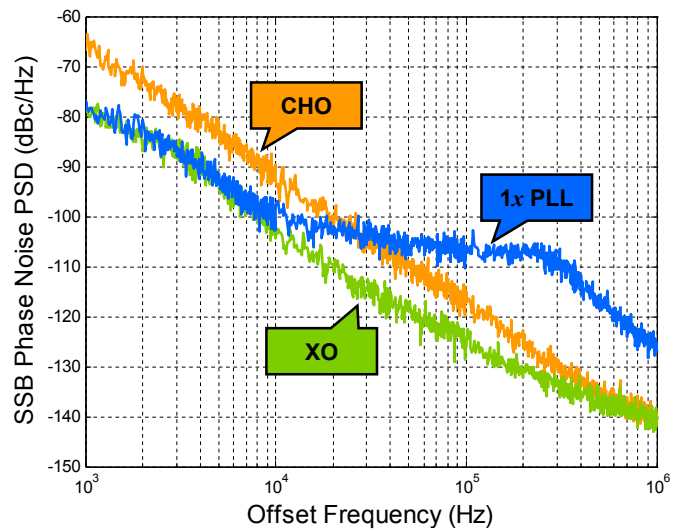

Figure 19.6.3: SSB phase noise PSD of the CHO configured to 24MHz compared to a 24MHz XO and a 1x ring-VCO PLL referenced to a 24MHz XTAL.

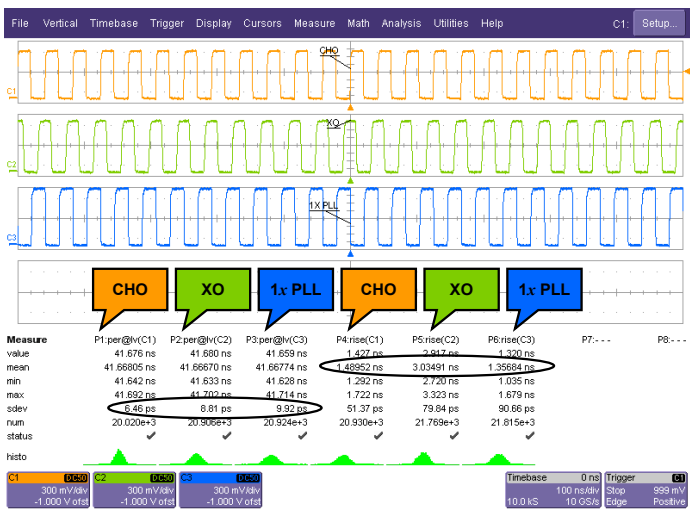

Figure 19.6.4: RMS period jitter (sdev of period) and rise time of the CHO configured to 24MHz compared to a 24MHz XO and a 1x ring-VCO PLL referenced to a 24MHz XTAL.

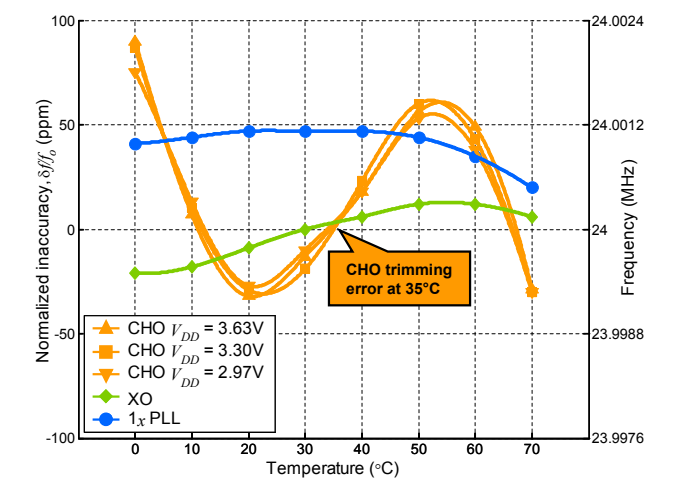

Figure 19.6.5: Total frequency error of the CHO configured to 24MHz including supply variation of ±10% from nominal and temperature variation from 0 to 70°C as compared to a 24MHz XO and a 1x ring-VCO PLL referenced to a 24MHz XTAL.

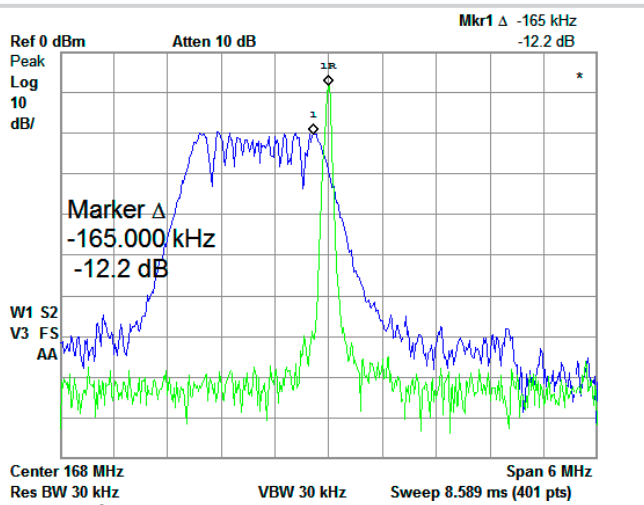

Figure 19.6.6: Spread spectrum power reduction by 12.2dB at the 7th harmonic of the clock generator configured to 24MHz and via direct downspread modulation of the fixed capacitor array at a 30kHz rate and 1% modulation depth (240kHz).

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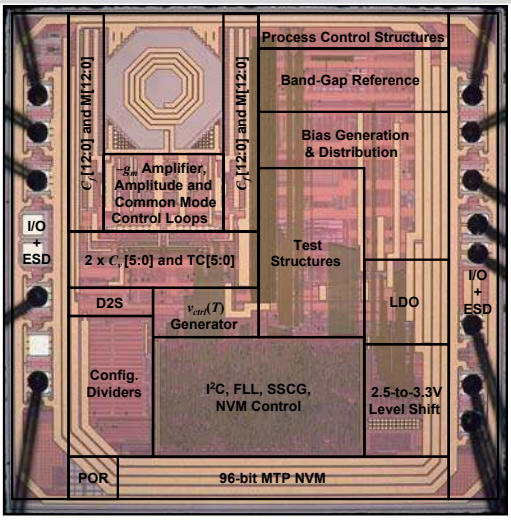

Figure 19.6.7: Die micrograph of the configurable self-referenced CHO clock generator in a DG 1P4M 0.25µm CMOS process technology with MiM and 2µm last metal options.

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