

A 0.5 V, 1.2 mW, 160 fJ, 600 MS/s 5 bit Flash ADC

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Abstract—An ultra-low voltage operation of 0.5 V, 5-bit Flash ADC has been developed and achieved an ENOB of 4.2-bit at a conversion rate of 600 MS/s. It consumes only 1.2 mW and attained an ultra-low FoM of 160 fJ/conv. steps at an ERBW of 200 MHz. A forward body bias technique and gate-interpolated double-tail latched comparator with variable delay method to compensate the mismatch voltage are introduced.

I. INTRODUCTION

Five to seven-bit, several hundred MS/s to around one GS/s ADCs are required for disk drive front-ends, high speed backplane, ultra-wideband receivers, and millimeter-wave receivers.

An ultra-low power operation is strongly required for the portable applications, ubiquitous wireless sensor systems, and the green IT regulation. Furthermore, a low resolution and low latency flash ADC is an important circuit block for other higher resolution ADCs such as a delta-sigma ADC, sub-ranging ADC, and pipeline ADC.

A low voltage operation is the most efficient way to reduce the power consumption and the challenges to realize low voltage operation for analog circuits and data converters will become more important along with further technology scaling where the conventional analog circuit technique will lose its validity. Therefore, we should investigate the use of low voltage operation to reduce the FoM of an ADC like digital circuits.

This paper describes the strategy to reduce the FoM of an ADC by reducing the operating voltage and the challenge for low voltage analog circuit design. The 5-bit flash ADC fabricated in 90 nm CMOS realizes an ultra-low voltage operation of 0.5 V and consumes very low power, 1.2 mW, at a conversion rate of 600 MS/s. An ENOB of 4.2-bit and an ultra-low FoM of 160 fJ/conv. step have been attained.

II. STRATEGY FOR LOW-VOLTAGE OPERATION

The FoM of a flash ADC is

$$\text{FoM} = \frac{P_d}{f_c \times 2^{\text{ENOB}}} \quad (1)$$

where P_d is the power dissipation of the ADC, f_c is the conversion frequency, and ENOB is the effective number of bits.

If E_c is the energy consumption for each comparator and followed logic circuits, equation (1) yields

$$\text{FoM} = \frac{f_c \times E_c \times 2^N}{f_c \times 2^{N-\Delta\text{ENOB}}} = E_c 2^{\Delta\text{ENOB}} \quad (2)$$

where ΔENOB is a reduction of ENOB from the ideal value. Therefore, reductions of E_c and ΔENOB are essential to attain low FoM [1].

The E_c can be expressed as the following with consideration of the sub-threshold leakage current.

$$E_c = C_c V_{DD}^2 + \frac{V_{DD} \cdot I_c \exp\left(-\frac{V_T}{S}\right)}{f_c} \quad (3)$$

where C_c is the unit capacitance for a comparator, V_{DD} is the supply voltage, I_c is the unit current for the sub-threshold leakage current, V_T is the threshold voltage, S is the sub-threshold swing.

The ΔENOB is given by following, if comparator noise can be neglected,

$$\Delta\text{ENOB} = \frac{1}{2} \log_2 \left(1 + 12 \left(\frac{V_{\text{off}}(\sigma)}{V_q} \right)^2 \right) \quad (4)$$

where V_q is the quantization voltage and $V_{\text{off}}(\sigma)$ is the sigma of offset voltage distribution.

Figure 1 shows the estimated E_c , FoM, and $2^{\Delta\text{ENOB}}$ vs. V_{DD} when the resolution is 5 bits, $V_{\text{off}}(\sigma)$ is 6 mV, $V_T=0.1$ V, and f_c is 600 MHz. We used $C_c=170$ fF, $I_c=156$ μ A, $S=44$ mV from the measured data.

The E_c is basically proportional to V_{DD}^2 however ΔENOB is inversely proportional to V_{DD} since the quantization voltage becomes lower with V_{DD} reduction. However $2^{\Delta\text{ENOB}}$ is not large enough to affect the FoM. Therefore, the FoM can be significantly reduced by reducing power supply voltage V_{DD} .

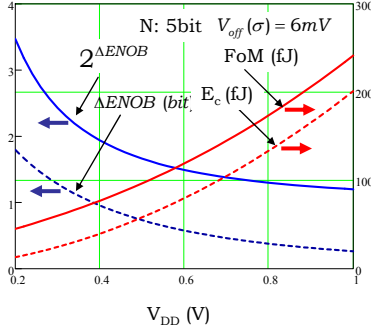


Fig. 1. Estimated E_c , FoM, and $2^{\Delta ENOB}$ vs. V_{DD} .

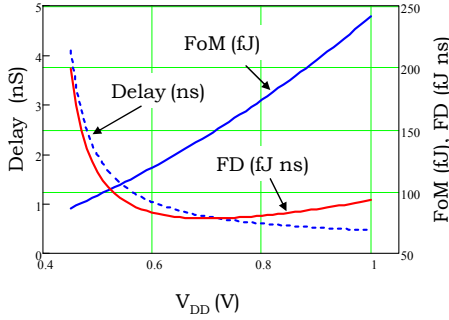


Fig. 2. FoM, Delay, and FD product vs. V_{DD} .

To increase the conversion frequency, an interleaving operation with multiple unit ADCs can be used and FoM can be kept almost the same, if the power consumption of additional circuits and the reduction of ENOB can be neglected.

However, excessive number of interleaving causes many issues such as an increase of occupied area, a reduction of PVT margins, a reduction of ENOB, furthermore an increase of input drive difficulty. Thus we should introduce FoM delay product (FD) like the energy-delay product (ED) in digital circuits [2][3]. The delay time should be defined as the reciprocal value of the maximum conversion frequency for a given operating voltage and we estimated it by using the following equation.

$$T_d = k \frac{V_{DD}}{(V_{DD} - V_T)^\alpha} \quad (5)$$

where k and α are the fitting constants, V_T is the effective threshold voltage. Figure 2 shows FoM shown in figure 1, with T_d derived from the equation (5), and FoM delay products. We used $V_T=0.4$ V (higher than the conventional definition of V_T) and $\alpha=1.2$. 0.7 V may offer the best V_{DD} to minimize the FD product.

This FD product suggests the balance between the number of interleaving and decrease of energy consumption. The lower value is preferable for low energy and high speed operation and the same value means the decrease of conversion speed by reducing the operating voltage can decrease the conversion energy equivalently.

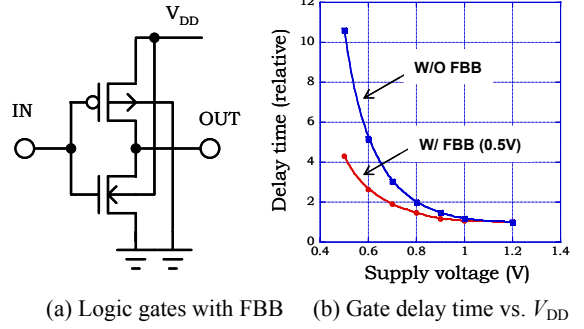


Fig. 3. Logic gates with forward body bias (FBB) and the gate delay time vs. supply voltage.

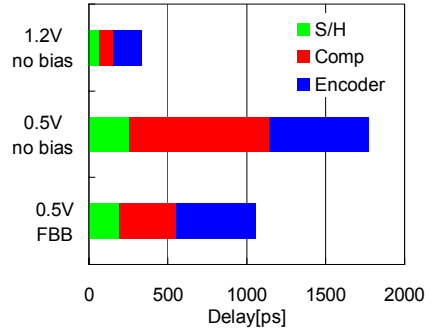


Fig. 4. Delay time of each circuit block for $V_{DD}=1.2$ V, and $V_{DD}=0.5$ V with and without FBB.

III. CIRCUIT DESIGN

A. Forward body bias technique

A gate delay time will increase significantly when the supply voltage is reduced to 0.5 V. Thus we introduced the forward body bias technique to address this issue. At the ultra low voltage operation which is lower than the built-in potential of the PN junction, the forward body bias (FBB) technique can be used easily to connect the body of NMOS to V_{DD} and the body of PMOS to the ground. This configuration makes circuit and layout simple, as shown in figure 3 (a). The reductions of V_T by FBB have been measured 100 mV for NMOS and 60 mV for PMOS. The gate delay time can be reduced to about half for the conventional CMOS circuit, as shown in figure 3 (b).

Figure 4 shows the delay time of each circuit block for $V_{DD}=1.2$ V and $V_{DD}=0.5$ V with and without FBB. The delay time is increased by about 6x without FBB, however it can be suppressed by about 3.5x with FBB. The comparator is the most sensitive to the voltage lowering.

B. Mismatch compensation by variable delay

We used a double-tail latched comparator [4] since this is suitable for low voltage operation compared with the conventional single-tail latched comparator owing to the reduced number of transistor stack. However, we had to

develop a new mismatch compensation technique using variable time delay method.

A variable capacitance method is widely used to compensate the offset voltage mismatch of dynamic comparator [5]. However, it loses its advantage with lowering the operating voltage, since the sensitivity of capacitance of the MOS varactor to the control voltage is reduced. Thus we developed mismatch compensation technique using variable delay circuit, as shown in figure 5.

This figure shows the dynamic preamplifier circuit in the double-tail latched comparator. The activation clock timing for the output nodes are controlled by variable delay circuits. Figure 6 shows the variable delay circuits for NMOS type and PMOS type.

Table 1 compares several mismatch compensation methods. Input offset mismatch voltage of the comparator is about 10 mV without any mismatch compensations. The capacitance method can't compensate the mismatch with sufficient accuracy. The current method can compensate sufficiently however power consumption is large.

This timing method using a NMOS transistor, shown in figure 6 (a), exhibits a smaller mismatch voltage; however, power consumption is very large. This is due to the large PMOS transistor for variable delay inverter inserted to the clock circuit. PMOS type, shown in figure 6 (b), provides the best balance between compensation accuracy, delay time, and power consumption. Thus we used this PMOS type circuit.

Figure 7 shows the layout of the comparator. The area for compensation is not too large in comparison with the core comparator circuit.

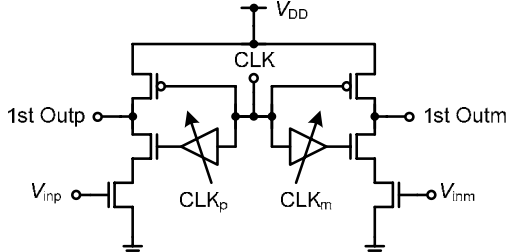


Fig. 5. Mismatch compensation by variable delay circuit.

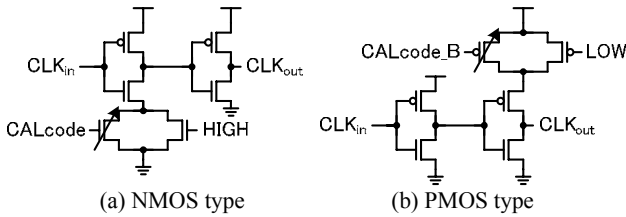


Fig. 6. Variable delay circuits for NMOS type and PMOS type.

Table 1. The comparison of several mismatch methods.

	no CAL	Cur CAL	Cap CAL	Time CAL_N	Time CAL_P
σ_{offset} [mV]	10.1	1.32	5.79	1.09	1.49
Power@500MHz [μ W]	14.5	41.3 (14.6)	21.4	49.4	24.5
Delay [ps]	365	450	756	682	511

C. Overall design of ADC

Figure 8 shows an overall block diagram of this ADC. Eight sample and hold circuits are located at the input part. Two-bit gate-interpolated comparators [6] are located between the sample and hold circuits. The sample and hold circuit is useful to increase available input frequency and to realize flexible interfacing to the signal whose common voltage is different from the common voltage of the ADC. It however increases input capacitance, input switching current, and power dissipation of the ADC since the driving power for the sample and hold circuit will increase. In contrast, the gate-interpolation method can reduce these power consumptions without a serious sacrifice in the ADC's performance. 6-bit up and down counters are used for the digital mismatch compensation.

Figure 9 shows a chip layout of this ADC. An occupied area is about 0.083 mm². The chip has been fabricated in 90 nm CMOS technology with deep N-well option.

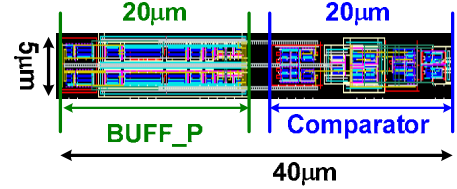


Fig. 7 The layout of comparator.

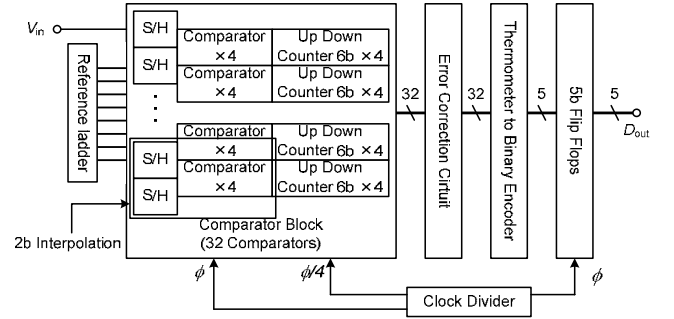


Fig. 8. Overall block diagram of the ADC.

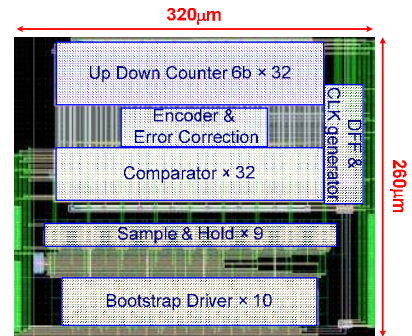


Fig. 9. Chip layout of the ADC.

IV. EXPERIMENTAL RESULTS

Figure 10 shows the measured DNL and INL at the conversion rate of 600 MS/s at V_{DD} of 0.5 V, with and without offset calibration. The DNL is less than ± 0.8 LSB and INL is less than ± 1.0 LSB.

Figure 11 (a) shows a spur free dynamic range (SFDR) and signal to noise and distortion ratio (SNDR) versus the conversion rate when the input signal frequency is about 50 MHz. The SNDR remains higher than 27 dB (4.2 ENOB) until 600 MS/s. Figure 11 (b) shows SFDR and SNDR versus the input frequency at the sampling rate of 600 MS/s. The effective resolution bandwidth (ERBW) is about 200 MHz.

An ultra-low voltage operation of 0.5 V has been attained with a small power consumption of 1.2 mW and a high conversion frequency of 600 MS/s. Also, a very low FoM of 160 fJ/conv.step has been obtained from ERB. The current for the reference ladder is about 300 μ A and the body bias leakage current is 10 μ A. Table 2 summarizes the performance of this ADC and compares it to the previous relevant works.

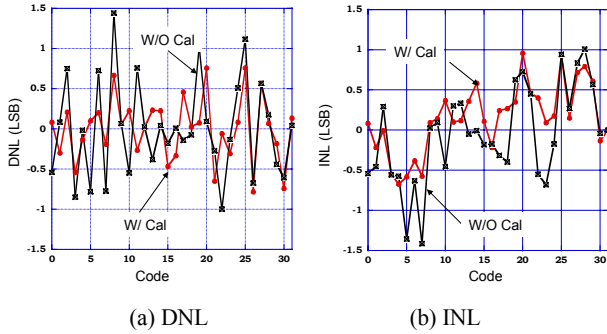


Fig. 10. DNL and INL at 600 MS/s and 0.5 V.

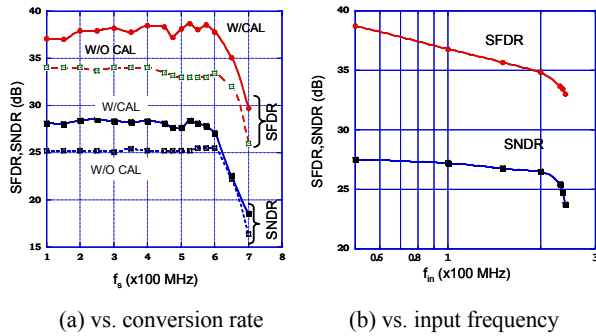


Fig. 11. SFDR and SNDR vs. conversion rate and input frequency.

Table. 2 Performance summary and comparison.

Reference #	[7]	[8]	[9]	[10]	This work
Resolution (bit)	5	5	5	5	5
fs (GS/s)	0.5	1.75	1.75	0.06	0.6
SNDR (dB)	26	30	30	26	27
Pd (mW)	5.9	2.2	7.6	1.3	1.2
Active area (mm ²)	0.87	0.017	0.03	-	0.083
Vdd (V)	1.2	1	1	0.6	0.5
FoM(fJ)	750	50	150	1060	160
CMOS Tech. (nm)	65	90	90	90	90
Architecture	SAR	Fold+Flash	Flash	Flash	Flash

V. CONCLUSION

We attempted to reduce the supply voltage of a high speed ADC down to 0.5 V for future voltage lowering and low energy operation. A 5-bit Flash ADC has achieved a high conversion rate of 600 MS/s at a low supply voltage of 0.5 V. It consumes only 1.2 mW and an ultra-low FoM of 160 fJ/conv. step was attained. A forward body bias method and a gate-interpolated double-tail latched comparator with a variable delay method to compensate for the mismatch voltage are introduced.

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