A 0.5V 4.85Mbps Dual-Mode Baseband Transceiver with Extended Frequency Calibration for Biotelemetry Applications

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***Abstract*—This work provides a dual-mode transceiver chipset for wireless body area network (WBAN). The modulation schemes include both MT-CDMA and OFDM. A phase-frequency tunable clock generator (PFTCG) is designed with frequency and phase tuning capability on the fly. A rotator-and-synthesizer driven (RSD) frequency pre-calibration with the aid of the PFTCG enables calibration for extended 100ppm frequency error (2.5x of state-of-the-art systems). This chip is manufactured in 90nm standard CMOS process. The supply voltage to the chip core is globally applied at 0.5V with 12 power- and voltage-domain partitions for sleep-active and voltage-scaling management. The PFTCG is operated at 5MHz with RMS jitter 145ps. The transceiver chipset provides maximum 4.85Mbps data rate with 73.7% power reduction in baseband circuit processing.**

***Index Terms*—PLL, power domain, voltage scaling , WBAN**

I. Introduction

UBIQUITOUS healthcare monitoring plays a crucial role in physical status tracking and recording. This extends medical services from the closed in-hospital systems to any open roaming spaces. Wireless body area network (WBAN), consisting of a multiple of wireless sensor nodes (WSNs) and a central processing node (CPN) [1], is specifically designed for body signal collection and monitoring to provide reliable physical information. The WSN is capable of sensing and processing body information, and transmits the data wirelessly to a CPN. The WBAN, especially the WSN, is required to provide reliable signal exchanges and ultra-low power (μW-level) with highly integrated tiny area.

WBAN-oriented applications may cover from non-invasive to implanted systems that further differ in data rate requirements. Moreover, the wireless channel conditions inside a body also perform different features from that on the skin surface. Existing possible systems [2-3] for the WBAN applications, however, provide single modulation scheme that have difficulty meeting the whole application spectrum with unacceptable power consumption. Furthermore, those candidate systems operate at the industry-science-medical (ISM) band may easily be fully occupied by unexpected interference. Accordingly, Federal Communications Committee (FCC) defines a set of wireless medical telemetry service (WMTS) band [4], and our previous proposal [1] was designed under the basis of the WMTS constraints.

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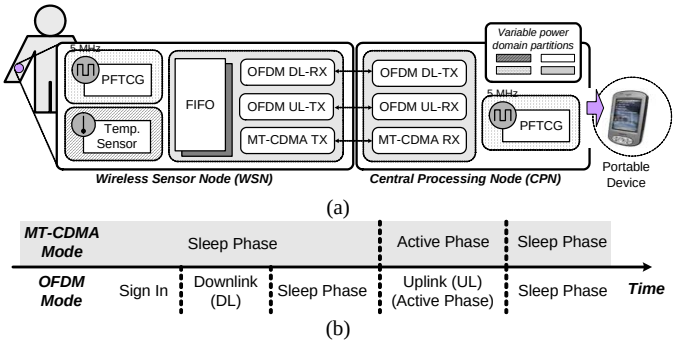

Fig. 1. The dual-mode baseband transceiver with (a) abstract view of functional blocks and (b) behavior time line.

It is necessary to provide a dedicated hardware solution for μW-WBAN applications. State-of-the-art platforms [5-6] achieve highly integrated SoC designs with mature FSK wireless scheme. An alternative RF front-end design [7] focuses on a pulse-based radio transmission. In the board-level approach, a planar thin-film technology [8] is used for comfortable wearing. Those published chips are implemented above 1V supply voltage with milli-order power consumption, and the frequency-error toleration is not extended for possible area shrinking and component integration.

A WBAN platform is proposed in this work to meet dual-mode high data rate with extended frequency-error calibration capability. The circuit is globally operated at sub-1V with μ-level power consumption.

This paper is organized as follows. In section II, a system operation is given, and section III presents a baseband transceiver design. Then the simulation and experimental results are presented in section IV followed by the conclusion in section V.

II. System Operations

The proposed wireless body on the chip (WiBoC) platform contains a WSN and a CPN that are attached on human body skin and integrated in a portable device, respectively. The system block diagram and behavior time-line are illustrated in Fig. 1. A register-based FIFO is designed in the WSN that is used to accumulate body signals from an internally integrated temperature sensor or an external readout sensor. The memory

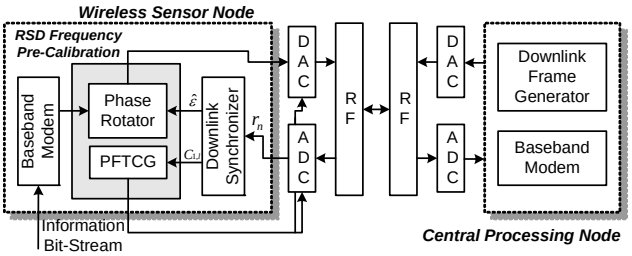

Fig. 2. The baseband transceiver with RSD frequency pre-calibration.

size and clocking speed are optimized for and aimed at the electrocardiogram (ECG) signal that are regarded as the most complex signals among body information sources. Compared to the baseband processing speed, the WSN takes much longer time accumulating body signals. This results in the WSN-CPN pair staying inactive for most of the time and awake in burst for data transmission. The baseband processor provides both MT-CDMA and OFDM modes for selection, and the transmission behavior is shown in Fig. 1(b) [9].

The OFDM symbols are pre-calibrated with the estimated carrier frequency offset (CFO) and sampling clock offset (SCO) via the rotator-and-synthesizer driven (RSD) frequency pre-calibration, where the frequency information is from the downlink synchronizer. The downlink synchronizer estimates CFO and SCO from the downlink frame. We propose the phase rotator which rotates the data by the estimated CFO value before the data are transmitted. A phase-frequency tunable clock generator (PFTCG) generates an accurate clock which is adjusted by the estimated SCO. The benefits of providing phase tuning capability are disclosed in [1] (for power reduction). This PFTCG is used to adjust the generated clock phase and frequency automatically for better system performance and reduced power consumption. Therefore, the baseband clock will be accurately tuned by the generator and the SCO effect will be reduced.

In the down-link process, the CFO between the WSN and CPN is estimated by the expression

$$z = \sum_{n=0}^{N-1} r_{n+N} \cdot (r_n)^* = \sum_{n=0}^{N-1} r_n e^{j2\pi\varepsilon} \cdot (r_n)^* = e^{j2\pi\varepsilon} \sum_{n=0}^{N-1} |\, r_n \,|^2 \qquad (1)$$

where r_n is a periodic transmitted down-link frame [9], N is the length of the preamble, and z is the inner product of consecutive two preambles. The ε is the added CFO value, and the estimated CFO is computed via

$$\hat{\varepsilon} = (1/2\pi)\tan^{-1}(z) \qquad (2)$$

The remaining received and ready-for-transmitted data will be compensated by this estimated value.

The SCO value is estimated by the pilot information in preambles [9]. The behavior of the clock offset can be modeled in frequency domain as

$$\theta_{l,k} = C_{l,0} + C_{l,1}k \qquad (3)$$

where k is the index of the subcarrier, and $\theta_{l,k}$ is the phase rotation of the data at k_{th} carrier in l_{th} preamble. The coefficient $C_{l,0}$ means the CFO value. The slope $C_{l,1}$ is used to estimate SCO.

The SCO effect on these pilots can be described as the following matrix form

$$KC_l = \theta_l \qquad (4)$$

where $K = \begin{bmatrix} 1 & k_1 \\ 1 & k_2 \\ : & : \\ : & : \\ 1 & k_m \end{bmatrix}$, $C_l = \begin{bmatrix} C_{l,0} \\ C_{l,1} \end{bmatrix}$, and $\theta_l = \begin{bmatrix} \theta_{l,k_1} \\ \theta_{l,k_2} \\ : \\ : \\ \theta_{l,k_m} \end{bmatrix}$

We can obtain the $C_{l,1}$ in the preamble phase rotation by least square algorithm.

$$C_l = (K^T K)^{-1} K^T \theta_l \qquad (5)$$

According to the estimated value in (5), the PFTCG is able to alter its generated frequency to reduce the sampling rate mismatch from the CPN side.

III. Baseband Transceiver Design

A. Baseband Modem

This chipset is designed with power-domain partitions for voltage scaling, multi-supply voltage, and power gating to achieve extreme low power consumption as illustrated in Fig. 3. With the voltage scaling and multi-supply voltage techniques, the system is partitioned into 12 power domains with possible different voltage supplies. According to the required operating speed and the achievable functionality, the supply voltage 0.5V is provided globally to every functional block, except special function blocks and transfer-domain (TD) that are operated at 1.0V to interface with I/O pads. Inactive domains can be switched into sleep phase for most leakage power saving. This active-sleep behavior is achieved by a power management cell (PMC) that contains a distributed coarse-grain power gating cell (DCG-PGC) [1]. The power manager sends commands to the PMC to turn ON/OFF the power-gated domain (PGD). If a hardware block always stays active, its power will not be gated and is referred as always-on domain (AOD).

In addition, the chipset has several clock domains to drive different sequential circuits. For the MT-CDMA block, a clock of 1/31 time of the original frequency is required. Besides, a low frequency to drive the sensor is necessary. Therefore, an embedded clock generator provides the 5MHz clock source, and a clock manager unit is designed for frequency synthesis. The synthesized frequency outputs 5MHz, 161kHz, and 610Hz clocks to cover all possible requirements.

B. Clock Generator

The phase-frequency tunable clock generator (PFTCG) is designed for performance improvement and power reduction in WSN and CPN, respectively, as shown in Fig. 4. There are 4 major blocks, including phase-frequency detector (PFD), controller, digitally-controlled oscillator (DCO) and phase

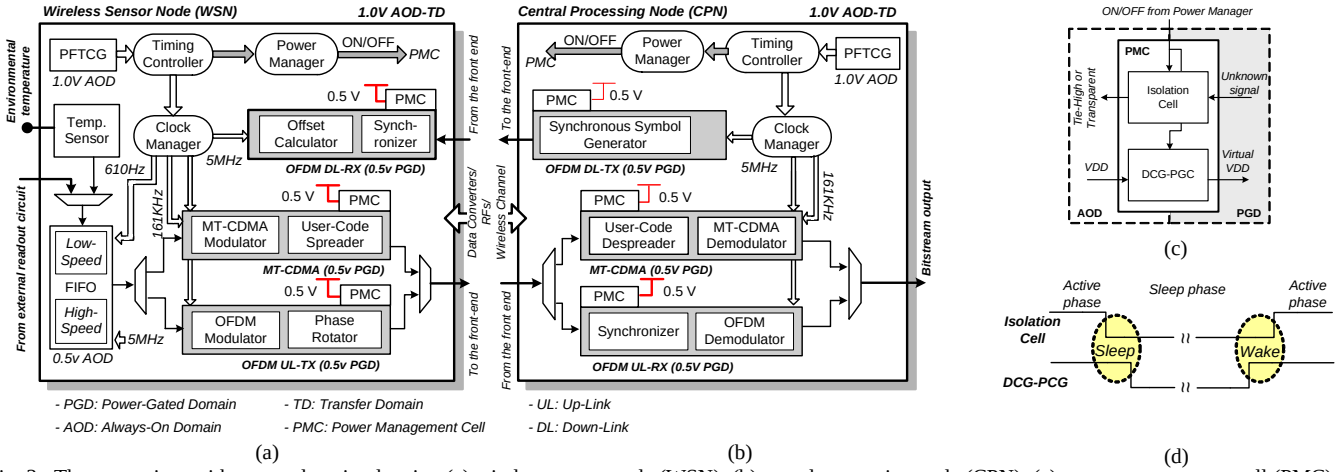

Fig. 3. The transceiver with power domain planning (a) wireless sensor node (WSN); (b)central processing node (CPN); (c) power management cell (PMC); (d) power management control sequence

selection multiplexer. The PFD and DCO are used for 5MHz clock generation. In the beginning of clock generation and locking loop, the PFD generates an UP or DOWN command to modify the delay in the tracking loop. When this loop achieves the lock state, the resulting clock frequency corresponds to the desired 5MHz clock, which is regarded as the coarse tuning loop.

The DCO further generates eight phases as the lock state is reached. It is designed with 8 delay buffers, and each buffer provides $T_{REFCLK}/8$ delay time, resulting in 8 clock signals with equal-spaced $T_{REFCLK}/8$ between *Cycle_N* and *Cycle_(N+1)*. Then one of these 8 sources is selected via the phase-selection. The correct frequency is generated by the closed loop of PFD, controller, and the phase_0 (PH0) in the DCO. This guarantees the resulted clocks keep the same delay spacing $T_{REFCLK}/8$ when the process-voltage-temperature (PVT) condition changes.

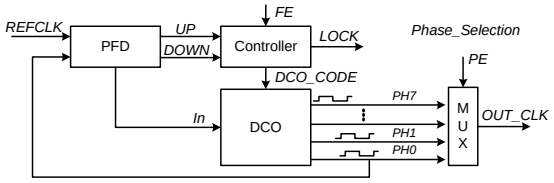

Fig 4. The proposed PFTCG architecture

The PFTCG allows the WSN and CPN to slightly change the generated clock frequency and phase by sending a command frequency-error (FE) and phase-error (PE) to the controller and multiplexer, respectively. This frequency fine-tuning capability is to reduce the sampling clock offset between the WSN and CPN for better performance, and the phase-selection capability enables the CPN to sample incoming signals at better instances without increasing sampling frequency.

IV. Simulation and Experimental Results

The proposed WiBoC baseband transceiver chipset is fabricated in 90nm 1P9M CMOS standard process, where both devices of high- and regular-threshold voltages (SPHVT and SPRVT) are applied in this design. The measurement instruments include a LeCroy LC584A and a current-meter with resolution of 100pA.

Figure 5 presents the overall system performance with extended frequency error 100ppm by simulation. A non-pre-calibrated performance curve has a saturated 100% frame error rate (FER). The RSD pre-calibration compensates the frequency error, and the performance is converged to SNR=5.5dB at FER=1% which is identical to the one with normal frequency error 20ppm.

The PFTCG is an always-on building block so that it is implemented in the high threshold-voltage device for static current saving. The generated clock frequency and phase number are 5MHz and 8 phases, respectively. Figure 6 shows four generated phases (PH0, PH2, PH4, PH6). This multi-phase clock generation provides better system performance and reduced power in data converter circuits as discussed in [1]. The measured RMS and peak-to-peak jitter is 145ps and 340ps, respectively. The power consumption is 145.8μW at 5MHz frequency and 1V supply voltage.

The building blocks in this chip are tended to be designed with individual groups of power pads. This enables the power consumption in some of the blocks measured separately. TABLE I shows the measured core power consumption in the corresponding power domain.

The power-domain is turned on by the DCG-PGC. The OFDM DL-TX building block is used for the illustration of the current profile between active and sleep states. This current profile is generated by concatenating a resistor (51k ohm) in the way of core power path for clear instrument observation, and the voltage between this resistor's two sides is shown in Fig. 7. As the ENABLE signal is activated, the OFDM DL-TX domain is turned on, and more current is drawn (current = (measured voltage)/51kohm) that corresponds to μ-level power consumption.

This WiBoC improves the system data rate from 143kbps to 4.85Mbps. This largely reduces the system working duty cycle (the percentage of circuit-active time). The transmission power is reduced from previous proposal 21μW [1] to this work 5.52μW, resulting in 73.7% efficiency improvement in baseband circuit processing. Figure 8 shows the micro chip photos. Each bold-rectangular denotes a separate power domain with the rest region as the transfer domain for I/O-pad interfaces. TABLE II summarizes the features of this work.

V. Conclusion

This work provides a dual-mode baseband transceiver chipset. A clock generator with frequency and phase tuning capability is provided for system performance improvement and power reduction. The supply voltage is scaled to 0.5V with dedicated power-domain partitions. The power efficiency is improved in baseband signal processing. The extended frequency calibration reflects the system robustness, enabling the use of inaccurate reference clocks for higher system integration purposes. As a result, a low power, highly-integrated, and robust WBAN system is achieved for biotelemetry applications.

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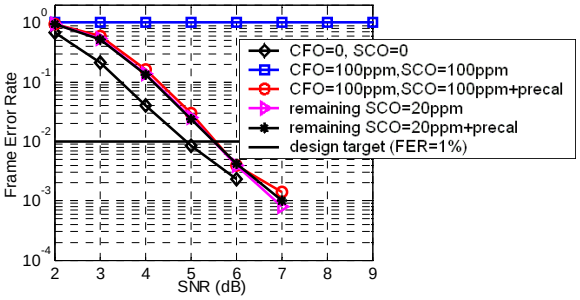

Fig. 5. System performance with RSD frequency pre-calibration.

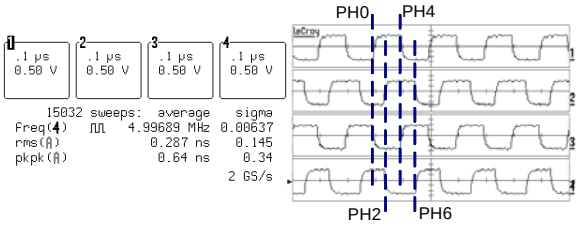

Fig. 6. Clock Phases from PFTCG

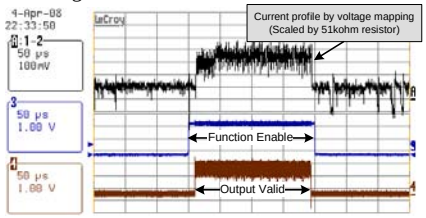

Fig. 7. Current profile between sleep and active

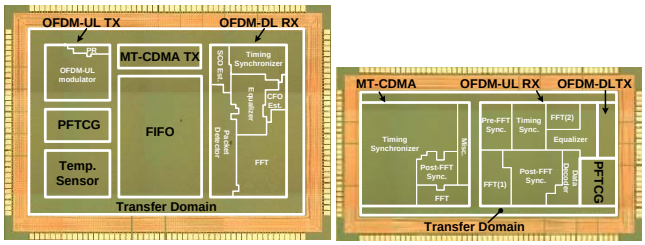

Fig. 8. Micro chip photo (a) WSN; (b) CPN

TABLE I
CHIP CORE POWER IN WSN AND CPN CHIPSET

WSN		CPN	
Total Modulator	5.52μW	DL-TX	3.94μW
		UL-RX	520μW
		MT-RX	490μW
FIFO+TS	289.5μW	N/A	N/A
PFTCG	145.8μW	PFTCG	145.8μW

TABLE II
CHIP SUMMARY

Technology	Standard 90nm SPHVT/SPRVT CMOS
Core Supply Voltage	Globally 0.5V
Max Data Rate	4.85Mbps (OFDM) 143kbps (MT-CDMA)
PFTCG	8 Phases Generations RMS Jitter 145ps
Die Size	WSN: 2191μm x 3030 μm CPN: 1980 μm x 2980 μm

References

[1] Jui-Yuan Yu, Ching-Che Chung, Wan-Chun Liao, and Chen-Yi Lee, "A sub-mW Multi-Tone CDMA Baseband Transceiver Chipset for Wireless Body Area Network Applications," *ISSCC Dig. Tech. Papers*, pp. 364-365, Feb. 2007.

[2] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Wireless Personal Area Networks (WPANs)*, IEEE Standard 802.15.1, 2005.

[3] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)*, IEEE Standard 802.15.4, 2003.

[4] Federal Communications Commission, "Amendment of Parts 2 and 95 of the Commission's Rules to Create a Wireless Medical Telemetry Service," FCC Washington, D.C., Rep. FCC00-211, 2000.

[5] Alan C-W. Wong, Declan Mc Donagh, Ganesh Kathiresan, Okundu C. Omeni, Omar El-Jamaly, Thomas C-K. Chan, Paul Paddan, Alison J. Burdett, "A 1V, Micropower System-on-Chip for Vital-Sign Monitoring in Wireless Body Sensor Networks," *ISSCC Dig. Tech. Papers*, pp. 138-139, Feb. 2008.

[6] A.C.W. Wong, G. Kathiresan, C.K.T. Chan, O. Eljamaly, and A.J. Burdett, "A 1V Wireless Transceiver for an Ultra Low Power SoC for Biotelemetry Applications," *ESSCIRC Dig. Tech. Papers*, pp. 127-130, Sep. 2007.

[7] D. Guermandi, S. Gambini, and J. Rabaey, "A 1V 250Kpps 90nm CMOS Pulse Based Transceiver for CM-Range Wireless Communication," *ESSCIRC Dig. Tech. Papers*, pp. 135-138, Sep. 2007.

[8] Hyejung Kim, Yongsang Kim, Young-Se Kwon, and Hoi-Jun Yoo, "A 1.12mW Continuous Healthcare Monitor Chip Integrated on a planar Fashionable Circuit Board," *ISSCC Dig. Tech. Papers*, pp. 150-151, Feb. 2008.

[9] Hsiao-Han Ma, Jui-Yuan Yu, Tsan-Wen Chen, Chien-Ying Yu, and Chen-Yi Lee, "An OFDMA Scheme Wireless Body Area Network with Frequency Pre-Calibration," in *Proc. 2008 IEEE VLSI-DAT*, pp. 192-195, Apr. 2008.