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# A 0.53-THz Subharmonic Injection-Locked Phased Array With 63- $\mu$ W Radiated Power in 40-nm CMOS — Source link

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# A 0.53 THz Subharmonic Injection-Locked Phased-Array with 63 $\mu$W Radiated Power in 40-nm CMOS

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***Abstract*—This paper presents a 0.53 THz subharmonic injection-locked 1×4 phased-array based on an injection-locked oscillator (ILO) chain. Thanks to the ILO chain, the phase errors in the phased-array can be compensated without introducing power variation. This technique enables accurate beam-steering with a 60° scan range in the E-plane at 0.53 THz. A six-stage triple-push oscillator is proposed to generate the signal at 0.53 THz. Compared to a conventional triple-push oscillator, it reduces layout constrains, improves signal balance, and enhances output power by at least 3 dB. The phased-array is implemented in 40-nm CMOS. With an injection power of 0 dBm, the injection-locked phased-array generates an output frequency from 529 to 534 GHz. At 531.5 GHz, the proposed phased-array achieves -12 dBm radiated power and 0.24‰ DC-to-THz efficiency without the use of silicon lens, quartz superstrate or substrate-thinning. The chip consumes 260 mW DC power and occupies an area of 2.5 mm$^2$.**

***Index Terms*—CMOS, terahertz, phased-array, injection lock, voltage-controlled oscillator(VCO).**

## I. Introduction

In terahertz (THz) applications such as imaging and high data-rate communication, phased-arrays can play important roles because of their beam-steering capability [1], [2]. These applications often require a phased-array transmitter with high radiated power and accurate beam-steering functionality at THz frequency. Conventionally, THz phased-arrays are usually implemented using III-V technologies and waveguide-based components [1], [2]. In recent years, there has been a growing interest in designing THz circuits using silicon-based technologies because they have the advantage of compact package, low-cost in high-volume production, and full integration with digital circuits [3]–[28].

Although there are many silicon-based phased-array designs in millimeter and submillimeter wave frequency band [29]–[36], the number of THz phased-array designs in silicon technologies is limited [3]–[5]. In [3] and [4], THz phased-arrays based on inter-coupled harmonic oscillators were proposed in a 130-nm SiGe technology and a 65-nm CMOS technology, respectively. In [5], a phased-array based on amplifier-multiplier chains was implemented at 0.4 THz using a 40-nm CMOS technology.

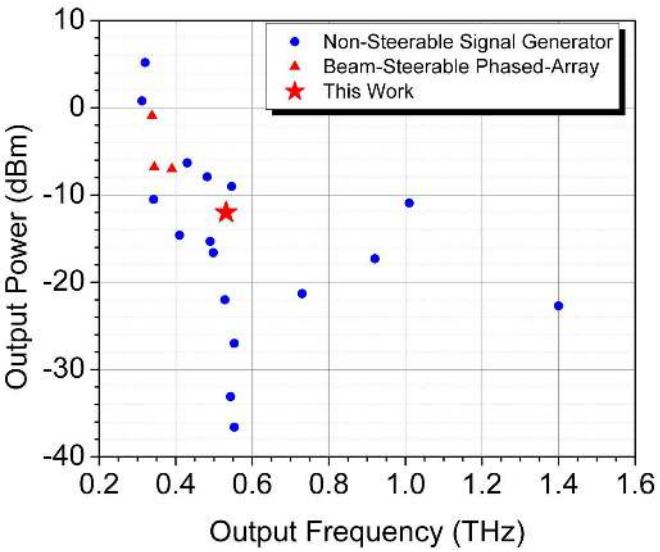


Fig. 1. The output frequency and output power of silicon-based THz signal generators [3]–[16], [19], [21], [22], [24]–[27].

So far, increasing the output frequency of a silicon-based phased-array beyond 0.5 THz has not been achieved, as it faces two major obstacles. One obstacle is that the design of multipliers or harmonic oscillators with such high output frequencies is particularly challenging. Several signal source designs based on harmonic oscillators beyond 0.5 THz have been proposed [13]–[24]. However, most of them suffer from limited output power or low power efficiency, especially when the signal sources are implemented using CMOS technologies. Multipliers have also been exploited to generate power above 0.5 THz. Nevertheless, they all need a relatively big input power ranging from 8 to 17 dBm [25]–[28]. The other obstacle in the design of silicon-based THz phased-arrays is that accurate phase control of the THz signal is difficult. Due to device modeling inaccuracy, dummy filling impact and process variation, the measured phase error of a high-frequency phase shifter is usually bigger than the simulated value. Furthermore, the variable-gain amplifier (VGA) used to compensate the gain variation of a phase shifter usually introduces phase error to the amplified signal [29], [30]. Consequently, the phase errors induced by the phase shifters and VGAs will degrade

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the beam-steering performance, and phase compensation techniques may be needed to correct the phase errors. For instance, in the phased-array designs presented in [31], [33], an extra phase bit was used as a trim to the phase errors. Compared to the millimeter wave phased-array which usually operates at its fundamental frequency, the phase error issue is exacerbated in a silicon-based THz phased-array, because the THz signals are commonly generated using multipliers or harmonic oscillators, and the phase errors induced at the fundamental frequency will get multiplied at the extracted harmonic frequency.

In this paper, a 0.53 THz 1×4 phased-array based on an ILO chain is presented. The chip is designed and fabricated in a 40-nm CMOS technology. The ILO chain can provide compensation for the severe phase errors in the THz phased-array without causing power variation. This technique enables accurate beam-steering with a 60° scan range in the E-plane. A six-stage triple-push oscillator is proposed to generate the 0.53 THz signal. Compared to a traditional three-stage triple-push oscillator, the proposed triple-push oscillator reduces layout constrains, improves signal balance, and enhances output power by at least 3 dB. Combining the radiation from four six-stage triple-push oscillators, -12 dBm radiated power and 0.24‰ DC-to-THz efficiency are achieved at 531.5 GHz without the use of silicon lens, quartz superstrate or substrate-thinning. The power consumption of the phased-array is 260 mW. The size of the chip is 2.5 $mm^2$. As seen in Fig. 1, this work is the first silicon-based phased-array above 0.5 THz.

## II. Phased-Array Architecture Based on Injection-Locked Oscillator Chain

To generate a beam-steerable THz signal using silicon-based technologies, frequency multiplying blocks are typically needed after phase shifting blocks to multiply the output frequency to THz range. As discussed in the previous section, the phase error in the phase shifting block will be multiplied together with the frequency, and the beam-steering performance of the THz phased-array will be degraded due to the severe phase error. Hence, the critical point in the design of a silicon-based THz phase-array is designing a frequency multiplying architecture that can compensate the phase error and at the same time does not cause variation of the THz output power.

Fig. 2(a) and (b) show two frequency multiplying architectures that can be used for generating THz signals. In both of them, two frequency multiplying blocks are cascaded to generate a output frequency that is M×N higher than the input frequency. With this M×N multiplying factor, a THz output frequency can be produced, and in the mean time the frequency of the power distribution network and the phase shifters before the frequency multiplying blocks can be kept in a low enough frequency band to achieve good performance.

The architecture in Fig. 2(a) is a multiplier chain in which two multipliers are cascaded. This architecture is commonly used for mm-wave and THz signal generation in silicon technologies [25], [28], [37]. Recently, it has also been reported to be used in a THz silicon-based phased-array design [5]. In this architecture, the phase errors caused by the phase shifters and the VGAs in a phased-array cannot be compensated, and will be multiplied by M×N at the output port of the multiplier chain. As a result, the beam-steering performance of the phased-array will deteriorate due to the phase errors.

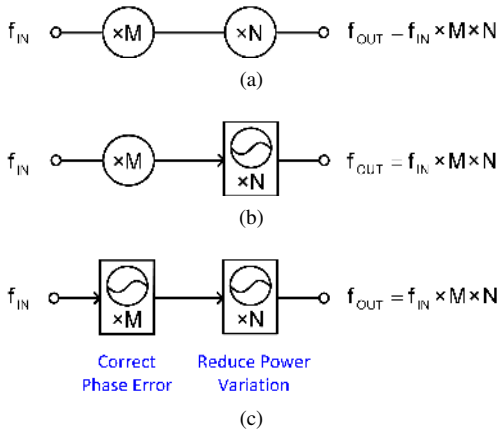



Fig. 2. Three frequency multiplying architectures with M×N multiplying factor. (a) A multiplier chain, and (b) a subharmonic injection-locked oscillator, and (c) a subharmonic injection-locked architecture based on the injection-locked oscillator chain.

The architecture in Fig. 2(b) is a subharmonic injection-locked oscillator that is usually used for mm-wave signal generation [38]–[40]. Different with the multiplier chain, the second stage in this architecture is an ILO. In this architecture, a phase tuning function can be incorporated in the ILO. When a signal is injected into the ILO, the phase shift between the locked oscillation signal and the injection signal can be continuously changed by adjusting the free-oscillation frequency of the ILO [41], [42]. The phase tuning ability in this architecture has been used to perform LO-based phase-shifting in RF and mm-wave phased-array designs [43], [44]. However, using this phase tuning method faces the problem of power variation. When the phase tuning is performed, the change of the free-oscillation frequency of the ILO causes the variation of the ILO output power [45]. Besides, when the control voltage of the varactors in the ILO is tuned to adjust its free-oscillation frequency, the equivalent parallel conductance of the varactor is changed, which will also induce the variation of the ILO output power. The power variation during the ILO-based phase tuning will cause the degradation of the beam-steering performance of the phased-array.

In this work, a subharmonic injection-locked phased-array architecture based on an ILO chain is proposed. The ILO chain is shown in Fig. 2(c), where two injection-locked harmonic oscillators are cascaded. This architecture also provides a M×N multiplying factor. At the same time, it can provide compensation for the phase errors in a THz phased-array without introducing output power variation. In this ILO chain, the phase error is compensated in the first ILO by adjusting its free-oscillation frequency. Although this phase compensation will cause power variation at the output of the first ILO, this power variation cannot lead to obvious power variation at the output port of the second ILO. This is due to the fact that the aforementioned reasons causing the power variation in an ILO do not exist in the second ILO, and the impact of the

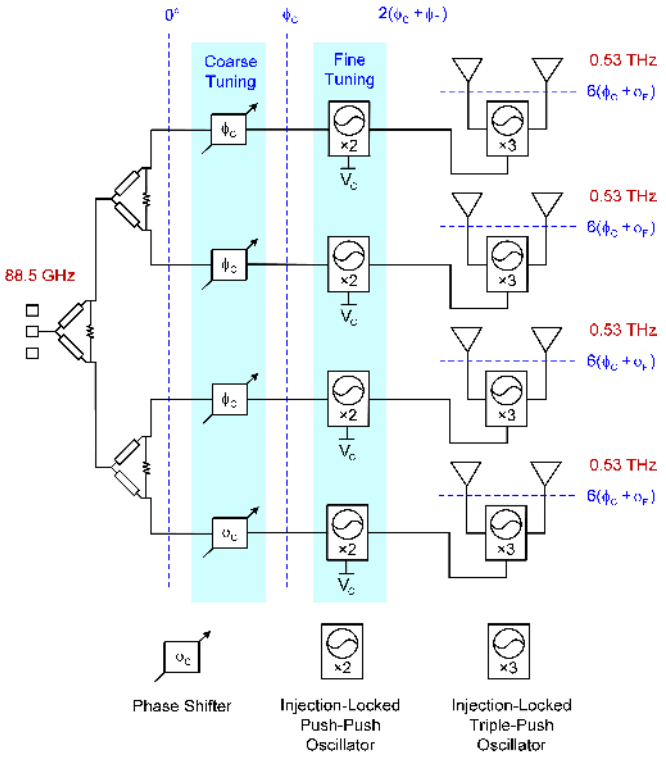



Fig. 3. The block diagram of the 0.53 THz phased-array.

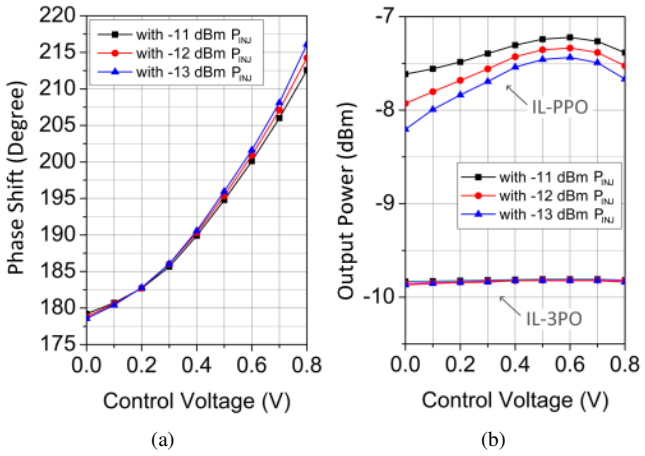



Fig. 4. (a) The simulated fine phase tuning $\phi_F$ under different control voltages of the IL-PPO, and (b) the simulated output power of the IL-PPO and the IL-3PO under different control voltages of the IL-PPO.

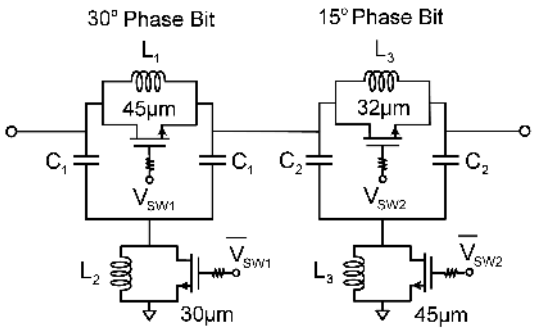
power variation at the output of the first ILO is suppressed by the second ILO, whose ouput power is primarily determined by the oscillator itself. Consequently, the output power of the ILO chain can be stable during the phase error correction.

To prove this concept, a 0.53 THz subharmonic injection-locked 1×4 phased-array based-on an ILO chain is implemented in a 40-nm CMOS technology. The block diagram of the proposed phased-array is shown in Fig. 3. In this phased-array, a subharmonic injection signal at 88.5 GHz is distributed to four channels using cascading Wilkinson dividers, and fed to individual phase shifters that can provide 2-bit coarse phase shift $\phi_C$. The output of the phase shifter is fed into an ILO chain in which an injection-locked push-push oscillator (IL-PPO) and an injection-locked triple-push oscillator (IL-3PO) are cascaded. The IL-3PO has two outputs at 0.53 THz, which are connected to two in-phase antennas radiating from the top side of the chip.

A fine phase tuning $\phi_F$ is introduced in the IL-PPO. As shown in Fig. 3, after cascading the IL-PPO and the IL-3PO, the phase shift is multiplied by 6, so the phase shift of the radiated signal at 0.53 THz is $6(\phi_C+\phi_F)$. With the continuous fine phase tuning $\phi_F$, possible phase error in the coarse phase tuning $\phi_C$ can be compensated. Fig. 4(a) shows the simulated phase change $\phi_F$ under different control voltages of the IL-PPO when an input power ranging from -13 dBm to -11 dBm is injected at 88.5 GHz. Fig. 4(b) shows the corresponding power variation at the outputs of the IL-PPO and the IL-3PO. In these simulations, the injection power is swept in order to include the impact of the input power fluctuation, which can be caused by the loss error of the 2-bit phase shifter. It can be seen that the phase control in the IL-PPO can cause power variation at the output of the IL-PPO. Nevertheless, the power variation is almost eliminated after the IL-3PO, which indicates that the phase error compensation is done without causing the variation of the output power of the ILO chain. In the measurements of the fabricated phase-array chip, the variation of the radiated power in each channel of the phased-array is less than $\pm$0.2 dB over all the coarse phase states and fine phase control. Thanks to this ILO-chain-based phased-array architecture, accurate beam-steering with a 60° scan range is realized at 0.53 THz, as shown in the measurement section of this paper.

In the proposed subharmonic injection-locked phased-array, the frequency of the power distribution network and the phase shifters is reduced to around 88.5 GHz, which is one sixth of the radiation frequency of 0.53 THz. This low input frequency can reduce the loss in the power distribution network and the phase shifters. Simulation shows that the loss caused by the input pad, the Wilkinson divider, and the phase shifter is around 4 dB. Thanks to the low loss, amplifier chains which are commonly used to amplify the distributed signal in each individual channel are not needed in this design. Thus, low DC power consumption and small chip size is achieved. Single-ended microstrip lines are used to implement the power distribution network, ensuring low signal mismatch and low coupling between different channels. The simulated isolation between different output ports of the power distribution network is better than 30 dB at 88.5 GHz. The simulated amplitude and phase mismatch at 88.5 GHz are less than 0.05 dB and 0.3°, respectively.

The phase noise of the proposed phased-array at the output frequency of 0.53 THz is related to an injection signal at about 88.5 GHz, where it is easier to achieve a good phase noise for a free-running CMOS oscillator as demonstrated in [46]. Considering an oscillator can provide a phase noise of -92 dBc/Hz at 1 MHz offset at 89 GHz in a 40-nm CMOS technology [46], a phase noise of -76 dBc/Hz at 1 MHz offset can be achieved at the output frequency of 0.53 THz using the proposed architecture, because the phase noise will increase by $20 \cdot \log_{10} 6$ when the frequency is multiplied by 6. This




| $L_1$ (pH) | $C_1$ (fF) | $L_2$ (pH) | $L_3$ (pH) | $C_2$ (fF) | $L_4$ (pH) |
|---|---|---|---|---|---|
| 95.1 | 14.3 | 32.8 | 82.4 | 10.9 | 24.5 |

Fig. 5. The schematic of the phase shifter.

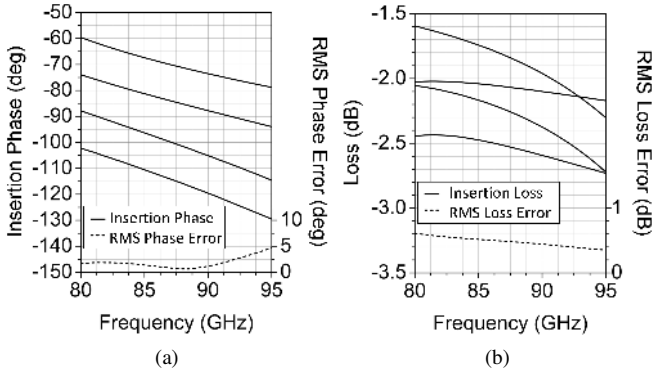



Fig. 6. The simulated insertion phase and loss of the 88.5 GHz 2-bit phase shifter.

result is comparable with the phase noise of the state-of-the-art CMOS phase-locked loop design with similar output frequency [16]. The focus of this work is on THz phased-array implementation, so an external injection signal is used in this design. In the future, an on-chip oscillator could be implemented as a central frequency reference.

## III. Building Blocks of the THz Phased-Array

### A. Phase Shifter

The schematic of the 88.5 GHz 2-bit phase shifter is shown in Fig. 5. The phase shifter is based on switched low-pass networks and is a concatenation of a 30° phase bit and a 15° phase bit. It can provide a phase shift of 0°, -15°, -30° or -45° at 88.5 GHz, which translates to 0°, -90°, -180° or -270° at the radiation frequency of 0.53 THz. As shown in Fig. 5, the 30° phase bit and 15° phase bit have the same topology. In the bypass-state, the upper transistor is on, and the lower transistor is off. The parallel inductor resonates with the off-state capacitance of the lower transistor. In the phase-delay state, the upper transistor is off, and the lower transistor is on. Then, a low-pass network with desired phase delay is created [31]. Triple well body-floating transistors are used in this design to reduce the loss of the phase shifter [47]. The simulated phase shift and insertion loss of the 2-bit phase shifter is shown in Fig. 6. The root mean square (RMS) phase error and loss error at 88.5 GHz are 1.2° and 0.4 dB, respectively. The simulated $S_{11}$ and $S_{22}$ are lower than -10 dB at 88.5 GHz for all the phase states.

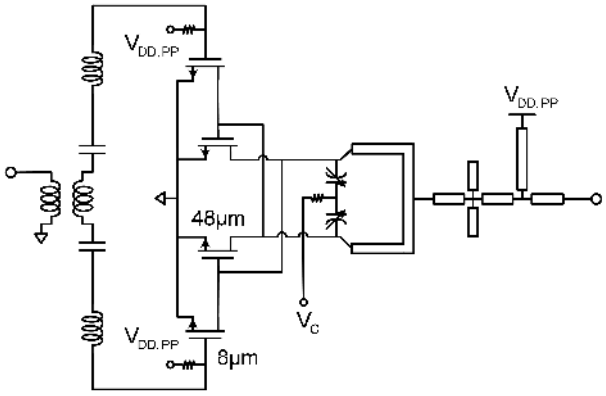



Fig. 7. The schematic of injection-locked push-push oscillator.

### B. Injection-Locked Push-Push Oscillator

The schematic of the IL-PPO is shown in Fig. 7. The push-push oscillator is based on a cross-couple oscillator with its second harmonic extracted around 177 GHz. At the input side, a transformer balun is used to perform single-ended to differential conversion for the injected signal. The 1:1 transformer has parallel primary and secondary windings to reduce the parasitic capacitance between the two windings, thus improving the signal balance of the balun. After the balun, DC blocking capacitors are used to avoid DC current from going through the center tap of the transformer balun, and series inductors are used to perform impedance transformation for maximum power transfer. The simulated loss of the balun along with the series capacitors and inductors is 2.5 dB at 88.5 GHz. The simulated amplitude and phase imbalance at 88.5 GHz are 0.1 dB and 0.3°, respectively. After the matching inductors, the differential injection signal is delivered to the cross-couple oscillator tank through the injection transistors, which are biased using 9 kΩ resistors at the gate nodes. The 36.8 pH inductor in the oscillator tank is implemented using microstrip lines and the simulated Q factor is 14.4. At the output side, a microstrip-based matching network is designed for maximum power transfer and has a simulated loss of 1.85 dB at 177 GHz. The supply voltage of the cross-couple oscillator and the injection transistors are added through the RF-shorted parallel stub in the output matching network. The transistors used in the cross-coupled pair are 46×1 $\mu$m, and the injection transistors are 8×1 $\mu$m. Accumulation-mode varactors are used in the oscillator tank to control the free-oscillation frequency of the oscillator. With a -11 dBm injection power, the simulated output power after the output matching network is -7.4 dBm at 177 GHz under a 0.81 V supply voltage. The simulated power consumption of one IL-PPO is 33.6 mW under a 0.81 V supply voltage.

Fig. 8 shows the simulated phase tuning performance of the IL-PPO under different injection powers at 88.5 GHz. It is found that the phase change in the whole locking range

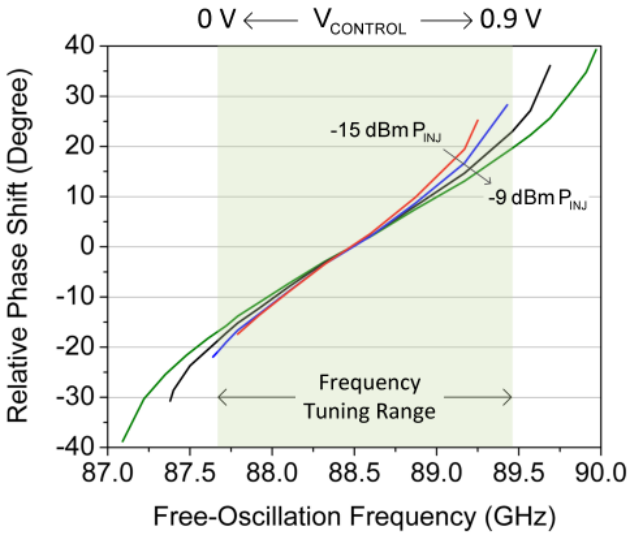



Fig. 8. The simulated phase tuning performance of the injection-locked push-push oscillator under different injection powers at 88.5 GHz.

increases when larger locking range is obtained by increasing the injection power. However, the achievable phase change will be limited by the frequency tuning range of the oscillator if the frequency tuning range is smaller than the locking range. Since the phase is less sensitive to the change of the free-oscillation frequency as the locking range increases, the achievable phase change will reduce when the locking range exceeds the frequency tuning range. As a result, for certain frequency tuning range, an injection signal with a proper power level is needed to maximize the achievable phase change.

### C. Injection-Locked Six-Stage Triple-Push Oscillator

A triple-push oscillator has been proved to be a good candidate for mm-wave and THz signal generation because of its third harmonic extraction ability and high loop gain at the frequency close to the $f_{max}$ of a transistor [9]. However, the three stages in a traditional triple-push oscillator are distributed in layout along a triangle, thus making the routing of the three parallel stubs very difficult. Two layout methods for triple-push oscillators have been reported so far. One method is connecting the three parallel stubs at the outside of the triangle, as shown in Fig. 9(a). This will obviously result in a non-ideal layout, and cause signal imbalance between the three stages since one parallel stub has to go around the triangle to reach the connecting point of the three parallel stubs. The other reported method is connecting the three parallel stubs in the middle of the triangle, as shown in Fig. 9(b). This can make the electrical length of the three parallel stubs more similar to each other. However, the output signal path has to go across one inter-stage transmission line if it needs to be connected to an on-chip antenna, which has to be put at the outside of the triangle because of its big size. As a result, the coupling between the output signal path and the inter-stage transmission line will cause signal unbalance in a THz design. For an integrated phased-array design above

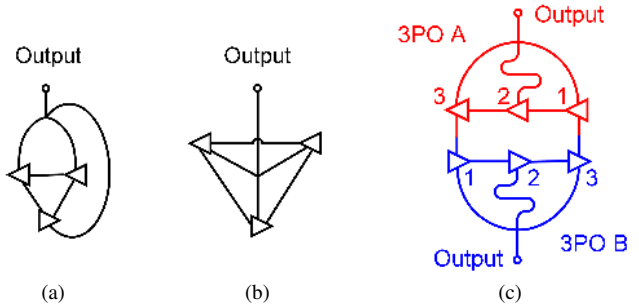



Fig. 9. (a) The traditional triple-push oscillator which connects the three parallel stubs at the outside of the triangle, and (b) the traditional triple-push oscillator which connects the three parallel stubs in the middle of the triangle, and (c) and the proposed six-stage triple-push oscillator.

0.5 THz, on-chip antennas are needed. Therefore, the second layout method is not suitable. In this work, a novel triple-push oscillator with six stages is proposed to address the layout problem in the traditional triple-push oscillators. As shown in Fig. 9(c), the six-stage triple-push oscillator is actually composed of two three-stage triple-push oscillators A and B. In the proposed six-stage triple-push oscillator, the output of the third stage in triple-push oscillator A is connected to the input of the first stage in triple-push oscillator B, and the third stage in triple-push oscillator B is connected to the first stage in triple-push oscillator A. Then, a loop containing six stages is composed. The ideal phase difference between two adjacent stages at the oscillation frequency is still 120°, which is the same with that in a traditional triple-push oscillator. At the third harmonic frequency, the signals from the six stages are in-phase. As shown in Fig. 9(c), the six stages are aligned in two lines. The adjacent three parallel stubs on one side of the two lines can be easily connected together. By using a zigzag routing for the parallel stubs in the middle, all the parallel stubs can have the same electrical length. Using the proposed six-stage triple-push oscilator, the signal imbalance caused by the layout constrains in a traditional triple-push oscillator is reduced. Besides, the proposed six-stage triple-push oscillator inherently doubles the output power compared to a three-stage triple-push oscillator because the number of stages increases from 3 to 6.

The schematic of the IL-3PO used in the proposed phased-array is shown in Fig. 10. The triple-push oscillator is locked to the output signal of the IL-PPO at around 177 GHz, and radiates the third harmonic power through two antennas at 0.53 THz. They are delivered to two on-chip patch antennas which are located with a pitch of 0.58 $\lambda_0$ at the radiation frequency. Hence, the radiated signals from the two patch antennas can combine constructively at 0.53 THz. Besides going to the extraction point, the third-order harmonic power from each of the six stages can also go to the next cascading stage. The transmission line between two adjacent stages can help to reduce this power [48]. The simulated power going towards the extraction point is 3.8 dB higher than the power going towards the next stage. The injection is performed at the gate of stage 1 through an injection transistor. From stage 2 to stage 6, 2.5 fF compensating capacitors are added to the gates of the stages in

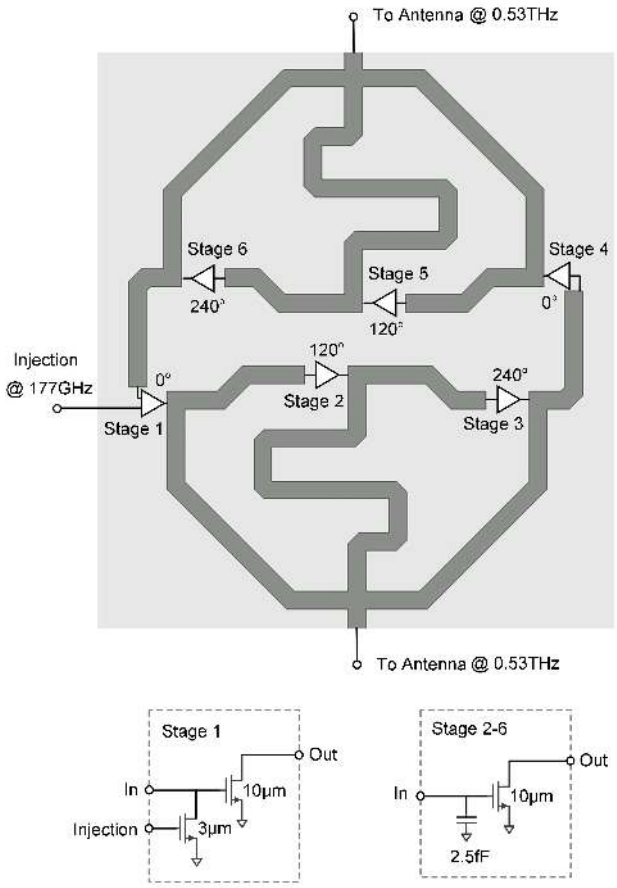



Fig. 10. The schematic and layout of the injection-locked six-stage triple-push oscillator.

order to reduce the signal imbalance caused by the capacitance contribution of the injection transistor. With an injection power of -7.4 dBm and a supply voltage of 0.9 V, the simulated RMS phase error and RMS amplitude error in the six stages at 177 GHz is less than 2° and 0.3 dB, respectively. The transistors in the six stages are $10\times1$ $\mu$m and the injection transistor is $3\times1$ $\mu$m. All the microstrip lines in the IL-3PO have a 61 Ω characteristic impedance, and are implemented using metal 9 and metal 11. It has been reported that the microstrip line loss in a silicon technology is 5.5 dB/mm at 0.5 THz [49]. This high loss may be ascribed to the ground surface roughness caused by the numerous holes on the ground plane in the thin metal layer of an advanced silicon technology [50], [51]. By using metal 9 as the ground plane, the holes can be kept far enough from the return current on the ground plane, because the maximum allowed distance between the holes in metal 9 is much bigger than that in the lower thin metal layers. Thus, the loss caused by ground surface roughness can be avoided. With an injection power of -7.4 dBm and a supply voltage of 0.9 V, the simulated locking range is from 175.1 GHz to 177.4 GHz, and the simulated output power generated by the IL-3PO is -9.8 dBm at 531 GHz. The simulated DC power consumption of one IL-3PO is 33.6 mW under a 0.9 V supply voltage.

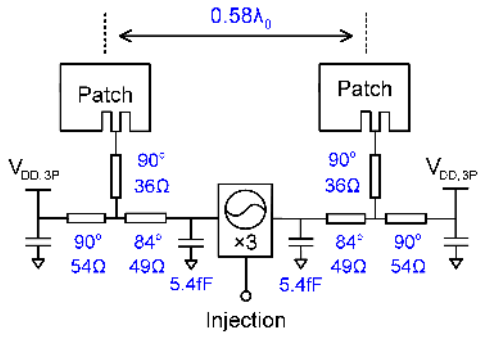


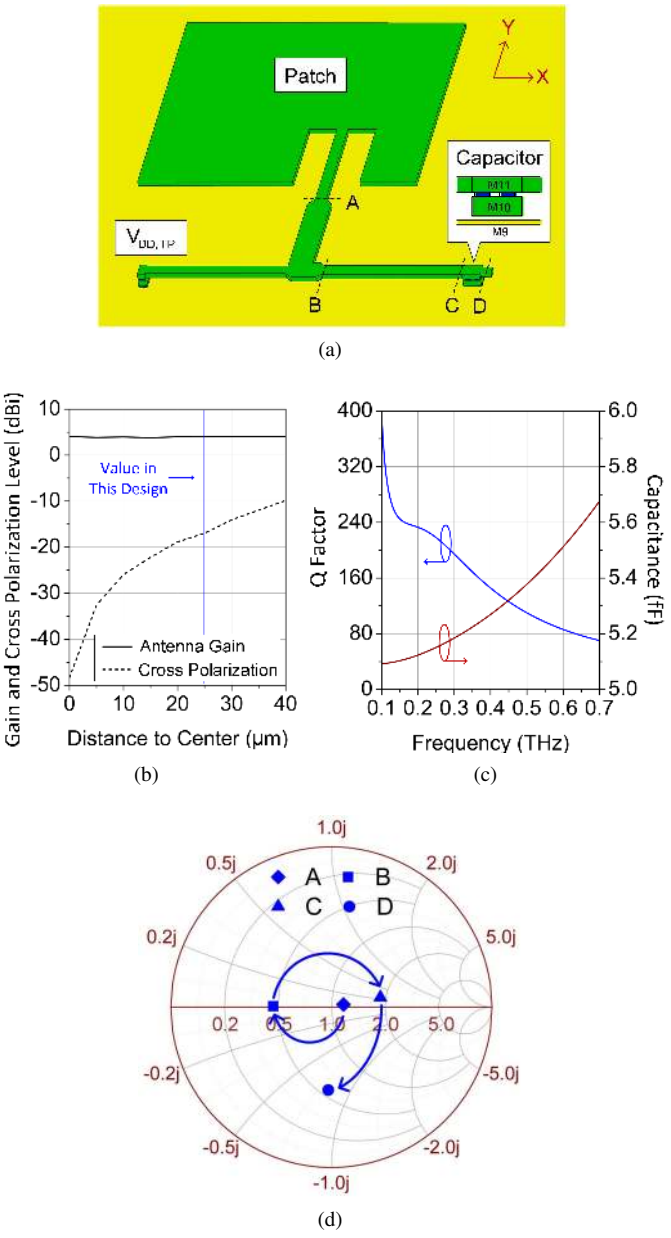

Fig. 11. The schematic of the patch antenna and its input matching network.

### D. Antenna Array

In the proposed phased-array, patch antennas with on-chip ground plane are used for radiating THz signals into the free space. In an on-chip patch antenna, the surface waves caused by the thick silicon substrate are eliminated, because the ground plane of the on-chip patch antenna is above the silicon substrate. Above the ground plane, the very thin dielectric layer can only allow the lowest order $TM_0$ surface wave mode to exist [52]. Based on the method proposed in [53], the scan blindness angle of the antenna array on such a thin grounded dielectric layer is $\pm87.4°$ when the antenna element spacing is 0.5 $\lambda_0$. This indicates that the antenna array can scan to $\pm87.4°$ before triggering a dominant $TM_0$ mode. In the antennas that are impacted by the thick silicon substrate, the radiation pattern is highly influenced by the location of the antenna on the chip, the dimension of the chip, and the distribution of the bond wires. Comparatively, the radiation pattern of a patch antenna is less influenced by those factors, because the thick silicon substrate is shielded. Thus, by using a patch antenna array, the radiation pattern from each channel of a phased-array can be similar. Furthermore, low inter-element coupling can be achieved in a patch antenna array as the coupling through the thick silicon substrate is avoided.

As shown in Fig. 11, the signals extracted from the two output ports of one IL-3PO are fed to two individual patch antennas with a pitch of 0.58 $\lambda_0$. The pitch is larger than 0.5 $\lambda_0$ to leave enough layout space for the IL-3PO between the two antennas in order to reduce the coupling between the IL-3PO and the antennas. Between the input port of the patch antenna and the output port of the six-stage triple-push oscillator, microstrip lines and a capacitor are used to compose an impedance matching network to provide the optimum load impedance for the IL-3PO. Besides, the power supply of the triple-push oscillator is added through a RF-shorted quarter-wavelength microstrip line connected in parallel with this matching network.

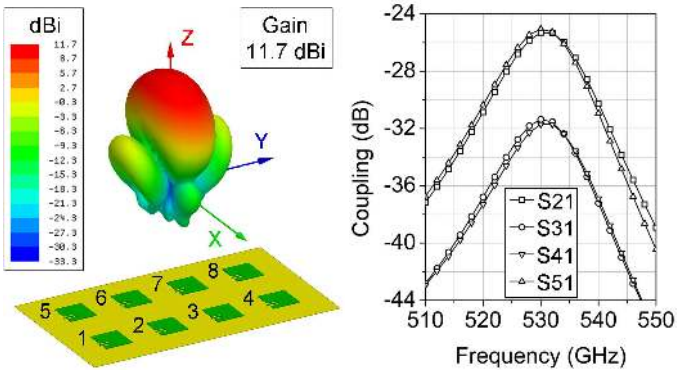
The layout of one patch antenna and its input matching network is shown in Fig. 12(a). The input port of the antenna moves inwards the center of the patch along the Y axis to obtain a lower input resistance. Besides, the input port is not in the center of the patch antenna along the X axis. This is to move the patch antenna away from the other circuit blocks as shown in Fig. 14. Fig. 12(b) shows the simulated antenna




(a) (b) (c) (d)

Fig. 12. (a) The 3D view of one patch antenna and its input matching network. (b) The simulated antenna gain and cross polarization level when the input port of the patch antenna in Fig. 12(a) is moved along the X axis. (c) The simulated capacitance and Q factor of the parallel plate capacitor shown in Fig. 12(a). (d) Impedance transformation of the input matching network.

gain and cross polarization level at the broadside of the patch antenna for different distances between the input port and the center of the patch in the X axis. Although the antenna gain remains nearly constant when the input port moves along the X axis, the cross polarization level increases when the input is not in the center. In this design, a distance of 25 $\mu$m is chosen. At this distance, the cross polarization level is still 20 dB lower than the co-polarization. The patch antenna designed in this work is implemented using metal 11 as the patch layer and metal 9 as the ground layer. The simulated gain and efficiency of a patch antenna are 4 dB and 44%, respectively. The microstrip lines in the matching network are implemented using metal 11 as the signal line and metal 9 as the ground




(a) (b)

Fig. 13. (a) The simulated radiation pattern of the antenna array. (b) The simulated coupling between different antenna elements in the antenna array.

plane. The capacitor in the matching network is only 5.4 fF due to the very high output frequency. This small capacitance is achieved using a parallel plate capacitor implemented using metal 10 and metal 9, as shown in Fig. 12(a). The simulated capacitance and Q factor of the parallel plate capacitor are shown in Fig. 12(c). Fig. 12(d) shows the impedance matching of the matching network on the Smith chart. The simulated loss of the matching network is 0.53 dB at 0.53 THz.

The antenna array in the proposed phase-array consists of 8 patch antennas as shown in Fig. 13(a). The pitch of adjacent channels is 0.52 $\lambda_0$ at 0.53 THz. The pitch is larger than 0.5 $\lambda_0$ in order to leave more layout space for the circuits between adjacent antennas. Using the method in [53], the scan blindness angle of the proposed antenna array with a 0.52 $\lambda_0$ pitch is calculated as $\pm 67.2°$, which is much bigger than the aimed beam-steering range of this design. The antenna array is simulated by drawing the silicon substrate, the on-chip ground plane, dielectric layer, the patches, and the bond wires in an air box in HFSS. Fig. 13(a) shows the simulated radiation pattern of the antenna array. The simulated gain of the antenna array is 11.7 dBi. The 3-dB beam width is 25° in the E-plane and 46° in the H-plane. The side-lobes are 14 dB lower than the main beam. In this antenna array, the two antennas along the X axis are connected to the same IL-3PO, so they are radiating with the same phase. The phase difference between different antennas along the Y axis can be controled by the phase controling blocks in the four channels of the phased-array. In a phased-array transmitter, the coupling between different elements of the antenna array is important [32]. Fig. 13(b) shows the simulated coupling between different antenna elements in the proposed patch antenna array. The coupling is lower than -25 dB in the frequency of interest thanks to ground plane proximity.

## IV. Measurements

This chip is implemented in a 40-nm bulk CMOS process. The micrograph of the chip is shown in Fig. 14. The chip size is 1.46×1.71 mm$^2$ including pads. The picture of the wire-bonded chip on the PCB is shown in Fig. 15. The chip is mounted in a cavity in the middle of the PCB to reduce the length of the bond wires. The distance between the patch

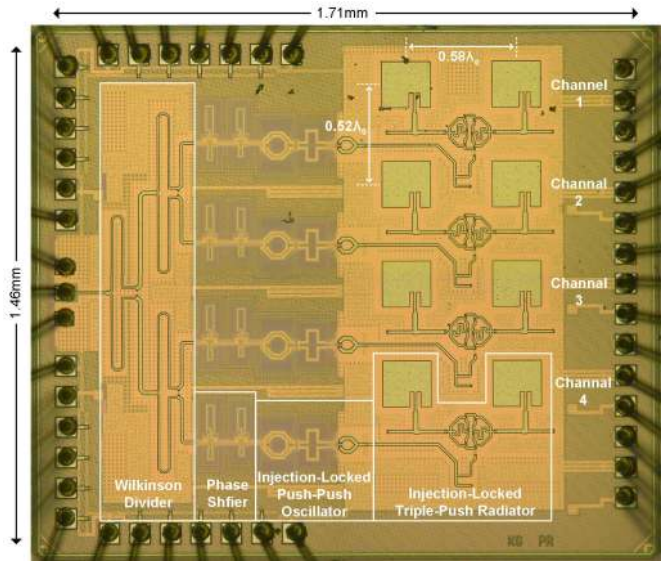



Fig. 14. Die micrograph of the 0.53 THz phased-array.

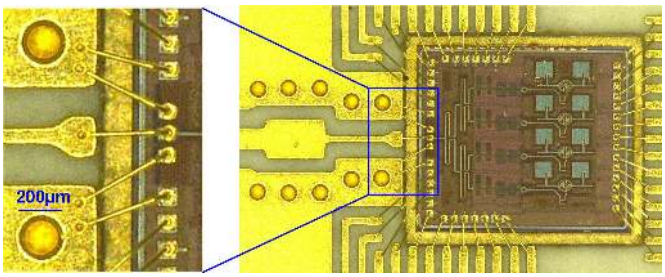
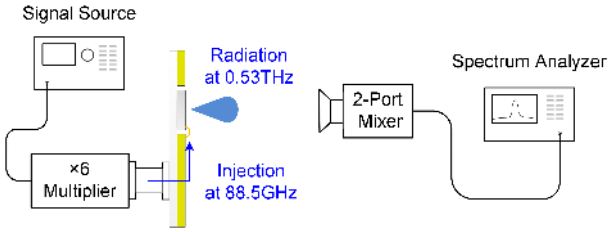
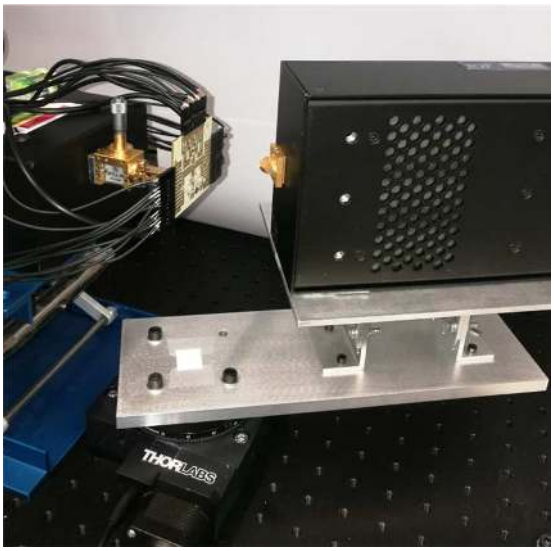



Fig. 15. Photo of wire-bonded chip on PCB.




(a)




(b)

Fig. 16. (a) The measurement setup used to measure the output frequency, radiation pattern and EIRP of the phased-array. This setup is calibrated using a Erickson PM4 power meter and a VDI WR1.5 source module [22], [35], [36]. (b) Photo of the chip package and the rotary test platform.

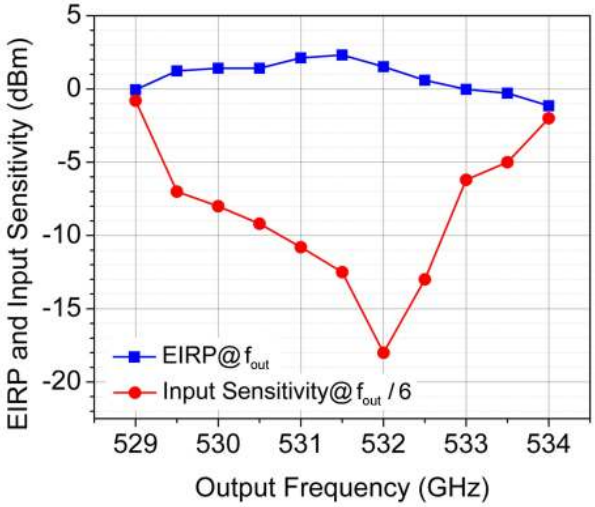



Fig. 17. Measured input sensitivity curve under 0.9 V $V_{DD,3P}$ and measured equivalent isotropically radiated power (EIRP) with a 0 dBm injection power and 0.9 V $V_{DD,3P}$

antennas and the gold bond wires is larger than 200 $\mu$m, and the height of the gold bond wires is lower than 150 $\mu$m in order to avoid the impact of the bond wires on antenna radiation. Simulation shows that the bond wires have negligible impact on the radiation pattern of the phased-array even at the largest beam-steering angle of $\pm 30°$. As shown in Fig. 15, the width of the signal line of the grounded coplanar waveguide (GCPW) is varied to change its characteristic impedance to perform impedance matching for the injection signal at around 88.5 GHz. The measurement setups are shown in Fig. 16. As shown in Fig. 16(a), the chip radiates from the top side without using silicon lens, substrate-thinning or quartz superstrate. The input signal around 88.5 GHz is provided through a waveguide-to-PCB transition and a 11 mm GCPW transmission line. The loss of the GCPW transmission line on the PCB and the waveguide-to-PCB transition is obtained by measuring a stand-alone back-to-back sample and is deembedded from all the measured results of the chip. The measured results of the phased-array include the loss of the PCB-to-chip wire-bond transition. The output frequency, radiation pattern and equivalent isotropic radiated power (EIRP) of the chip are measured using a R&S spectrum analyzer and a VDI WR1.5 down-converting receiver. The distance between the chip and the receiving horn antenna fulfills the far-field distance requirement. This setup is calibrated using a Erickson PM4 power meter and a VDI WR1.5 source module [22], [35], [36]. The directivity of the radiation is calculated using the measured radiation pattern, and the radiated power is obtained using the measured EIRP and directivity [48].

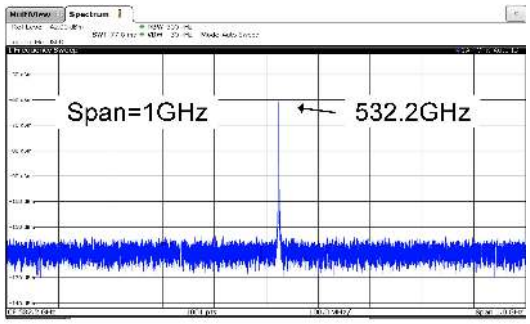



Fig. 18. Output spectrum locked at 532.2GHz, before power calibration.

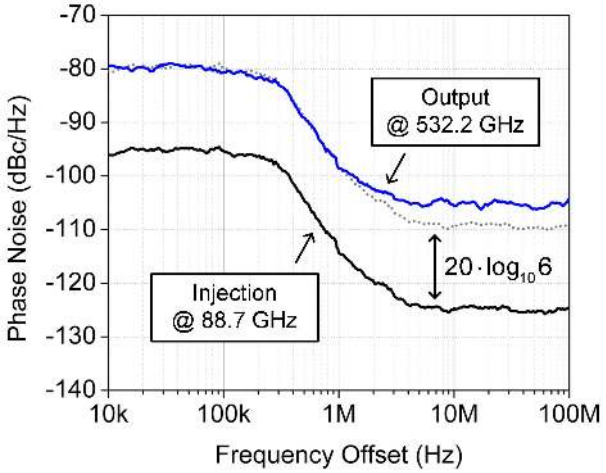



Fig. 19. Measured phase noise of both the output signal at 532.2 GHz and the injection signal at 88.7 GHz.

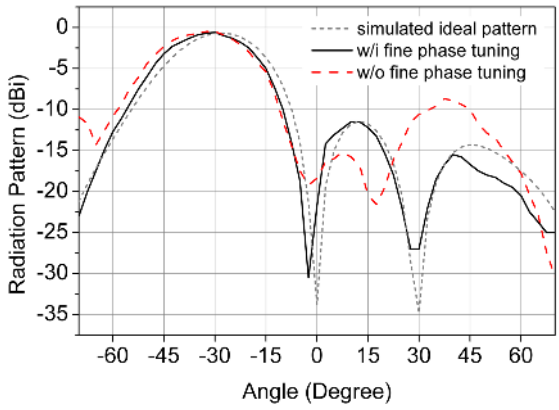



Fig. 20. The measured scanning pattern of the phased-array at 531.5 GHz for the phase setting of (-270°, -180°, -90°, 0°) with and without the fine phase tuning.

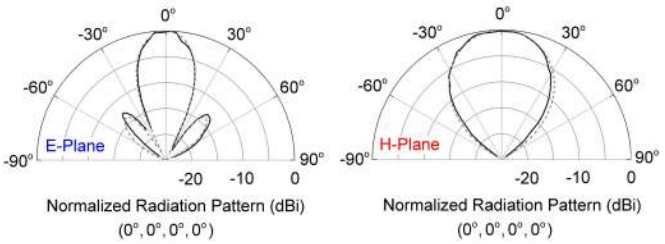



Fig. 21. Measured (solid line) and simulated (dashed line) broadside radiation patterns at 531.5GHz.

Fig. 17 shows the measured EIRP of the phased-array with a 0 dBm injection power when the supply voltage of the triple-push oscillator ($V_{DD,3P}$) is 0.9 V. The peak EIRP is 2.3 dBm at 531.5 GHz. Based on the measured antenna directivity of 14.3 dBi at this frequency, the peak radiated power of the phased-array is calculated as -12 dBm. The measured input sensitivity curve of the phased-array under 0.9 V $V_{DD,3P}$ is also shown in Fig. 17. With less than 0 dBm injection power, the phased-array can be locked from 529 GHz to 534 GHz. Fig. 18 shows the measured output spectrum at 532.2 GHz. Fig. 19 shows the measured phase noise of both the output signal at 532.2 GHz and the injection signal at 88.7 GHz. It can be seen that the output phase noise degradation from the injection signal is by about $20 \cdot \log_{10} 6$ for frequency offset up to 1 MHz.

To perform accurate beam-steering, the phases in the four channels are controled with two steps. First, the 2-bit phase shifters in the four channel are used to provide the coarse phase shift for the target beam-steering angle. Second, the fine phase tuning in the IL-PPOs is used to correct the phase errors caused by the non-ideality of the 2-bit phase shifters. For instance, after the phase states of the 2-bit phase shifters in the four channels of the proposed phased-array are set to (0°, -90°, -180°, -270°), the actual phase difference between adjacent channels in the phased-array may deviate from 90° due to unavoidable phase errors. In order to adjust the phase difference between channel 1 and channel 2 towards the ideal value, channel 3 and channel 4 of the phased-array are turned off, and the combined radiation from channel 1 and channel 2 is measured at the 28.5° direction using the WR1.5 down-converting receiver and the spectrum analyzer. Then, with the control voltage of the IL-PPO in channel 1 kept constant, the control voltage of the IL-PPO in channel 2 is altered and the received power shown on the spectrum analyzer is observed. Once the received power reaches its peak value, a phase difference of 90° is achieved between channel 1 and channel 2 because this 1×2 array with exact 90° phase difference should lead to a beam-steering angle of 28.5° according to the standard equiation [54]. After correcting the phase errors between channel 2 and channel 1, the same procedure is done to adjust the phase difference between channel 3 and channel 2 and the phase difference between channel 4 and channel 3. This way, the phase errors in all the channels are compensated. As shown in Fig. 20, for the phase setting of (-270°, -180°, -90°, 0°), the measured scanning pattern at 531.5 GHz with fine phase tuning matches better with the simulated pattern of the phased-array with ideal phase shift in each channel. After the phase compensation, each phase setting of the phased-array corresponds to a set of control voltages of the four 2-bit phase shifters and a set of control voltages of the four IL-PPOs, and a lookup table is used to record the required control voltages for all the phase setting.

Fig. 21 shows the broadside radiation pattern of the phased-

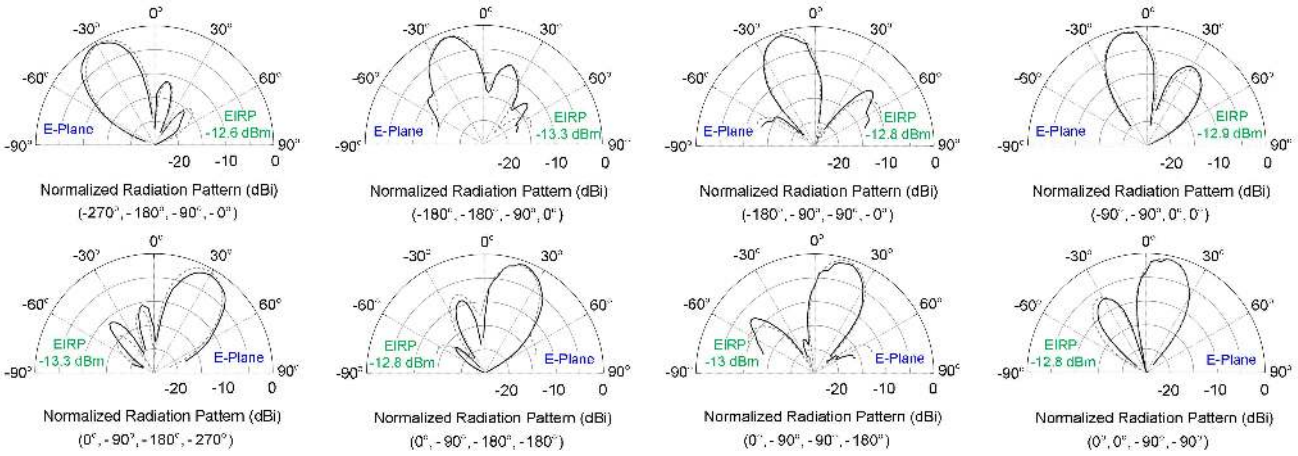



Fig. 22. Measured (solid line) and simulated (dashed line) beam-steering pattern in the E-plane at 531.5 GHz.

TABLE I
PERFORMANCE SUMMARY OF STATE-OF-THE-ART

| | Freq. (GHz) | Beam Steering (°) | $P_{rad}$ (dBm) | Tuning Range (%) | $P_{DC}$ (W) | DC-to-THz Eff. (‰) | EIRP (dBm) | Antenna Type | Configuration | Area ($mm^2$) | Tech. ($f_{max}$) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| This Work | 531.5 | 60 | -12 | 0.9 | 0.260 | 0.24 | 2.3 | Patch Antenna | 1×4 ILO Chain | 2.5 | 40nm Bulk CMOS (300GHz) |
| ISSCC17 [3] | 344 | 128/53 | -6.8 | 15.1 | 0.31 to 0.64[2] | N/A | 4.9 | Patch Antenna | 2×2 Inter-Coupled Osc. | 1.2 | 130nm SiGe (215GHz) |
| JSSC15 [4] | 338 | 45/50 | -0.9 | 2.1 | 1.54 | 0.53 | 17 | Patch Antenna | 4×4 Inter-Coupled Osc. | 3.9 | 65nm Bulk CMOS (250GHz) |
| MTT16 [5] | 390 | 75 | -7 | 10.3 | 1.5 | 0.13 | 8 | Patch Antenna with Quatz Superstrate | 1×8 Multiplier[3] | 10.5 | 45nm SOI CMOS (260GHz) |
| JSSC14 [13] | 530 | 0 | -12[1] | 3.2 | 0.156 | 0.4 | 25 | Ring Antenna with Silicon Lens | 4×4 Non-Coherent Osc. | 4.2 | 130nm SiGe (500GHz) |
| JSSC16 [16] | 553 | 0 | -27 | 3.8 | 0.172 | 0.01 | N/A | Ring Antenna with Silicon Lens | No Array PLL | 2.79 | 65nm Bulk CMOS (240GHz) |
| IMS15 [21] | 546 | 0 | -9 | 1.8 | 1.3 | 0.1 | 24.4 | Ring Antenna with Silicon Lens | 2×4 Inter-Coupled Osc. | 2.16 | 65nm Bulk CMOS (240GHz) |
| RFIC17 [12] | 428 | 0 | -6.8 | 2.1 | 0.164 | 1.42 | 15 | Slot Antenna with Silicon Lens | No Array Osc. + Multiplier | 0.19 | 130nm SiGe (450GHz) |
| JSSC18 [15] | 1010 | 0 | -10.9 | 0.6 | 1.1 | 0.074 | 13.1 | Slot Antenna with Silicon Lens | 6×7 Inter-Coupled Osc. | 1 | 130nm SiGe (450GHz) |
| TTST18 [24] | 528 | 0 | -22 | 5.8 | 0.019 | 0.332 | -7.4 | Slot Antenna with Dielectric Lens | No Array Osc. + Multiplier | 0.12 | 28nm Bulk CMOS (220GHz) |
| MTT18 [8] | 342 | 0 | -10.5 | 5.9 | 0.425 | 0.21 | 1.2 | Patch Antenna | 1×4 Inter-Coupled Osc. | 1.33 | 130nm SiGe (215GHz) |

[1] Average radiated power of a single source pixel in a non-coherent oscillator array.

[2] For frequencies from 370 GHz to 318 GHz. The DC power for 344 GHz with the peak radiated power is not presented.

[3] A 10 dBm input power is needed at 100 GHz.

array at 531.5 GHz. When the four IL-3POs are radiating with the same phase, the phased-array shows a radiation pattern matching well with simulation in both the E-plane and H-plane. Fig. 22 shows the beam-steering performance of the phased-array at 531.5 GHz under different phase setting. All the radiation patterns are normalized to the maximum value at the broadside. The measured beam-steering pattern also matches well with the simulated pattern of the phase-array with ideal phase shift in each channel. For the phase setting of (0°, -90°, -180°, -270°) or (-270°, -180°, -90°, 0°), a beam-steering angle of $\pm 30°$ is achieved.

The isolation between different channels is important in a

phased-array system. In this work, the isolation is measured as follows. Channel 1 and channel 2 are turned on and set to the same phase, while channel 3 and channel 4 are turned off. The combined radiation from channel 1 and channel 2 is measured at the broadside direction while the phase control of channel 3 and channel 4 are changed. During all the coarse and fine phase control in channel 3 and channel 4, the variation of the measured power is less than $\pm 0.2$ dB.

The measured DC power consumption of the chip is 260 mW. Table I compares this work with state-of-the-art silicon-based signal sources with similar output frequencies. This work has the highest DC-to-THz efficiency among all the CMOS signal sources above 0.5 THz without the use of high-resistivity silicon lens or quartz superstrate. Table I also includes previously reported silicon-based THz phased-arrays. Compared to the other THz phased-array designs, this work has the highest operating frequency and the lowest DC power consumption.

## V. Conclusion

This paper presents the first silicon-based phased-array with frequency above 0.5 THz. By using a subharmonic injection-locked architecture based on an ILO chain, the phase error in the phased-array is compensated without introducing power variation. This technique enables accurate beam-steering with a 60° scan range in the E-plane. Combining the radiation from four six-stage triple-push oscillators, -12 dBm radiated power and 0.24‰ DC-to-THz efficiency are achieved at 531.5 GHz without the use of silicon lens, quartz superstrate or substrate-thinning. The required input power for the proposed phased-array is below 0 dBm, and the frequency of input signal is in W-band. Due to the comparatively low input frequency and low input power, the proposed architecture can potentially be scaled to a larger $1\times$N array by adding more channels along the Y direction. Besides, by mirroring the $1\times$N array in the X axis, a $2\times$N array can be composed, and beam-steering in the H-plane can be performed.

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