A 0.5V 1KS/s 2.5nW 8.52-ENOB 6.8fJ/Conversion-Step SAR ADC for Biomedical Applications

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***Abstract*—A low-FOM SAR ADC using the leakage reduction bootstrapped switch (LRBS) to achieve a satisfactory ENOB and using a low-power approach with a low voltage, low sampling rate, and low-DAC-capacitance structure is presented for biomedical applications. LRBS is proposed to alleviate the leakage caused by the low-power approach to increase SNDR and ENOB. From the measurement results, the 0.18µm CMOS prototype chip with the total DAC capacitance of 2.765pF consumes 2.5nW and achieves a SNDR of 53.05dB under a 0.5V supply voltage at 1KS/s with a Nyquist input. The resulting FOM is 6.8fJ/conversion-step.**

I. Introduction

The demands on low-energy CMOS biomedical SoC for the portable devices have been rapidly increased. The successive approximation (SAR) analog-to-digital converter (ADC) has the energy-efficient feature due to the simple structure such that the SAR ADC is suitable for biomedical applications. For SAR ADCs, the sampling rate at KHz level for biomedical signals such as electroencephalography (EEG) and electrocardiography (EKG) is sufficiently required. Generally, the passive sample-and-hold circuit [1]-[5] and low-supply voltage [2]-[6] techniques are applied to the power reduction for SAR ADCs. However, the SAR ADC with sharing sampling capacitance and digital-to-analog converter (DAC) capacitance would face the leakage and signal-to-noise-and-distortion ratio (SNDR)/effective number of bits (ENOB) loss challenge while using above techniques and lowering the DAC capacitance to further save the power. The reasons are as follows. First, due to the low supply voltage, the sampling switch of the SAR ADC suffers from the subthreshold leakage. Second, as the sampling rate decreases, the leakage current through the switches would affect the conversion precision since the total "leaking time" is increased. In addition, the SAR ADC has to hold the voltage stored at the capacitor until the end to the bit cycling phase. Several leakage reduction schemes for sampling switches have been provided in [7]-[9]. However, in [7]-[8], since they either use sampling transistors in series [7] or non-boosted clock [8], it will be difficult to sample at a low supply voltage. In [9], the static power consumption exists. Due to the above reasons, the proposed leakage reduction bootstrapped switch (LRBS) and the low-capacitance structure that shares sampling capacitance and DAC capacitance are adopted in this work to achieve a satisfactory SNDR/ENOB and further reduce the power consumption, respectively. The proposed SAR ADC can achieve the power consumption of 2.5nW and the figure of merit (FOM) of 6.8fJ/conversion-step with a 0.5V supply at the sampling rate of 1KHz.

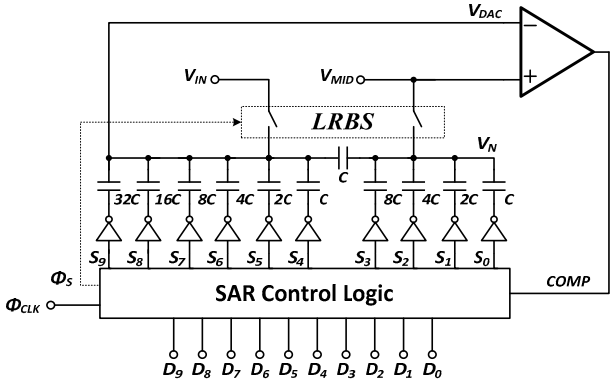

Fig. 1. SAR ADC architecture with the proposed LRBS.

II. Circuit Design

To reduce the power consumption, the SAR ADC employs the low-power approach that combines low voltage, low sampling rate, and low-DAC-capacitance structure. However, the influence of leakage current is incurred such that the SNDR/ENOB becomes worse. LRBS is utilized to reduce the leakage to recover the satisfactory SNDR and ENOB. Fig. 1 shows the block diagram of the SAR ADC architecture with the proposed LRBS. The single-ended configuration is adopted in this work to alleviate the circuit complexity and reduce the power consumption. By employing the single-ended configuration, a fixed reference voltage V_{MID} that equals $V_{DD}/2$ can be tied to the positive input terminal of the comparator to prevent the input offset voltage induced by the variation of common-mode voltage. The split capacitor array of the DAC in Fig. 1 is implemented with the 35fF metal-insulator-metal (MIM) unit capacitors to reduce the power consumption of DAC. For such small capacitors, the layout of the capacitor array utilizes common-centroid placement in [10] and n-well shielding to improve the matching property and reduce the substrate noise coupling, respectively. In the DAC, the reference switches are implemented with the CMOS inverters. The total capacitance of the DAC is 2.765pF. The input signal V_{IN} is sampled at V_{DAC} in the DAC capacitor array during the sampling phase with LRBS. At the same time, the node V_N is reset to V_{MID} using the same circuit. For the SAR ADC with a low supply voltage and a low sampling rate, the charge stored in such small capacitance must be held carefully

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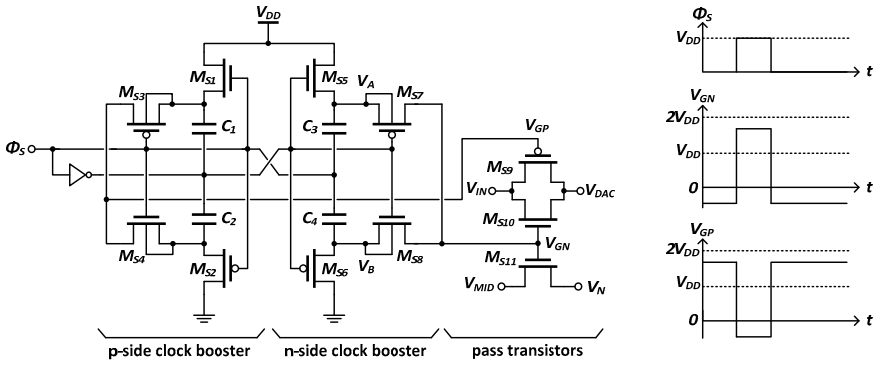

Fig. 2. Proposed LRBS schematic and waveforms of the original and boosted clock.

during the bit cycling phase to keep the conversion precision. Thus, we are motivated to design the LRBS circuit to recover the satisfactory ENOB.

A. Leakage Reduction Bootstrapped Switch (LRBS)

As described in the previous section, the leakage needs to be considered in the low-voltage, low-sampling rate and low-DAC-capacitance SAR ADC. The subthreshold leakage current [11] can be expressed in the following

$$I_{DS} = \mu_0 C_{OX} \cdot \frac{W}{L} \cdot (m-1) \cdot \left(\frac{kT}{q}\right)^2 \cdot e^{\frac{V_{GS}-V_t}{mkT/q}} \cdot \left(1 - e^{-V_{DS} \cdot q/kT}\right) \quad (1)$$

where μ_0 is the zero bias mobility, C_{OX} is the gate oxide capacitance, W/L is the aspect ratio, m is the body effect coefficient, kT/q is the thermal voltage, and V_t is the threshold voltage. In order to decrease the leakage current, the possible approach is either to lower V_{GS} or V_{DS} of the transistor. For the proposed SAR ADC, the control logic controls the DAC output to approximate V_{MID}, so V_{DS} of the pass transistor varies during the bit cycling phase. Hence, the better promising solution to the leakage current is to lower V_{GS}.

To implement such a switch circuit to reduce leakage at a low supply voltage, it is worth emphasizing two notes. First, the conductance of pass transistors is needed to enhance to correctly sample signals. Second, the switch circuit needs to consume no static power for power reduction. The proposed LRBS circuit as shown in Fig. 2 consists of p-side clock booster, n-side clock booster, and pass transistors. LRBS uses the clock boosters to generate not only the boosted high voltage but also the boosted low voltage for the pass transistors. Thus, the turn-on conductance can be enhanced to reduce signal distortion and the turned-off conductance is reduced to alleviate subthreshold leakage with a low supply voltage. The pass transistors for sampling consist of p-type and n-type transistors of M_{S9} and M_{S10}, respectively, to increase the input range by rail-to-rail such that the SNDR can be improved. M_{S11} is used for reset V_N to V_{MID}. In accordance with the design rule, a nearly minimum size is chosen for the pass transistors to alleviate the reversed-bias leakage. In the n-side booster, when Φ_S is high, M_{S6} discharges V_B. Then M_{S7} passes the stored charge in C_3 to V_{GN} to boost the turn-on voltage beyond V_{DD}. As Φ_S becomes low, M_{S5} charges V_A and M_{S8} is turned on to generate a boosted turn-off voltage at V_{GN}.

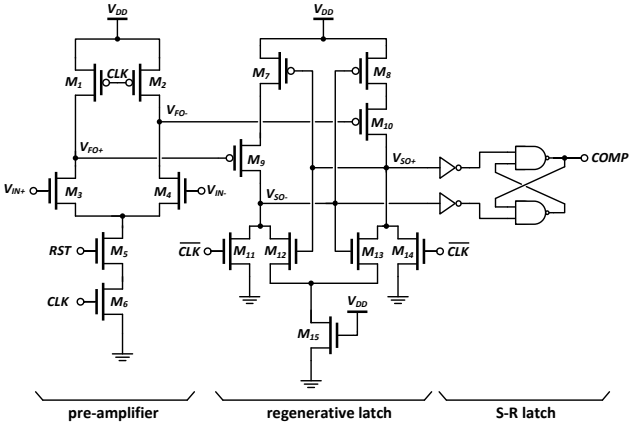

Fig. 3. Three-stage dynamic comparator schematic.

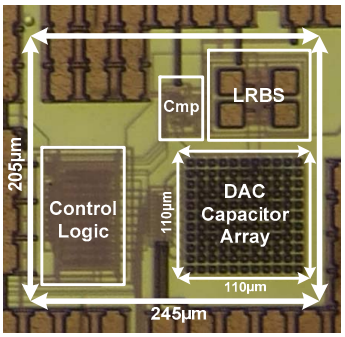

Fig. 4. Chip micrograph.

The n-side booster generates the boosted clock for M_{S10} and M_{S11}. The p-side booster operates similarly as the n-side one to provide the boosted clock for M_{S9}. Both n-side and p-side clock boosters do not consume static power. In the clock boosters, the capacitance of C_1-C_4 is over assigned with 500fF in order to alleviate the parasitic capacitance effect. The post-simulation indicates that the clock booster of the proposed LRBS can generate the boosted high voltage up to 0.84V and the boosted low voltage down to -0.23V. Because the difference of boosted high and low voltages is only about 1V, the doubt of reliability is reduced.

B. Three-Stage Dynamic Comparator

The three-stage dynamic comparator in Fig. 3 is modified from [1]. The dynamic operation of the comparator bypasses

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	JSSC'10 [1]	JSSC'03 [2]		JSSC'09 [3]	JSSC'11 [4]	ISSCC'11 [5]	ISSCC'06 [6]	This Work
Technology	0.065 µm	0.18 µm		0.35 µm	0.18 µm	0.065 µm	0.35 µm	0.18 µm
Active Area	0.026 mm^2	0.11 mm^2		~0.28 mm$^{2\,\dagger}$	0.125 mm^2	0.212 mm^2	~0.52 mm$^{2\,\dagger}$	0.05 mm^2
Resolution	10 bit	9 bit	8 bit	12 bit	10 bit	10 bit	11 bit	10 bit
Supply Voltage	1V	0.6V	0.5V	1V	0.6V	0.55V	1V	0.5V
Input Range	$2V_{pp\text{-}diff}$	$0.3V_{pp}$	$0.125V_{pp}$	Rail-to-Rail		-	Rail-to-Rail	
Sampling Rate	1 MS/s	34 KS/s	4.1 KS/s	1 KS/s	100 KS/s	20 KS/s	1 KS/s	1 KS/s
SNDR	54.4 dB	46.5 dB	43.3 dB	63 dB	57.7 dB	55.0 dB	-	53.05 dB
SFDR	-	-	-	74 dB	67 dB	68.8 dB	-	70.21 dB
ENOB	8.75 bit	7.43 bit	6.90 bit	10.2 bit	9.3 bit	8.84 bit	-	8.52 bit
Power	1900 nW	3120 nW	850 nW	230 nW	1300 nW	206 nW	~851 nW ‡	2.5 nW
FOM	4.4 fJ/c.-s.	531 fJ/c.-s.	1735 fJ/c.-s.	195 fJ/c.-s.	21 fJ/c.-s.	22.4 fJ/c.-s.	-	6.8 fJ/c.-s.
Reconfigurable Resolution	No	Yes		No	No	Yes	No	No

† Estimated from the die photo area. ‡ Calculated from the ISSCC slide material of [6].

not only the static power consumption but also the power demands of the bias circuit. The comparator consists of a dynamic pre-amplifier, a regenerative latch, and an S-R latch for buffering. In the dynamic pre-amplifier, M_5 is located at between the input pair and M_6. In order to save power, the discharging path at the first stage can be blocked when *RST* is disabled during the sampling phase of the SAR ADC. The purpose of M_{15} in the regenerative latch is to bias M_{12} and M_{13} to increase the gain. Since V_{IN+} is connected to V_{MID} to turn on M_3, the comparator can work no matter how low V_{IN-} is. While V_{IN-} is too low to turn M_4 on, V_{FO+} and V_{FO-} will be "0" and "1", respectively, after the evaluation phase of the comparator such that the regenerative latch could operate correctly. Hence, the input range of V_{IN-} can be rail-to-rail without using *p*-type and *n*-type stages in parallel.

C. SAR Control Logic

According to the algorithm from [6], the SAR control logic sets S_0=S_1=…=S_8=1 and S_9=0 at the sampling phase to achieve the rail-to-rail input range. This is because V_{DD}/2 can be subtracted from V_{DAC} at the most significant bit selection during the bit cycling phase. As a result, the range of V_{DAC} can be from V_{IN}-V_{DD}/2 to V_{IN}+V_{DD}/2. Since the control logic leads to large standby leakage power, the stacked device [12] and size scaling techniques are employed in the control logic to increase the threshold voltage. Furthermore, the logic gates are implemented with the pass-transistor logic to increase the resistance in the leakage path.

III. MEASUREMENT RESULTS

Fig. 4 shows the prototype chip fabricated in Taiwan Semiconductor Company (TSMC) 0.18µm 1P6M CMOS process. The core area occupies 0.05mm^2. The linearity and distortion specifications are measured by Agilent 93000 SOC Series Test System. Fig. 5 shows the measured linearity specifications at 1KS/s with a 0.5V supply voltage. The integral nonlinearity (INL) and differential nonlinearity (DNL) are +0.63/-0.82LSB and +0.98/-0.62LSB, respectively. The linearity error is mainly contributed from the parasitic capacitance and the mismatch in the DAC. Fig. 6 shows the output spectrums measured with 6.6528Hz and 499.2065Hz sinusoidal input at 1KS/s and a 0.5V supply. The measured

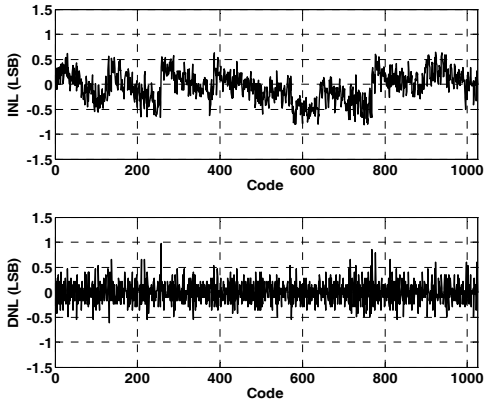

Fig. 5. Measured INL and DNL at 1KS/s with a 0.5V supply.

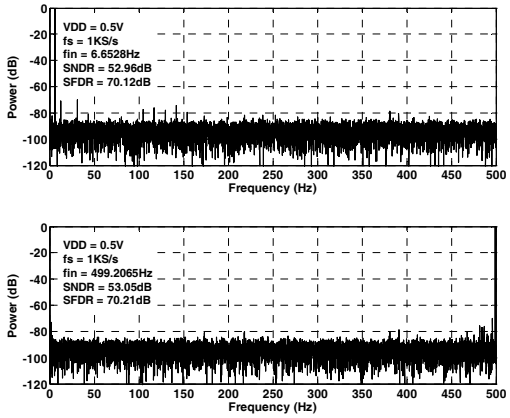

Fig. 6. Measured output spectrums at 1KS/s with a 0.5V supply.

SNDR and spurious-free dynamic range (SFDR) at Nyquist input are 53.05dB and 70.21dB, respectively. That means the ENOB is 8.52bit. As can be seen in Fig. 7, the effective resolution bandwidth (ERBW) can reach the Nyquist frequency. Fig. 8 shows SNDR at Nyquist input versus sampling rate at different supply voltages. The proposed SAR ADC can work with a lower supply voltage of 0.4V. The lower SNDR is obtained at lower V_{DD} due to the noise of the comparator. The current consumption of the SAR-ADC chip is measured by Keithley 6517A electrometer. The measured

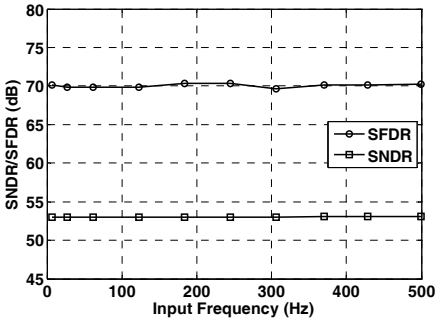

Fig. 7. SNDR and SFDR versus input frequency at 1KS/s with a 0.5V supply voltage.

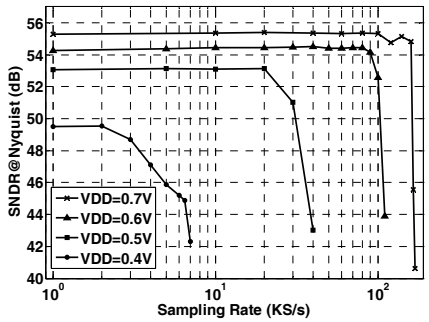

Fig. 8. SNDR versus sampling rate with a Nyquist input at different supply voltages.

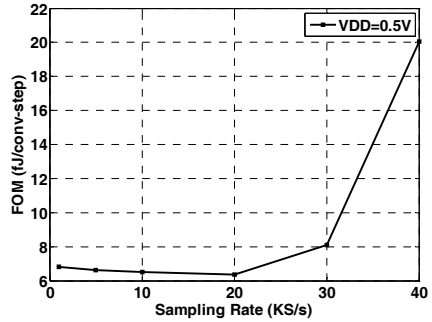

Fig. 9. FOM versus sampling rate with a Nyquist input at a 0.5V supply voltage.

power consumption is 2.5nW in which 58.2% in control logic, 23.5% in capacitive DAC, and 18.3% in analog circuit are determined. The FOM is defined as

$$FOM = Power / \left(2^{ENOB} \cdot \min\left\{2 \cdot ERBW, f_S\right\}\right) \qquad (2)$$

where f_S is the sampling rate. Fig. 9 shows the FOM at Nyquist input versus sampling rate at a 0.5V supply voltage. The resulting and best FOMs are 6.8fJ/conversion-step and 6.4 fJ/conversion-step at 1KS/s and 20KS/s, respectively. The maximum sampling rate is limited by the turn-on conductance of the sampling switch. Due to the range from 1KS/s and 20KS/s, the chip is applicable for not only single- but also multi-channel biomedical signal recording. Table I summarizes the measured specifications and comparison results among the related low-voltage and low-sampling-rate ADCs.

IV. Conclusion

In this paper, the proposed LRBS circuit and the low-power approach with low voltage, low sampling rate and low-DAC-capacitance structure are provided to achieve a low FOM for SAR ADC. In other words, to overcome the leakage caused by the low-power approach, LRBS is proposed to diminish the leakage current of the pass transistors such that SNDR/ENOB can be recovered. The prototype SAR ADC achieves the power consumption of 2.5nW and FOM of 6.8fJ/conversion-step at a 0.5V supply voltage with a low sampling rate of 1KS/s.

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