A 0.6 V, 4.32 mW, 68 GHz Low Phase-Noise VCO With Intrinsic-Tuned Technique in 0.13 μm CMOS

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***Abstract*—An intrinsic-tuned, 68 GHz voltage controlled oscillator (VCO) without an extra on-chip accumulation-mode metal oxide semiconductor (MOS)-varactor is demonstrated in a standard, 0.13 μm CMOS technology. This VCO exhibits phase noises of −98.4 dBc/Hz and −115.2 dBc/Hz at 1 and 10 MHz offset, respectively, along with a tuning range of 4.5% even under a small power consumption of 4.32 mW. Besides, the highest figure-of-merit (taking frequency tuning range into account) of −182 dBc/Hz under the 1 MHz offset condition is achieved among all previously reported >60 GHz CMOS-based VCOs, which is attributed to the proposed intrinsic tuning mechanism.**

***Index Terms*—Accumulation-mode, back-gate, CMOS, intrinsic tuned, millimeter-wave (MMW), phase noise, quality factor, small chip size, varactor, voltage controlled oscillator (VCO).**

I. Introduction

RECENTLY, on-chip, accumulation-mode metal oxide semiconductor (MOS)-varactors have been adopted in millimeter-wave (MMW) voltage controlled oscillators (VCOs) for frequency tuning [1]–[6]. Published MMW VCOs incorporating MOS-varactors [1]–[4] exhibit phase noises between −102.7 and −108 dBc/Hz at 10 MHz offset. This fact indicates that phase noise can be further improved by enhancing the low quality factor (Q) of the MMW varactor (Q ∼12.5 at 24 GHz for $C_{\max}/C_{\min}$ =3.5 [2] and Q ∼5 at 60 GHz for $C_{\max}/C_{\min}$ =2 [7]), which is the main reason for the degradation of figure-of-merit (FOM) of the MMW VCOs. Although, a differential-tuned mechanism has been proposed for suppressing the external noise caused by the measurement [3], the issue about the low Q varactor still remains. Push-push topology is usually utilized for MMW VCO designs [5], [6], where the LC resonant tank is designed at half of the desired output frequency (f_0) to avoid the inherent low gain characteristic of the MOSFET at higher frequencies, so that the oscillation condition can still be easily sustained. Besides, better phase noise can also be achieved by push-push topology due to the high Q characteristic of on-chip accumulation-mode MOS-varactors at lower frequencies. However, process variations will cause an imperfect differential output of the VCO, resulting in a weaker desired signal at f_0 (< −20 dBm in [5], [6]). Therefore, it usually needs an additional amplifier to compensate for the mismatch loss, which consumes extra dc power. Others used a dielectric resonator for enhancing the Q of the LC resonant tank, and thus, a better phase noise was achieved [8]. Nevertheless a tuning range of only 0.2% was reported. In this letter, an alternate way for MMW VCO design is proposed, in which the low Q on-chip accumulation-mode MOS-varactor is replaced by an intrinsic PN junction capacitor for achieving a tunable low phase-noise MMW VCO. Although this method has been adopted in VCOs operated below 10 GHz [9], [10], this work demonstrates that it is especially advantageous in MMW VCOs.

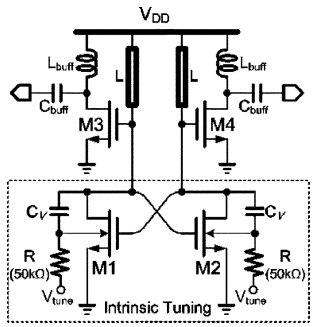

Fig. 1. Schematic of low phase-noise intrinsic-tuned VCO.

II. Intrinsic-Tuned VCO Design

The cross-coupled transistors are utilized to provide the sufficient negative resistance for compensating the losses in the LC resonant tank. Note that parasitic capacitances on the order of several tens of pico-Farads are inevitably associated with these transistors. On the other hand, for a MMW design, the values of the inductance and capacitance of the resonant tank are also on the order of femto-Henry and several tens of pico-Farads, respectively. Therefore the parasitic capacitive effect due to the cross-coupled transistors will become dominant at the oscillation frequencies of MMW VCO. In this letter, we regard the parasitic capacitance as a varactor in cross-coupled transistors, which avoids the use of low-Q accumulation-mode MOS varactor, so that the parasitic capacitance effect is minimized in designing a 68 GHz VCO as shown in Fig. 1. The triple-well device with the intrinsic junction capacitances are also illustrated in Fig. 2. $C_{\rm gsov}$ and $C_{\rm gdov}$ are the overlap capacitances. $C_{\rm ds}$ is the drain-source capacitance. $C_{\rm db}$ is the p-n junction capacitance between drain and bulk of the NMOS (M1 or M2). In the normal operation of an NMOS, the depletion region between the drain and bulk is formed and the p-n junction is re-

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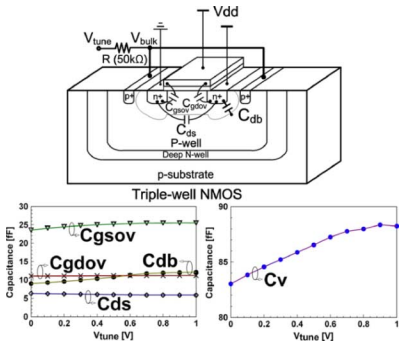

Fig. 2. Triple-well device with the intrinsic junction capacitances.

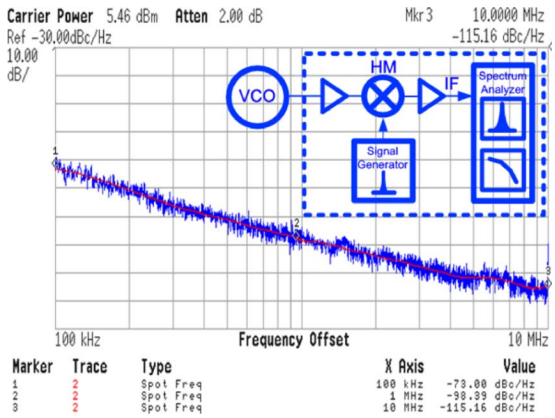

Fig. 3. Measurement setup and measured phase noise of the proposed VCO.

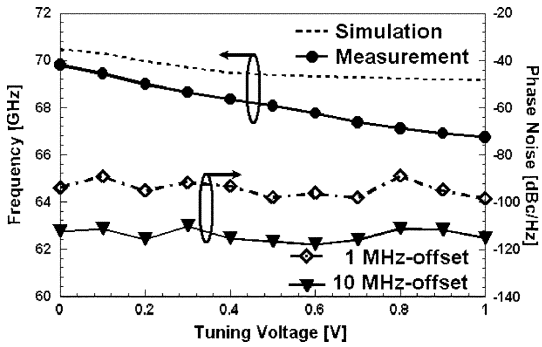

Fig. 4. Measured characteristics of oscillation frequency and phase noise versus tuning voltage.

verse-biased. Once the voltage is decreased at the n-type terminal or increased at the p-type terminal, the depletion region between the drain and bulk is reduced, resulting in a larger junction capacitance $C_{\rm db}$. It can be seen in Fig. 2 that the junction capacitance $C_{\rm db}$ increases from 8.9 to 12.1 fF when the voltage $V_{\rm tune}$ is increasing from 0 to 1 V. However, the drain to bulk voltage must be limited to be less than the turn-on voltage to prevent the p-n junction from entering into the forward-biased region. Besides, the capacitance $C_{\rm gsov}$ slightly increases with increasing $V_{\rm tune}$. Contrarily, the capacitances $C_{\rm gdov}$ and $C_{\rm ds}$ are insensitive to the voltage $V_{\rm tune}$. The effective capacitance C_v at the drain of M1 or M2 is approximately equal to $4C_{\rm gdov}+C_{\rm gsov}+C_{\rm ds}+C_{\rm db}$. The tuning range of $C_{\rm max}/C_{\rm min} = C_v(V_{\rm tune} = 1\ {\rm V})/C_v(V_{\rm tune} = 0\ {\rm V}) \sim 1.1$ in this proposed intrinsic-tuned technique is achieved. A center-tap inductor is utilized for providing the inductance in the LC resonant tank. The top two metals (Metal seven and eight) are stacked together, giving a total metal thickness of 4.8 μm-thick for decreasing the conductor loss. Hence the inductor Q is further improved. Simulations show that an inductance L of 54 pH along with a Q of 20 is obtained at 69.8 GHz. The resonant tank Q of the MMW VCO does not degrade much by the use of the proposed intrinsic tuning topology. The resonant frequency of the proposed VCO can be predicted approximately to be $\omega_0 = 1/\sqrt{L(C_v + C_{\rm buf\_in})}$ when the input capacitance $C_{\rm buf\_in}$ of the output buffer amplifier is taken into account. The output buffer amplifier is designed to prevent the oscillation from frequency drift in future integration. The stack winding inductor is utilized as the choke for the buffer amplifier of the VCO due to its merit of small-size. In the conventional stack inductor design, the distance d between the coil and reference ground is nonzero (e.g., 15 μm) to prevent the coupling caused from other coils or wirings for keeping the inductance stable. Nevertheless, it has been verified by simulation and measurement results that the closed ground (i.e., $d = 0$ μm) stack inductor contributes at least 75% area reduction factor compared to the condition of $d = 15$ μm under the similar inductance from dc to 67 GHz ($L_{\rm buff} \sim 0.21$ nH), which can greatly reduces the whole size of the VCO.

III. Experimental Results

The overall measurement setup for the phase noise is shown in the inset of Fig. 3. The VCO is measured via on-wafer probing with an Agilent 11970 V harmonic mixer (HM) which down-converts the output of VCO to an IF of $\sim$ 365 MHz. And then the IF is further analyzed by the Agilent E4448A 50 GHz spectrum analyzer [2], [4]. Note that two off-chip amplifiers, one before and the other after HM, have been used to compensate for loss due to measurement setup. The circuit is measured with 7.2 mA bias current from a 0.6 V supply. This is the lowest supply voltage among all previously reported CMOS-based MMW VCOs [1]–[6], [8]. If $V_{\rm DD}$ is increased to 1.2 V, simulation results show that both the oscillation frequency and tuning range decrease while the power consumption increases. Note that under the condition of $V_{\rm DD} = 0.6$ V and $V_{\rm tune} = 1$ V, 10.73 μA is going to the PN junction between the bulk and source of M1 (or M2). Since this current is much lower than that (3.6 mA) of drain to source ($I_{\rm ds}$) of M1, its impact is negligible. The discrepancy of $V_{\rm tune}$ and $V_{\rm bulk}$ is due to the use of large resistor R (50 kΩ) between them. From simulations, it is found that the leakage current from bulk to source will become appreciable, i.e., reaching 1/100 of Ids, only when $V_{\rm tune}$ is greater than 2.25 V. Fig. 4 shows characteristics of the phase noise and frequency tuning range (FTR) versus the tuning voltage varied from 0 to 1 V, respectively. The circuit operates with a FTR of 4.5% from the lowest frequency of 66.7 GHz to the highest frequency of 69.8 GHz. Note that while the simulated oscillation frequency is flattened near 1 V, which is consistent with the trend of junction capacitive Cv (see Fig. 2), the measured oscillation frequency does not show this trend. The discrepancy in the tendency between the measured and simulated oscillation frequencies may be attributed to the

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART MILLIMETER-WAVE VCO

Ref.	Technology [μm]	Technique Note	f_o [GHz]	FTR [%]	PN [dBc/Hz]		Power [mW]	FOM [dBc/Hz]		FOM_t [dBc/Hz]	
					1MHz	10MHz		1MHz	10MHz	1MHz	10MHz
[1] ISSCC 2001	CMOS 0.25	MOS-Var.	50	2	-97	/	13 @1.3V	-179.8	/	-165.8	/
[2] JSSC 2006	CMOS 0.13	MOS-Var.	56.5	10.27	-89	-108	9.8 @1.5V	-174.13	-173.13	-174.36	-173.36
			98.5	2.54	/	-102.7	7 @1.5V	/	-174.12	/	-161.63
[3] ISSCC 2005	CMOS 0.12	Differential MOS-Var.	44	9.8	-101	/	7.5 @1.5V	-185	/	-184.8	/
[4] ISSCC 2007	CMOS 0.065	MOS-Var.	70.2	9.55	/	-106.14	5.4 @1.2V	/	-175.76	/	-175.36
[5] ISSCC 2005	CMOS 0.13	Push-Push MOS-Var.	114	2.11	/	-107.6	8.4 @1.2V	/	-179.5	/	-165.96
[6] EL 2006	CMOS 0.13	Push-Push MOS-Var.	192.1	0.68	/	-100	16.5 @1.5V	/	-173.49	/	-150
[8] ISSCC 2006	CMOS 0.09	Resonator	60	0.2	-100	/	1.9 @1.0V	-193	/	-158.8	/
This Work	CMOS 0.13	Intrinsic Cap.	69.8	4.5	-98.4	-115.2	4.32 @0.6V	-188.9	-185.7	-182	/-178.8

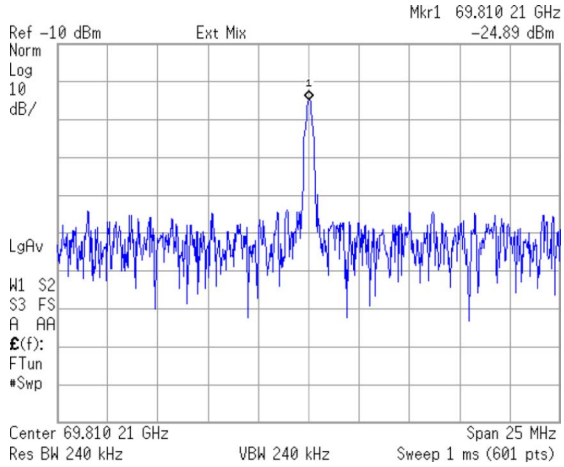

Fig. 5. Spectrum of the proposed VCO before calibrating the cable loss of 9.5 dB.

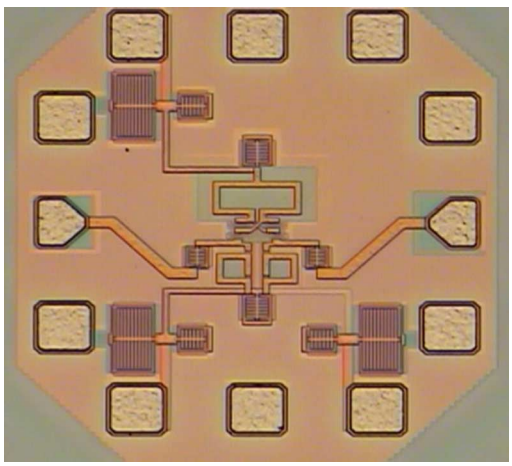

Fig. 6. Chip micrograph of proposed VCO.

inadequate modeling provided by the foundry, which is valid only up to 30 GHz. Measured phase noises of < -89 dBc/Hz and < -110 dBc/Hz at 1 and 10 MHz offset away from the carrier, respectively, are achieved over the whole tuning voltage. Output power of > -24.8 dBm without calibrating the cable loss of 9.5 dB is also obtained as shown in Fig. 5. The carrier power is much smaller than that in Fig. 3 because no amplifier/HM is used for this measurement. The die micrograph of the fabricated VCO including the buffer amplifier is shown in Fig. 6 with the core size of only $120 \times 130\ \mu\text{m}^2$.

IV. CONCLUSION

In this letter, the intrinsic-tuned 68 GHz VCO without an extra low-Q device is reported. This VCO achieves a phase noise of -115 dBc/Hz at 10 MHz offset, which is 7.2 dB better than the best [2] of all previous publications. Besides, compared with previous >60 GHz MMW VCOs [2], [4]–[6], [8], it is also found that the proposed VCO obtains the best FOM taking FTR into account [4] of $-182/-178.8$ dBc/Hz at 1/10 MHz offset, which is attributed to the removal of the low-Q varactor in the tunable oscillator (see Table I).

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