A 0.6-V Delta–Sigma Modulator With Subthreshold-Leakage Suppression Switches

Hyungdong Roh, Hyoungjoong Kim, Youngkil Choi, Jeongjin Roh, Yi-Gyeong Kim, and Jong-Kee Kwon

***Abstract*—A 0.6-V 34-μW delta–sigma modulator implemented by using a standard 0.13-μm complementary metal–oxide–semiconductor technology is presented. This brief analyzes a subthreshold-leakage current problem in switched-capacitor circuits and proposes subthreshold-leakage suppression switches to solve the problem. To verify the operation of the subthreshold-leakage suppression switches, two different fifth-order delta–sigma modulators are implemented with conventional switches and new switches. The input feedforward architecture is used to reduce the voltage swings of the integrators. A high-performance low-quiescent amplifier architecture is developed for the modulator. The modulator, with new switches, achieves a dynamic range of 83 dB, a peak signal-to-noise ratio of 82 dB, and a peak signal-to-noise-plus-distortion ratio of 81 dB in a signal bandwidth of 20 kHz. The power consumption is 34 μW for the modulator, and the core chip size is 0.33 mm^2.**

***Index Terms*—Analog-to-digital converter (ADC), delta–sigma modulator, harmonic distortion, leakage current, signal-to-noise-plus-distortion ratio (SNDR), switched-capacitor circuit.**

I. Introduction

In DIGITAL circuits, reducing the channel length provides high integration density, high speed, and low power consumption. Therefore, the minimum channel length continuously decreases as a result of advances in CMOS processing technology. In analog circuits, the maximum allowable voltage swing decreases and noise sensitivity increases due to the reduction of the supply voltage that results from a reduction in the channel length. It is difficult to design analog circuits with shorter channel lengths. Analog-to-digital converters (ADCs) are based on analog circuitry. A switched-capacitor delta–sigma ADC is suitable for operation at low supply voltages, since it is very robust against noise. However, a switched-capacitor circuit does not properly operate at very low supply voltages since the threshold voltage does not decrease with a decrease in the supply voltage, causing an increase in the switch impedance.

The typical solutions to this problem are the switched opamp [1], [2] and clock-boosting schemes [3]. However, using a switched opamp reduces the operation speed and makes it difficult to obtain a high resolution. The clock-boosting technique reduces the on-resistance by applying a gate voltage that is higher than the supply voltage, but it introduces a reliability issue. A third resolution to the switch-driving problem is to use low-$V_{\rm th}$ transistors for the CMOS switches. However, using a low-$V_{\rm th}$ transistor in a switch significantly increases the leakage current through the transistor in the subthreshold region. An analog T-switch (AT-switch) circuit was proposed in [4] for reducing the effects of the leakage current of a switched-capacitor circuit by forcing the reverse gate–source voltage $V_{\rm GS}$.

This brief analyzes the subthreshold-leakage current in the sample-and-hold (SH) stages and proposes a new switch to effectively alleviate the problem. To verify the performance of the new switches, two different fifth-order fully differential switched-capacitor modulators are designed and implemented.

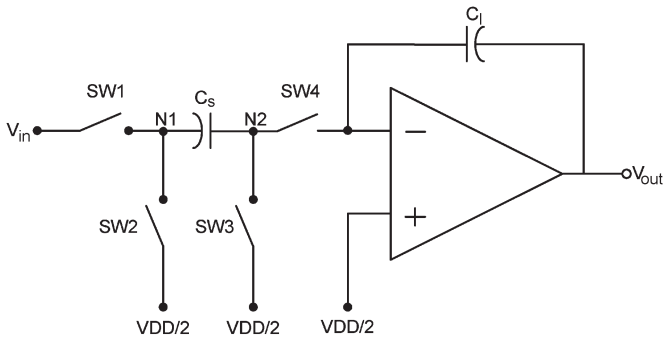

Fig. 1. Conventional switched-capacitor integrator.

II. Analyzing the Leakage Problem

Fig. 1 shows a conventional switched-capacitor integrator, shown in a single-ended architecture for simplicity. In general, the input switch SW1 is made with a CMOS transmission gate for a wide input-voltage swing, whereas the SW2, SW3, and SW4 switches only use NMOS transistors. For a noninverting delaying operation of the integrator in Fig. 1, SW1 and SW3 are closed during the sampling phase to charge the sampling capacitor C_s, and SW2 and SW4 are closed during the integrating phase to deliver the charge stored in C_s to the output. Although there is no current through an ideal MOS switch, if the voltage between the gate and the source is less than the threshold voltage, then in reality there could be a small amount. If we denote the on-resistance of SW1 at the end of the sampling phase as $R_{\rm on,SW1}$ and assume that $V_{\rm in}$ is higher than $VDD/2$, then the voltage at the N1 node becomes

$$V_{\rm N1} = V_{\rm in} - R_{\rm on,SW1} \cdot I_{\rm SW2}. \quad (1)$$

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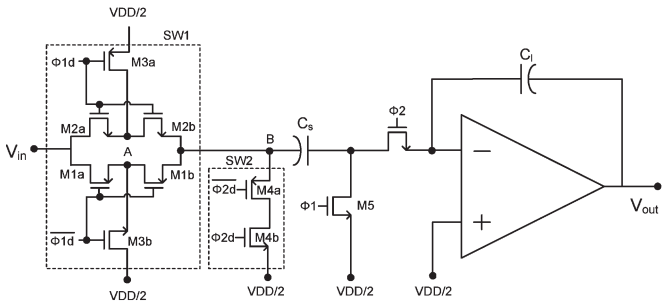

Fig. 2. Switched-capacitor integrator with AT-switch [4].

The voltage at the N1 node during the integrating phase becomes

$$V_{\mathrm{N1}} = \frac{VDD}{2} + R_{\mathrm{on,SW2}} \cdot I_{\mathrm{SW1}}. \tag{2}$$

As shown in (1) and (2), voltage errors occur due to the leakage current flowing through the turned-off switches. When the input voltage becomes lower than $VDD/2$, the minus/plus signs of the equations change. The two equations clearly show that the errors are dependent on the input voltage, and this implies that the distortions will be caused by the errors. The leakage current can be expressed as follows [5], [6]:

$$I_{\mathrm{ds}} = \mu_0 C_{\mathrm{ox}} \frac{W}{L}(m-1)(\nu_T)^2 \cdot e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{TH}}}{m\cdot\nu_T}} \cdot \left(1-e^{\frac{-V_{\mathrm{DS}}}{\nu_T}}\right). \tag{3}$$

The foregoing equation can be simplified into the following relationship:

$$I_{\mathrm{ds}} \propto \frac{W}{L} \cdot e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{TH}}}{m\cdot\nu_T}} \cdot \left(1-e^{\frac{-V_{\mathrm{DS}}}{\nu_T}}\right) \tag{4}$$

where m and ν_T denote the body effect coefficient and the thermal voltage, respectively. The preceding equations show that the leakage current depends on V_{DS}, which is determined by the input voltage for SW1. This implies that if the amplitude of the input voltage increases, then the leakage current increases to generate harmonic distortions.

There are two ways of reducing the leakage current by using (4) without significantly increasing the length of a transistor, which will unacceptably increase the on-resistance of the switch. The first involves applying a reverse voltage across the gate and the source [4]. If V_{GS} is below 0 V, then the transistor's operating region moves toward the deep inside cutoff region to reduce the leakage current. Fig. 2 shows an example of reducing the leakage current by decreasing V_{GS} to below 0 V. In the sampling phase, a reverse voltage is applied to one of the two transistors (M4a or M4b) to block the leakage current. In the integrating phase, $VDD/2$ is applied between M1a (or M2a) and M1b (or M2b), resulting in a reverse voltage across the gate and the source at each transistor, which reduces the leakage current.

Since the delta–sigma modulator is a feedback system, a feedback digital-to-analog converter (DAC) can be connected to the integrator in two ways. The first scheme is to implement another switched-capacitor branch to the negative input of the amplifier, which is in parallel with the input signal path. A more commonly used scheme is to apply the feedback voltage to the bottom end of the SW2 in Fig. 1, which reduces the number of capacitors and switches. However, in the AT-switch scheme, the feedback voltage cannot be connected to the bottom end of the SW2 in Fig. 2 since the feedback voltage changes at each switching cycle and the reverse V_{GS} cannot be guaranteed. To block the leakage current of M4a and M4b, the bottom end of SW2 must be connected to the constant dc voltage of $VDD/2$. Accordingly, an additional SH circuit must be implemented for the feedback signal path. The separate feedback branches also require large capacitors to reduce the kT/C noise. Therefore, the chip area is necessarily large since the capacitors generally occupy large areas in the switched-capacitor modulator layout.

III. New Switch Design

The second method of reducing the leakage current is to equalize the drain and source voltages in (4). The voltage difference between the drain and the source can be set to 0 V in the $1 - e^{-V_{\mathrm{DS}}/\nu_T}$ term to completely remove the leakage current. Based on this principle, a new leakage current suppression circuit is developed in this brief. Fig. 3 shows the operation of the proposed circuit during the sampling and integration phases. The thick lines indicate the connected signal paths. The waveforms at the bottom are the nonoverlapping clock waveforms, and the clock phase corresponding to operation is indicated by dashed lines.

Fig. 3(a) shows the sampling phase operation. SW1 and SW2 are turned on during the sampling phase, and SW3, SW4, and SW6 go into the cutoff region. At this time, SW5 is also turned on so that an identical voltage can be placed at N1, N2, and N3. SW1, SW2, and SW5 are turned off during the integrating phase, and SW4 and SW6 are turned on. SW3 is also turned on to completely block the leakage current through SW2.

The leakage current during the sampling phase is completely removed by the proposed switch configuration, whereas the leakage current during the integrating phase might still exist through SW5 if the size is not carefully determined. SW5 might have a high drain–source voltage during the integrating phase, and this might cause a leakage current that will change the voltage at the N2 node. In (1) and (2), the error voltage is expressed as a product of R_{on} and the leakage current. In our design, the widths of the SW6 transistors are increased to reduce $R_{\mathrm{on,SW6}}$, whereas the length of the SW5 transistors is increased to minimize the leakage current. This way, the error voltage can be reduced to a negligible level. The large switch size of SW6 increases the leakage current during the sampling phase, but this does not affect the accurate operation of the circuit because SW3 and SW4 are completely turned off. In addition, the large turn-on resistance of SW5 during the sampling phase does not degrade the overall speed of the circuit since the parasitic capacitance at the N2 node is very small compared with the capacitance at the N3 node. The leakage currents through SW7 and SW8 are not considered because there exists a reverse V_{GS} in these switches.

In the proposed technique, to maintain the turn-on resistance, the widths of SW1 and SW2 in Fig. 3 are double those of the conventional switch. Since the most critical node for fast settlement in the switched-capacitor integrator is the virtual

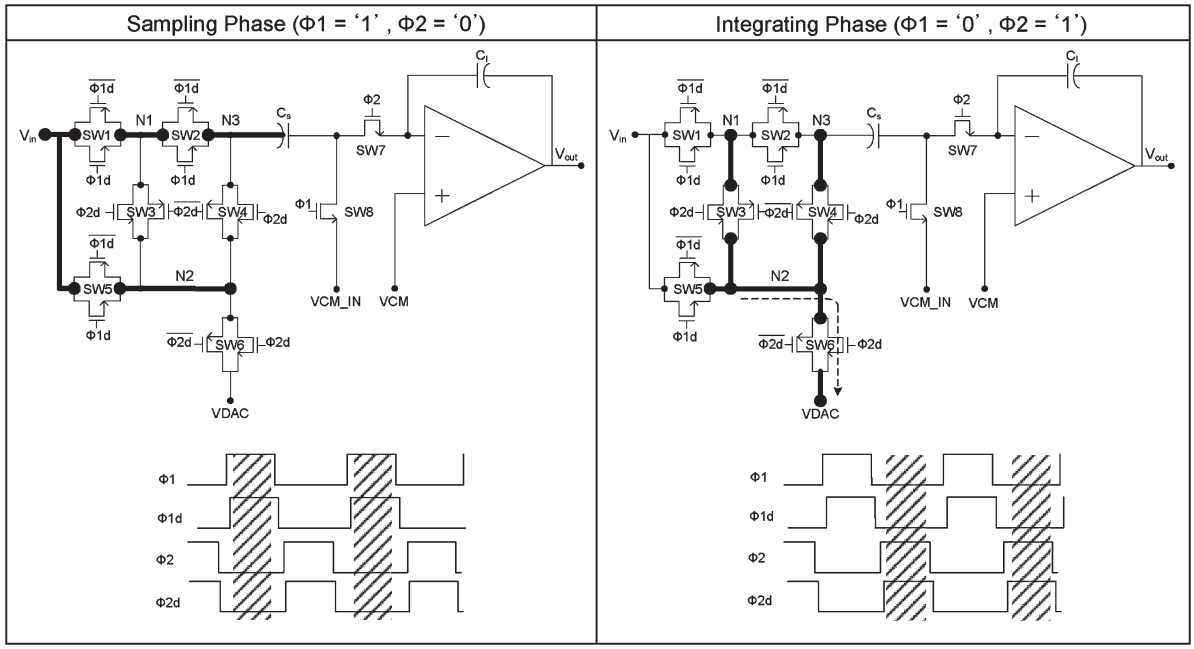

Fig. 3. Switched-capacitor integrator with proposed switch during (a) the sampling phase and (b) the integrating phase.

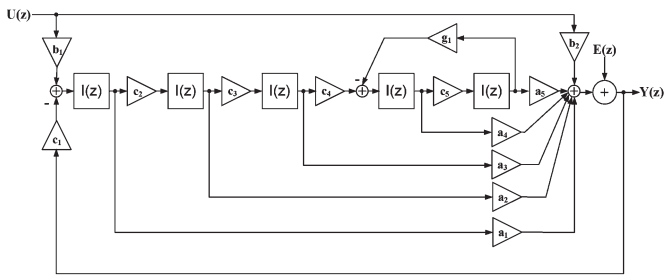

Fig. 4. Block diagram of a fifth-order single-bit input feedforward delta–sigma modulator.

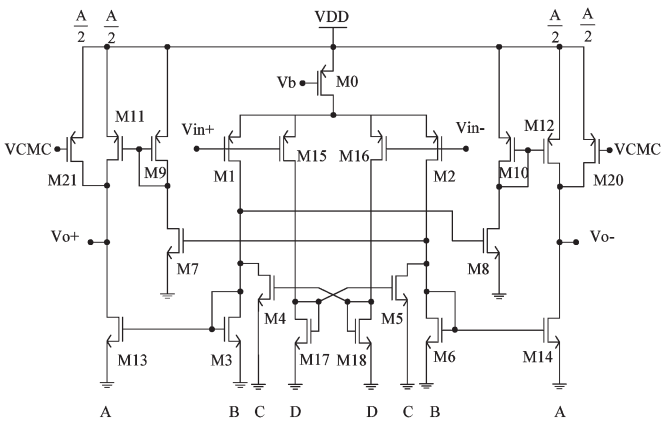

Fig. 5. Designed OTA.

ground node (operational transconductance amplifier (OTA) input node), the parasitic capacitances from these doubled switches do not degrade the performance, which is also verified from simulations and by using chip measurements. This doubling of the switch size might cause an increased charge injection, which is usually reduced by the use of delayed clocks [7].

IV. Implementation

This section describes the structure of the designed modulator and its circuit implementation. Only the new OTA architecture is explained, and other common blocks, which are similar to the circuits used in [9], are not described here.

Fig. 4 shows a single-bit fifth-order input feedforward modulator. In an input feedforward structure, the signal swings at the internal nodes of the modulator are reduced since only the quantization noise is processed in the loop filter of the modulator [10]–[12]. Therefore, the input feedforward structure is widely used in low-voltage low-power modulators. The coefficients of the modulator are optimized based on simulations, and the dynamic range is scaled according to the OTA's restrictions and the amplitude of the internal signal, as was done in [9]. The fifth-order architecture is selected to achieve a high signal-to-noise-plus-distortion ratio (SNDR) with a low oversampling ratio for relaxed OTA requirements. The noise transfer function is designed to achieve stable operation. The two pairs of optimized zeros can be designed for fifth-order modulators, but only one pair is implemented to avoid an extremely small coefficient value [8].

The OTA is an important block that consumes a significant amount of power. Therefore, it is important to choose an OTA structure that achieves high performance with low power consumption. A cascode topology is generally used to increase an OTA's gain. However, the reduced voltage headroom caused by using cascoding makes it difficult to use in low-voltage applications. Fig. 5 shows the OTA structure used in the proposed modulator, which is a fully differential version of that reported in [14]. At the input stage of the OTA, the loads of the M1

TABLE I
SIMULATED PERFORMANCES OF THE OTAS

Parameter	OTA1	Other OTAs
Supply voltage (V)	0.6	0.6
Power consumption (μW)	14.7	4.4
DC gain (dB)	53	50
Phase margin (degree)	32	38
GBW (MHz)	39	30
Slew rate (V/μs)	16	24
Effective load capacitance ($C_{L,eff}$) (pF)	3	0.5

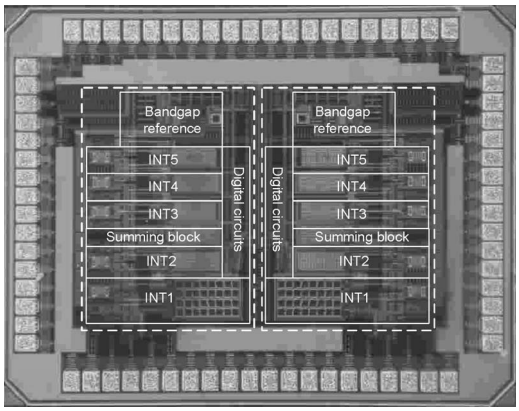

Fig. 6. Die photograph. (Left side) Modulator with the new switches. (Right side) Modulator with the conventional switches.

and M2 transistors are divided among M3, M4, M5, and M6. The letters at the bottom of Fig. 5 represent the W/L ratio of each transistor. The size of M1 is equal to B + C, which is the sum of M3 and M4, and the size of M15 is D. Therefore, the OTA's transconductance and output resistance can be expressed as

$$\begin{aligned} G_m &= \frac{3}{2} \times g_{m1,2} \times \frac{A}{B} + \frac{3}{2} \times g_{m15,16} \times \frac{C}{D} \times \frac{A}{B} \\ &= \frac{3}{2} \times \frac{I_t}{V_{OD}} \times \frac{A}{B} \times \frac{B+2C}{B+C+D} \\ R_{\text{out}} &= (r_{o20,o21} \| r_{o11,o12} \| r_{o13,o14}) \\ &= \frac{B+C+D}{A} \times \frac{4}{(\lambda_{20,21} + \lambda_{11,12} + 2\lambda_{13,14}) I_t}. \end{aligned} \quad (5)$$

From the foregoing equations, the OTA's gain can be obtained as

$$A_v = \left(1 + \frac{2C}{B}\right) \times \frac{6}{V_{OD}(\lambda_{20,21} + \lambda_{11,12} + 2\lambda_{13,14})}. \quad (6)$$

The gain equation [see (6)] indicates that the OTA's gain can be adjusted with the W/L ratio of M4/M3 and M6/M5. The current through M4 and M5 is reused to increase the OTA's gain.

The simulated performances of the OTAs are shown in Table I. Since the phase margin is low, the OTA input and output voltages have slight ringing at the beginning of the clock cycle in the capacitive feedback configuration. However, the amplifiers have high gain–bandwidth products (GBW) of 39 or 30 MHz for the 1.92-MHz clock frequency, so they settle with sufficient accuracy after the slight ringing [9].

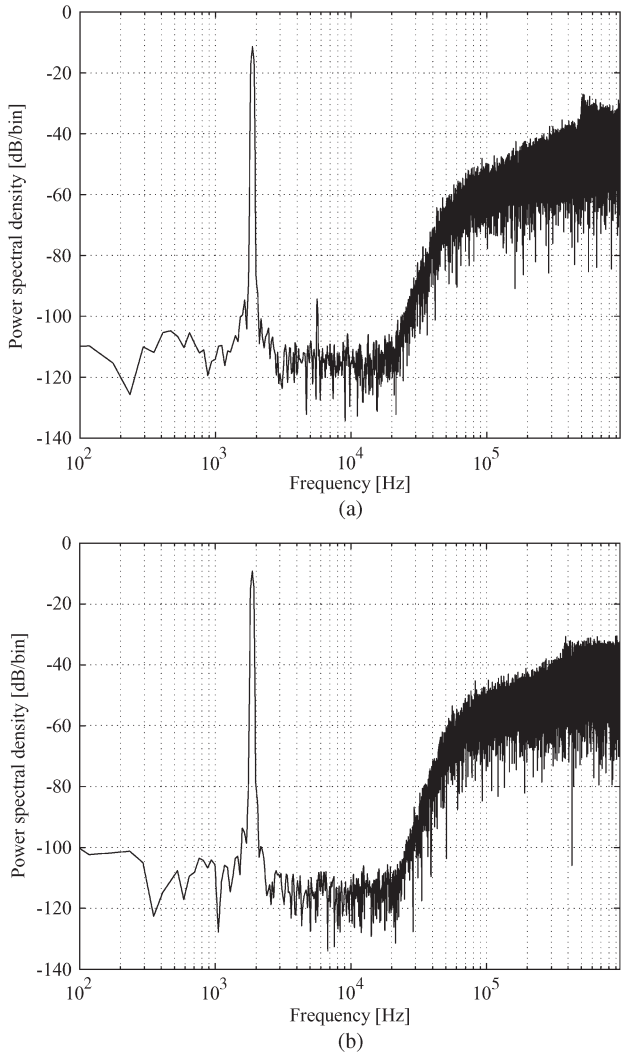

Fig. 7. Measured output spectra with and without leakage suppression switches. (a) Measured output spectrum with conventional switches (−5.5-dB input for peak SNDR). (b) Measured output spectrum with new switches (−3-dB input for peak SNDR).

TABLE II
PERFORMANCE SUMMARY

	Without leakage suppression circuit	With leakage suppression circuit
Supply voltage	0.6 V	0.6 V
Power consumption	34 μW	34 μW
Peak SNR	81 dB	82 dB
Peak SNDR	77 dB	81 dB
Sampling frequency	1.92 MHz	1.92 MHz
Signal bandwidth	20 kHz	20 kHz
Oversampling ratio	48	48
Core size	0.33 mm^2	0.33 mm^2

V. MEASUREMENT RESULTS

Two kinds of modulators are implemented by using a standard 0.13-μm CMOS process with threshold voltages of −150 and 200 mV for PMOS and NMOS, respectively. Fig. 6 shows a photograph of the fabricated chip incorporating two modulators that are vertically symmetrical. The left side modulator uses the new switches, and the right side uses the conventional switches.

TABLE III
PERFORMANCE COMPARISON OF LOW-VOLTAGE DELTA–SIGMA MODULATORS

Paper	Architecture	VDD [V]	Process	SNDR [dB]	BW [kHz]	P [μW]	Core size [mm^2]	FOM [pJ/conversion-step]
Sauerbrey 2002 [2]	$\Delta\Sigma$: SO	0.7	0.18 μm CMOS	67	8	80	0.082	2.73
Roh 2008 [9]	$\Delta\Sigma$: 4(1b) SC	0.9	0.13 μm CMOS	73	20	60	0.42	0.411
Yao 2004 [13]	$\Delta\Sigma$: 3(1b) SC	1.0	90 nm CMOS	81	20	140	0.18	0.381
Goes 2006 [15]	$\Delta\Sigma$: 2(1b) SC	0.9	0.18 μm CMOS	80	10	200	0.06	1.209
Pun 2007 [16]	$\Delta\Sigma$: 3(1b) CT	0.5	0.18 μm CMOS	74	25	300	0.6	1.465
Chae 2008 [17]	$\Delta\Sigma$: 3(1b) SC	0.7	0.18 μm CMOS	81	20	36	0.715	0.098
Kim 2008 [18]	$\Delta\Sigma$: 3(1.5b) SRC	0.9	0.13 μm CMOS	89	24	1500	1.44	1.356
This Work	$\Delta\Sigma$: 5(1b) SC	0.6	0.13 μm CMOS	81	20	34	0.33	0.092

SC: Switched-Capacitor, CT: Continuous-Time, SO: Switched-Opamp, SRC: Switched-RC.

The test board was also symmetrically designed for an accurate comparison of the modulators.

The output spectra of the modulators are shown in Fig. 7(a) and (b) with 1.875-kHz sinusoidal inputs. The power supply rails, V_{DD} and ground, which are assumed as a 0-dB full-scale input level in this brief, are used as feedback DAC reference voltages. The input levels for Fig. 7(a) and (b) are -5.5 and -3 dB, respectively, and 32k sampling points are used for each spectrum. The harmonic distortions are significantly reduced by using the proposed switches. The modulator with new switches achieves a peak SNDR of 81 dB, and the modulator with conventional switches achieves a peak SNDR of 77 dB from these spectra.

Table II compares the performance of modulators employing the new switches with those employing the conventional switches. The figure-of-merit (FOM) equation is

$$\text{FOM} = \frac{P}{2^{\frac{(\text{SNDR}-1.76)}{6.02}} \cdot 2 \cdot BW} \tag{7}$$

where BW and P denote signal bandwidth and power, respectively. The bandgap circuit consumes 8 μW of power, but it is not included in the power consumption of the modulator for the FOM calculation. The 1 μW of power used by the nonoverlapping clock generator is included in the modulator power consumption. The FOM is used to compare the state-of-the-art low-voltage modulators, as shown in Table III. While both of the two designed modulators show good performance with low power consumption, the modulator with the new switches achieves the lowest FOM among the low-voltage modulators by reducing the harmonic distortions.

VI. CONCLUSION

A low-voltage low-power delta–sigma modulator has been designed by using the standard 0.13-μm CMOS process. The input feedforward structure is used to reduce the output swings of the integrators. Furthermore, a high-performance OTA architecture is implemented to minimize power consumption. The leakage problem, with respect to the low-V_{TH} transistor, is solved by using the new switches. The implemented circuit achieves a higher level of performance among the state-of-the-art sub-1-V modulators.

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