A 0.6GHz to 2GHz Digital PLL with Wide Tracking Range

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***Abstract*— A digital PLL employing an adaptive tracking technique and a novel frequency acquisition scheme achieves a wide tracking range and fast frequency acquisition. The test chip fabricated in a 0.13μm CMOS process operates from 0.6GHz to 2GHz and achieves better than $\pm$3200ppm frequency tracking range when the reference clock is modulated with a 1MHz sine wave.**

I. Introduction

Advances in the IC fabrication technology have made digital implementations of phase-locked loops (PLLs) preferable over their analog counterparts. The benefits of a digital implementation are easy scalability with process shrink, elimination of the noise susceptible analog control for an oscillator, and the inherent noise immunity of digital circuits. Recently, several digital PLLs (DPLLs) have been reported [1]–[4] and demonstrate the ability of DPLLs to achieve the performance of analog PLLs and even outperform them.

Bang-bang or binary phase detectors (PDs) are commonly used in digital PLLs. The inherent bang-bang behavior of the reported DPLLs [3], [4] imposes an upper bound on the tracking bandwidth of a DPLL and thus limits its capability to track frequency modulated input signals. On the other hand, a phase detector with sub-picosecond resolution allows one to design a DPLL with a near-linear behavior and thereby achieve a wide-tracking bandwidth [5]. However, such a phase detector occupies a large area and consumes excessive power. The bang-bang phase detectors also limit the pull-in range of DPLLs to less than 10% of the oscillator free-running frequency. Consequently, bang-bang DPLLs require frequency acquisition aids such as a frequency-locked loop (FLL) operating in parallel with the PLL to achieve a wide-operating range. Although there are many ways to accomplish frequency locking in DPLLs, all of them suffer from a major drawback of slow frequency acquisition.

In this paper, we present a new digital PLL that targets both of the drawbacks mentioned above. The proposed DPLL employs (i) an adaptive tracking mechanism to improve the frequency tracking range, and (ii) a new frequency detector to allow for fast frequency acquisition. The paper is organized as follows. The dynamics of a bang-bang DPLL are examined in Section II and show the inherent tracking problems due to the bang-bang PD. Section III proposes a solution to improving the tracking range of bang-bang DPLLs. A new frequency detector for fast frequency lock is described in Section IV and the overall DPLL architecture is presented in Section V. Experimental results from the fabricated prototype DPLL are shown in Section VI and the paper is concluded in Section VII.

II. Dynamics of a DPLL with a Bang-Bang Phase Detector

A digital PLL (Fig. 1) consists of a bang-bang phase detector (!!PD), a digital loop filter (DLF), a digitally-controlled oscillator (DCO), and a feedback divider with a division ratio of N. A distinguishing feature of this DPLL is its bang-bang phase detector, that can determine only the sign of the phase error. Quantization of the phase error with only one bit introduces a strong nonlinearity into the loop and thus prevents us from using linear analysis techniques. The proportional-integral DLF is implemented by a proportional path that directly controls the DCO and an integral path that accumulates the phase error and controls the DCO separately. The z-domain transfer function of the DLF is given by Eq. (1),

$$H_{DLF}(z) = K_P + K_I \frac{z^{-D}}{1 - z^{-1}}, \qquad (1)$$

where K_P and K_I represent the gain of the proportional and the integral paths, respectively, and D is the integral path delay measured in units of reference clock cycles. For applications

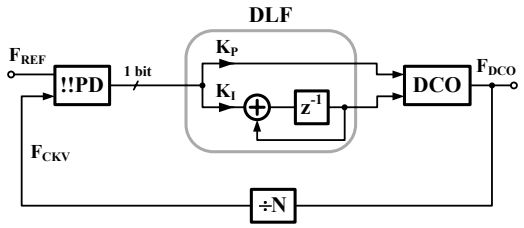

Fig. 1. Bang-bang digital PLL.

like Serial Advanced Technology Attachment (SATA) [6], that use spread-spectrum clocking, the frequency of the reference clock is not constant, but rather changes according to the frequency modulation profile. Thus, a bang-bang PLL has to track the frequency of the modulated reference clock. There are two ways a bang-bang DPLL can track the reference frequency modulation: (i) via the proportional path of the DLF, and (ii) via the integral path of the DLF. Fig. 2 shows how the DPLL divided clock F_{CKV} tracks the frequency modulated reference clock F_{REF}. The maximum frequency deviation that the proportional path can track is limited to: $\Delta F_{K_P} = \frac{K_P K_{DCO}}{N}$.

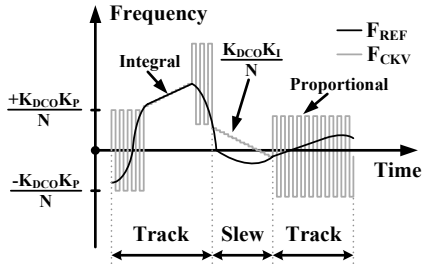

Fig. 2. Frequency tracking by a bang-bang DPLL.

If the amplitude of the frequency modulation exceeds the range of the proportional path, the integral path has to perform the tracking. The maximum frequency deviation that the integral path can track is limited by the DPLL tuning range only. Since the gain of the integral path is usually much smaller than the proportional path gain, the integral path can only track slow frequency changes. The amount of frequency change in the feedback divided clock F_{CKV}, that can be accumulated by the integral path over one cycle of the reference is given by $\Delta F_{K_I} = \frac{K_I K_{DCO}}{N}$. This imposes an upper limit on the reference frequency change rate. If the reference frequency changes at a rate faster than ΔF_{K_I}, the integral path slews (Fig. 2) and the phase error grows quadratically until the DPLL loses lock.

III. Improved Tracking Capability of Bang-Bang DPLLs

One way to improve the tracking range is to boost the proportional gain K_P in the DLF. However, the increased proportional step size also increases dithering jitter of the output clock. In other words, a bang-bang DPLL suffers from a direct tradeoff between the frequency tracking range and the jitter generation. An adaptive tracking technique that overcomes this tradeoff and achieves a wide tracking range without sacrificing the jitter performance is presented next. The block diagram of the proposed approach is shown in Fig. 3.

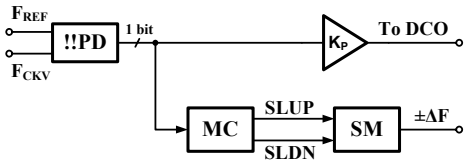

Fig. 3. Adaptive tracking mechanism.

The adaptive tracking approach works as follows: the sign bits from the bang-bang PD are stored and monitored by the monitoring circuit (MC) for the presence of a sequence of the same bits. These consecutive identical phase detector outputs indicate a large phase error resulting from the imperfect tracking of the input phase (frequency) error by the bang-bang DPLL. In such cases, the DPLL slews resulting in a large tracking jitter. If a sequence of many ones or many zeros is detected, the MC generates an SLUP or SLDN signal, respectively. Based on the SLUP and SLDN signals, the state machine (SM) (state diagram shown in Fig. 4 (a)) instantly increases or decreases the oscillator frequency by a fixed amount ΔF. By setting ΔF to be half of the frequency step of the proportional path, the tracking range improves by a factor of two (Fig. 4 (b)). Since the step size of the proportional path does not change, the jitter performance would not degrade.

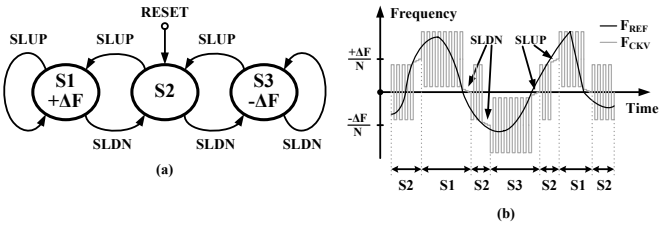

Fig. 4. Adaptive tracking mechanism: (a) state diagram of the finite-state machine, (b) frequency tracking operation.

The pull-in range of the bang-bang DPLL is limited to less than 10% of the free-running frequency of the VCO. In applications requiring a wider operating range, acquisition aids such as frequency locked loops are needed. The design of a frequency detector (similar to the one presented in [7]) that enables fast frequency-lock is the focus of the next section.

IV. Frequency Detector for Fast Frequency Lock

The key building block of an FLL is the frequency detector (FD) that determines the difference between the oscillator's divided clock F_{CKV} and the reference clock F_{REF}. There are many ways to accomplish frequency lock in digital PLLs [3], [8], [9], but all of them suffer from a major drawback - that of slow frequency acquisition. The FLL, used in the presented DPLL, utilizes a novel frequency detector [10] to obtain fast frequency acquisition. A simplified block diagram of the proposed frequency detector is shown in Fig. 5. It consists of the PLL's feedback divider, two registers, and a modulo arithmetic adder. The feedback divider in a PLL can be viewed as an asynchronous modulo-2^N counter (N is the number of divide-by-two stages), which counts DCO edges. The value of the feedback divider (counter) is sampled on each rising edge of the reference clock. Since the DCO output is not synchronous with the reference, to avoid a metastability problem, the reference clock is re-sampled with the DCO falling edge by two cascaded flip-flops. The falling (not rising) edge of the DCO has to be used to allow the divider to settle. To widen the frequency detection range, the feedback divider can have more stages ($M = 4$ in our design) than those required for the DPLL ($N = 3$ in our design). A frequency difference information is determined at each reference cycle, which ensures fast frequency lock. A stability analysis for the FLL was performed using a z-domain representation [10]. The FLL is stable when the condition $0 < K_{DCO} < 2F_{REF}$ is satisfied, where K_{DCO} is the oscillator gain.

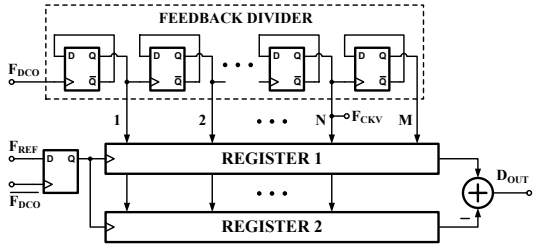

Fig. 5. Frequency detector for fast frequency lock.

V. Overall DPLL Architecture

The block diagram of the proposed DPLL architecture is shown in Fig. 6. It consists of two loops: an FLL and a PLL. On power-up only the FLL is active. The frequency detector (FD) determines the frequency difference and provides it as an input to the accumulator (ACC) in digital format (D_{OUT}). The output of ACC controls the frequency of a digitally controlled oscillator (DCO) via a 10-bit current mode digital-to-analog converter (DAC), which allows for a wide tuning range. The lock detector (LD) detects when the frequency lock is acquired, and then deactivates the FLL and activates the PLL. The sign of the phase-frequency difference in the PLL is determined by a bang-bang phase-frequency detector (!!PFD) that consists of a conventional PFD followed by a sampling D flip-flop. The one-bit digital output of the bang-bang PFD is filtered by a digital loop filter (DLF), which consists of proportional and integral paths with gains K_P and K_I, respectively. The proportional path drives the DCO directly through a high-speed path consisting of only a 1-bit DAC (PDAC). In order to improve the tracking range of the DPLL, a phase-frequency error monitoring circuit (MC) and a state machine (SM) have been incorporated in parallel with the DLF.

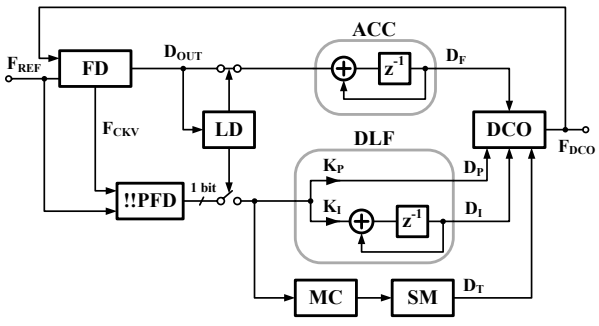

Fig. 6. Block diagram of the proposed DPLL.

The FLL accumulator output D_F, the PLL digital loop filter outputs D_P and D_I, and the SM output D_T are interfaced to the analog voltage controlled oscillator (VCO) through a set of DACs as depicted in Fig. 7. The FLL DAC is composed of a 10-bit thermometer-coded current steering DAC (FDAC) whose output current is converted to a control voltage V_{FLL} by the active biasing circuit shown in Fig. 7. Thermometer-coding in the DAC guarantees a monotonic digital-to-frequency characteristic of the DCO. The gain of the DCO FLL control is 1.5MHz/LSB, resulting in a frequency tuning range of about 1.5GHz.

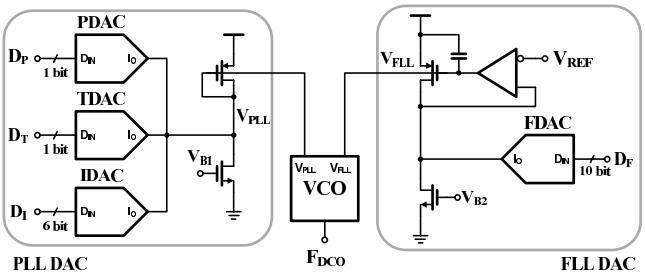

Fig. 7. Digitally controlled oscillator.

The fast-proportional control D_P, adaptive tracking control D_T, and the integral control D_I are interfaced to the VCO by a 1-bit proportional DAC (PDAC), a 1-bit tracking DAC (TDAC), and a 6-bit integral DAC (IDAC), respectively. The IDAC is implemented by a thermometer-coded current steering architecture to achieve guaranteed monotonicity. As illustrated in Fig. 7, a fast addition of the three control paths is achieved through current summing at the output of the DACs. The gain of the proportional and tracking controls is equal to 5MHz, while that of the integral path is 0.3MHz/LSB.

The VCO itself is implemented as a four stage ring oscillator. Pseudo-differential current-starved inverters used as delay cells in the VCO have two control inputs (V_{PLL} and V_{FLL}) and provide rail-to-rail swing.

VI. Experimental Results

The prototype IC was fabricated in a $0.13\mu m$ CMOS technology. To test the tracking range of the DPLL, the reference clock was sinusoidally modulated: $F_{REF}(t) = F_{REF} + A_{MOD}\, sin(2\pi\, F_{MOD}\, t)$. The modulating frequency F_{MOD} was swept from 10kHz to 1MHz and the maximum tolerable amplitude of modulation A_{MOD} was determined and is shown in Fig. 8. As seen from this figure, the tracking range of the DPLL was improved by a factor of two due to the proposed adaptive tracking technique. As a reference, SATA specifications [6] are shown in the figure with a triangular symbol. A separate measurement to compare the adaptive tracking to the more obvious case of a larger proportional step size is performed. In this measurement, the proportional step is increased until the SATA specification is met and the measured clock jitter increased from 13.1ps rms (Fig. 9) to 17.5ps rms. On the other hand, the adaptive tracking loop achieves the same frequency tracking range without any degradation of the clock jitter. Fig. 10 shows the locking behavior of the FLL with the new frequency detector. The FD locks the frequency from 1GHz to 1.6GHz within one LSB of 1.5MHz in about $4\mu s$. The measured locking behavior is in very good agreement with data from a behavioral simulation of the FLL. Fig. 11 shows the die micrograph. The test chip consumes 15.7mW of power while operating at 1.6GHz and occupies $0.27mm^2$

of area. The performance summary of the DPLL is presented in Table I.

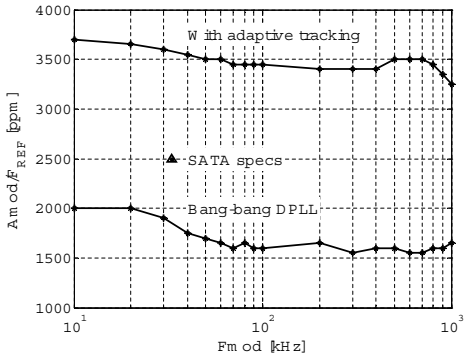

Fig. 8. DPLL input modulation tolerance.

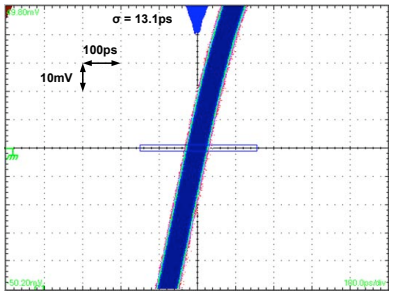

Fig. 9. DPLL jitter.

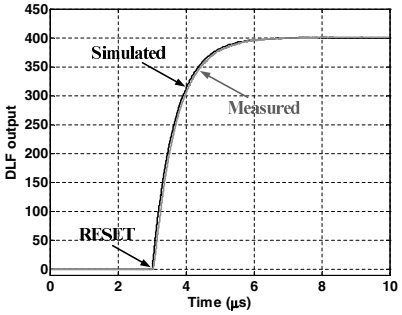

Fig. 10. Frequency locking behavior of the DPLL.

VII. Conclusion

In this work, a digital PLL is presented that employs an adaptive tracking technique and a novel frequency acquisition scheme to achieve a wide tracking range and fast frequency acquisition. The proposed adaptive frequency tracking technique decouples the jitter versus tracking range trade-off. A new frequency detector allows for a fast frequency lock of phase-locked loops. The proposed frequency detector provides frequency difference information at each reference cycle, and thus guarantees fast frequency acquisition. The frequency detector can be implemented by using standard logic available in any process, and, therefore, is suitable for digital as well as for analog PLLs.

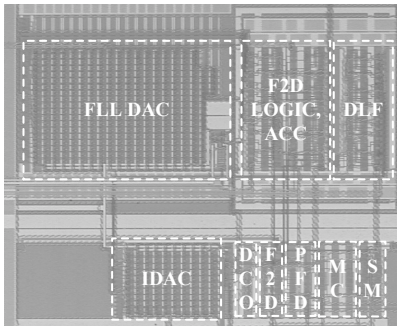

Fig. 11. Die micrograph.

TABLE I
DPLL PERFORMANCE SUMMARY.

Reference frequency	200MHz
Frequency range	0.6GHz to 2GHz
Feedback divider ratio	8
Power dissipation	15.7mW
RMS jitter @ 1.6GHz	13.1ps
Fabrication process	0.13μm CMOS
Die area	0.27mm^2

VIII. Acknowledgments

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