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MIXED SIGNAL LETTER

A 0.8-V 816-nW delta–sigma modulator for low-power biomedical applications

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Abstract This letter discusses the implementation of a low-voltage, low-power delta–sigma modulator as a sensing stage for biomedical applications. A distributed feed-forward structure and bulk-driven operational transconductance amplifier are used in order to achieve efficient operation at a supply voltage of 0.8 V. Instead of conventional low-voltage amplifier architectures, our design uses folded-cascode amplifiers, although they are not used in most low-voltage circuits. A wide input swing is achieved by using the bulk-driven approach, and the drawback of the limited voltage swing of the cascoded output stage is overcome by the distributed feed-forward modulator. The designed modulator has a dynamic range of 49 dB at a 0.8-V supply voltage and consumes only 816 nW of power for the 250-Hz bandwidth. The core chip size of the modulator is 1000 μm × 500 μm by using the 0.18-μm standard CMOS process.

Keywords Delta–sigma modulator · Switched-capacitor circuit · Biomedical circuit · Oversampling · Analog-to-digital converter (ADC) · Analog circuit design

1 Introduction

In modern biomedical systems, analog-to-digital converters (ADCs) are an important building block in digitizing sensed analog signals. Due to the increasing demand for implantable devices for the human body, low-power circuits are essential. One such biomedical device is the pacemaker, which detects and assists the heart's natural electrical activity. A pacemaker receives information regarding the heart's status, including the heart rate and rhythm, from pacing leads that are inserted into the heart. A pacemaker is also able to detect various heart irregularities [1–3].

The delta–sigma modulator appears to be adequate for the sensing stage because it is able to deliver a relatively high dynamic range for low signal bandwidth with a low power consumption. The high signal-to-noise ratio (SNR) achieved by the delta–sigma modulator enables effective detection of the cardiac signal. In our design, the bulk-driven approach [4–6] is used to apply the input signal to the bulk, rather than to the transistor gate, thereby effectively resolving the problems associated with the low 0.8-V supply and the decreasing overall power consumption of the modulator.

2 Delta–sigma architecture

Figure 1 shows the topology used in this letter. The designed modulator is a distributed feed-forward third-order delta–sigma structure that consists of three switched-capacitor integrators. The most significant factor that distinguishes the feed-forward delta–sigma modulator structure from its feedback counterpart is that the input signal is directly fed into the 1-bit quantizer via the feed-forward path, and only the quantization noise element is processed in the loop filter of the modulator [7, 8].

Consequently, the feed-forward structure can substantially restrain the distortion component, provided that the amplifier gain is 30 dB or higher [9]. This structure is more suitable for a bulk-driven approach because the bulk-driven circuit has a relatively lower gain than gate-driven circuit.

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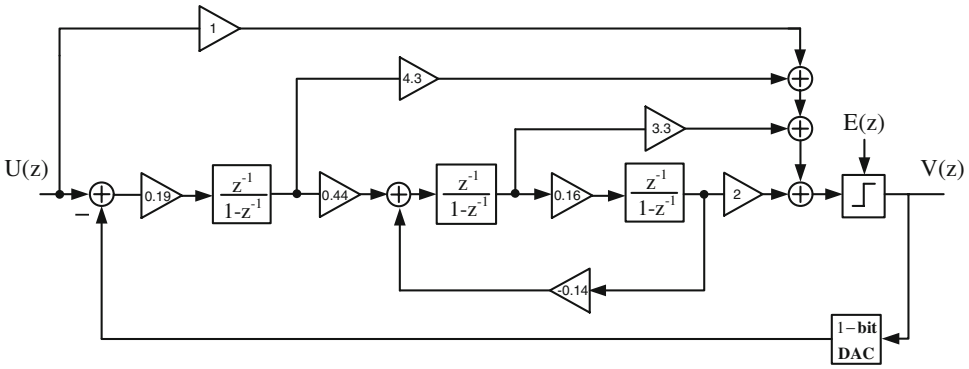

Fig. 1 Distributed feed-forward delta–sigma modulator

Despite the low-voltage operation, we used folded-cascode amplifiers, as explained in the next section, to increase the gain by maximizing output impedance with the inevitable low transconductance of the bulk-driven architecture.

3 Circuit implementation

3.1 Bulk-driven OTA

The most critical part of the low-voltage OTA is the input stage, the MOSFET of which must be turned on for signal processing. The bulk-driven approach is used to implement an OTA that operates at 0.8-V supply voltage. The most significant advantage of the bulk-driven approach is that there is no limitation on threshold voltage, which enables a low-voltage input stage of the amplifier.

The bulk-driven approach has a few disadvantages, the most important of which is that the body transconductance g_{mb} is 3–4 times smaller than the general gate transconductance g_m. Accordingly, the DC gain value and the bandwidth are relatively low compared to the gate-driven approach [10].

Figure 2 shows the designed amplifier structure, which is the folded-cascode differential OTA, designed by using the bulk-driven approach. As explained earlier, the input signal is applied to the bulk in order to remove the restriction otherwise created by the threshold voltage and to provide a wide input common-mode range. The ground level at the gates of the input stage supplies sufficient DC bias voltage to turn on the transistors.

The bulk-driven OTA would have higher input-referred noise power than gate-driven architecture due to the low transconductance of the input differential pair. The dynamic range (DR) of the OTA is calculated by the ratio between of the input signal power to the noise power, as shown below.

$$\mathrm{DR}_{\mathrm{input}} = 10\log\frac{P_{\mathrm{signal}}}{P_{\mathrm{thermal}} + P_{\mathrm{flicker}}}. \quad (1)$$

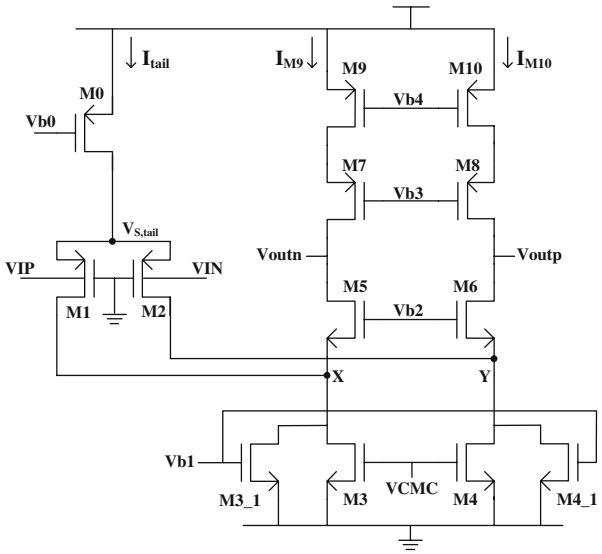

Fig. 2 Fully-differential folded-cascode operational transconductance amplifier

The thermal noise and the flicker noise power of the OTA is calculated by using HSPICE noise simulation and the input signal power is calculated by assuming the maximum input amplitude of 0.4 V. The DR of the designed OTA is calculated as 59.7 dB, which shows sufficient margin for our specifications. The leakage current of the input transistor is also simulated to detect any unexpected behavior. Table 1 shows the leakage current for the process and temperature corners in a static DC condition. As can be seen, the leakage current is about 3.12 pA in the worst case, and this does not affect the operation of the amplifier.

Table 2 shows simulation results of the first OTA with an effective load capacitance of C_{Leff} [11]. The OTA gain is 45 dB, the unity gain frequency is 49 kHz, and the phase margin is 90°. These results indicate that the OTA provides satisfactory performance to operate the modulator. The other OTAs have the same architecture, with a reduced current and performance to reduce power consumption.

Table 1 Leakage current of input transistors

Corner	−45°C	27°C	110°C
NN	8.22e-23	6.4e-18	5.06e-13
SS	1.34e-21	6.13e-17	3.12e-12
FF	1.02e-23	9.67e-19	1.27e-13
SF	1.27e-23	9.67e-19	1.51e-13
FS	9.92e-22	4.77e-17	2.52e-12

Table 2 First OTA circuit performance

Parameter	OTA
Supply voltage	0.8 V
DC gain	45 dB
Phase margin	90°
Unity gain frequency	49 kHz
Effective load capacitor (C_{Leff})	680 fF
Power consumption	400 nW
Process	0.18 μm
PMOS V_{th}	450 mV
NMOS V_{th}	430 mV

3.2 Switched-capacitor modulator

Figure 3 shows the overall circuit diagram of the switched-capacitor delta–sigma modulator described here. The OTA used in each integrator employs the bulk-driven approach. A dual reference DAC is used, with the VDD and the ground set as the positive and negative references, respectively, to eliminate the need to establish a separate reference voltage. For proper operation of MOS switches, a charge pump circuit is used for high-voltage generation [12].

4 Experimental results

Figure 4 shows a microphotograph of the designed chip. The circuit is fabricated by using the 1-poly 4-metal 0.18-μm process. The size of the core chip, excluding the bonding pads, is 1000 μm × 500 μm. In the layout, the

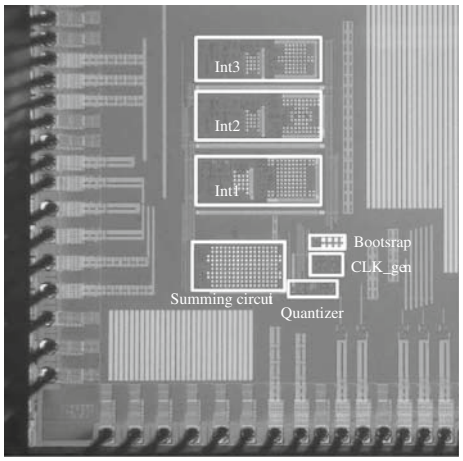

Fig. 4 Chip microphotograph

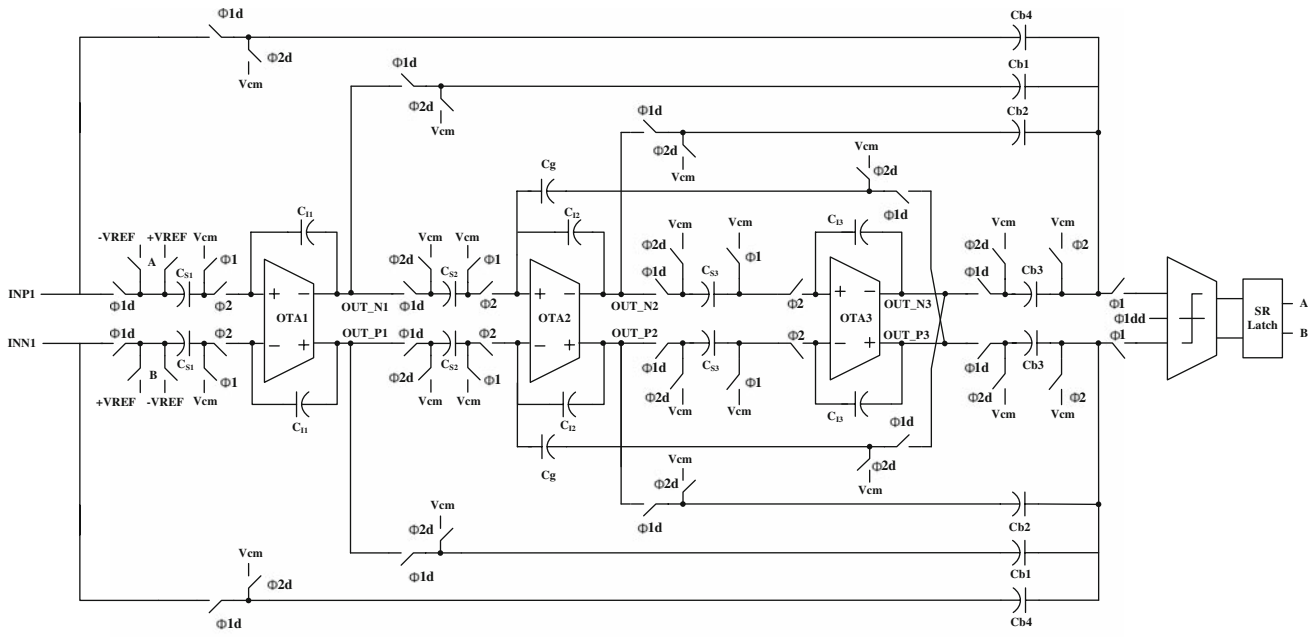

Fig. 3 1-bit third-order switched-capacitor delta–sigma modulator

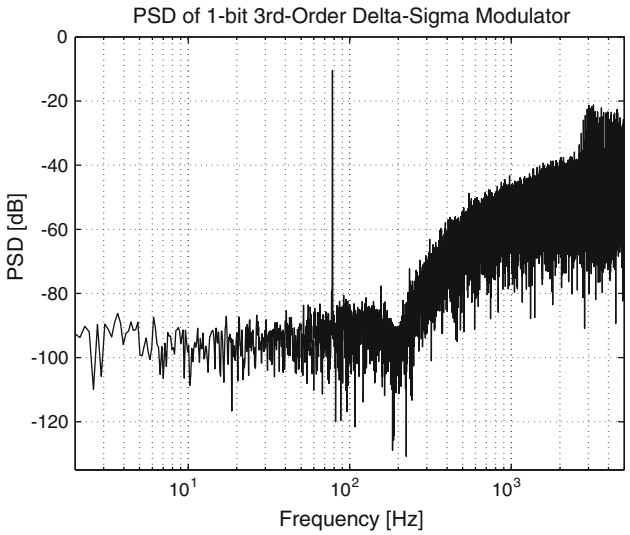

Fig. 5 Measured output spectrum

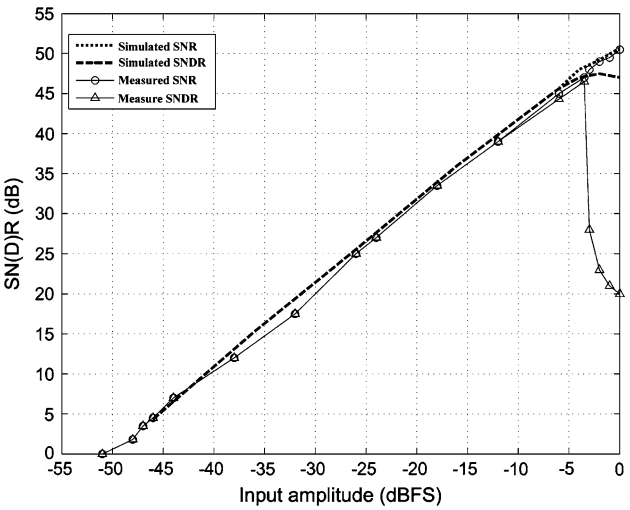

Fig. 6 Simulated and measured SNR and SNDR

analog and the digital blocks are separated so that the sensitive analog blocks are not affected by digital noise.

Figure 5 shows an FFT plot of the digital output from the fabricated chip. The number of samples is 65,536. The designed delta–sigma modulator operates for the 250-Hz signal bandwidth at a 10-kHz clock frequency. The input signal frequency was determined to be 80.125 Hz to observe the third harmonic component in the signal band, and it has a magnitude of −4 dB.

Figure 6 shows both the simulated and the measured results. In order to obtain an accurate simulation output, the nonidealities of the circuit are modeled in Matlab/Simulink [13]. The OTA's DC gain, unity gain bandwidth, slew rate, output signal swing, and thermal noise are all included in the behavioral models. The KT/C noise of the input sampling capacitor is also included in the behavioral simulation. The measured results are close to the simulated results, but do not match as the input signal level increases above −5 dB, with 0 dB defined as a voltage level of 0.25 V here. Significant harmonic components are observed for the large input amplitudes during the measurements.

After careful analysis, it is estimated that the parasitic capacitance at the input of the OTA causes delayed settling of the input differential pair, which would be a virtual ground node in an ideal situation. This effect is not modeled in the current version of Matlab/Simulink [13]. Figure 7 shows the HSPICE simulation results with and without the parasitic capacitance of 50 fF. Even though it would not be easy to completely remove these distortions due to our extremely low-power design target, it is expected that the performance could be improved by using a careful layout that minimizes parasitics.

The power is measured as 816 nW, the SNR as 48.46 dB, and the SNDR as 48.19 dB. The measurement results are summarized in Table 3.

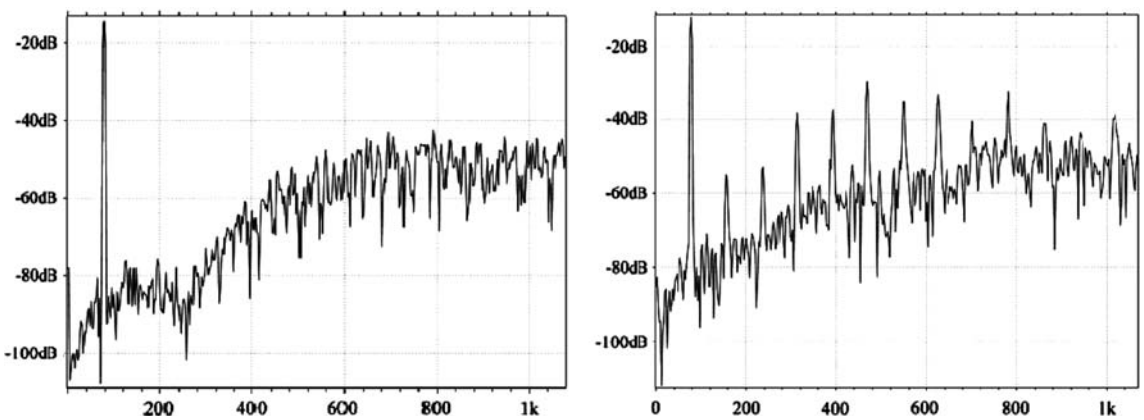

Fig. 7 Simulated output spectra without and with a parastic capacitor

Table 3 Performance summary

Supply voltage	0.8 V
Power consumption	816 nW
Peak SNR	50.2 dB
Dynamic range	49 dB
Sampling frequency	10 kHz
Signal bandwidth	250 Hz
Oversampling ratio	20
Core size	0.5 mm^2

5 Conclusion

This letter demonstrates a delta–sigma modulator for use in biomedical systems. A distributed feed-forward structure is used to implement a delta–sigma modulator that operates at a supply voltage of 0.8 V. We have employed folded-cascode architecture and demonstrated that the cascode device can be suitable for such applications when coupled with a well-optimized modulator architecture. The disadvantage of cascoding is overcome by the low voltage swing of the feed-forward structure. Power consumption of the overall delta–sigma modulator is 816 nW for the 250-Hz bandwidth, which is expected to substantially improve the battery duration for implantable low-power systems. It is expected that these achievements can be fully utilized in biomedical applications such as in cardiac pacemakers.

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