A 0.9-V Input Discontinuous-Conduction-Mode Boost Converter With CMOS-Control Rectifier

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***Abstract*—A 0.9-V input discontinuous-conduction-mode (DCM) boost converter delivering 2.5-V and 100-mA output is presented. A novel low-voltage pulse-width modulator is proposed. The modulator can be directly powered from the 0.9-V input instead of using the 2.5-V output as in general modulator designs. Sophisticated low-voltage analog blocks, which normally consume a large amount of power and chip area, are not required in the modulator. The impact of output-voltage ripple and transient-induced output-voltage perturbation on the operation of analog blocks inside the modulator is eliminated. Boost converter start-up sequence is also greatly simplified. A CMOS-control rectifier (CCR) is also proposed to improve converter power efficiency. The CCR is used to replace the conventional rectifying switch to provide adaptive dead-time, which helps to minimize charge-sharing loss and body-diode conduction loss. Corresponding thermal stress on the rectifying switch is hence minimized. The CCR also enables the use of small off-chip inductor and capacitor at sub-MHz switching frequency to improve light-load efficiency. This converter has been implemented in a 0.35-μm CMOS process. It is designed to operate at $\sim$667 kHz with a 1 μH inductor and 4.7 μF output capacitor to reduce both switching loss and form factor. Experimental results prove that the converter can be directly powered from 0.9-V input with $\sim$85% efficiency at 100-mA output.**

***Index Terms*—Sub-1V, boost converter, discontinuous-conduction mode, adaptive dead-time.**

I. Introduction

COMPACT size and long battery life are both required in today's battery-powered mobile systems. One of the effective solutions to reduce their size is the use of single-cell battery in which the commonly used nickel-based battery (e.g., NiMH) has minimum output voltage equal to $\sim$0.9 V. As most analog circuits are still operated at a supply voltage much larger than 1 V, for example audio amplifiers [1], [2], a boost converter is required to step up this sub-1V battery voltage to higher level. However, designing a sub-1V input boost converter with high power efficiency and small off-chip components is not trivial. One of the difficulties is the design of pulse-width modulator in which the sub-1V input voltage limits the available voltage swing and hence forces the use of sophisticated low-voltage analog circuits [3], which normally consumes more power and chip area. Even though the modulator can be powered from the boost converter output [3], [4], the modulator, especially the analog blocks, become highly sensitive to the ripple and the transient-induced perturbation at the converter output. Start-up circuits and carefully designed start-up sequence are also required as the modulator cannot be operated until the converter output is ready. Another design difficulty is the strong tradeoff between the power efficiency and the size of off-chip components. Inductor is normally the one consuming the most board space. Its size can be reduced by the use of small-value inductor. However, this makes the continuous-conduction-mode (CCM) converter operate at several MHz [5], [6] or even at tens to thousands MHz [7]–[9], which increases the switching loss and hence inevitably degrades the converter light-load efficiency.

In this work, as illustrated in Fig. 1, both a novel sub-1V pulse-width modulator and a CMOS-control rectifier (CCR) [10] are proposed to enable a 0.9-V input discontinuous-conduction-mode (DCM) boost converter with small off-chip components and high power efficiency. The proposed modulator can be directly powered from the 0.9-V input without the use of sophisticated low-voltage analog circuits. The problems associated with modulator powered from the converter output no longer exist. The proposed CCR helps to improve converter efficiency in different ways. It replaces the conventional rectifying switch to provide an adaptive dead-time, which reduces the charge-sharing loss and the body-diode conduction loss. The reduced body-diode loss helps to minimize the power dissipation and the corresponding thermal stress on the rectifying switch. Its diode-like characteristic facilitates the converter operate in DCM, which enables the use of small value inductor at moderate switching frequency (e.g., hundreds of kHz) such that switching loss is reduced.

This paper is organized as follows. Operation and design of the proposed modulator are thoroughly discussed in Section II. In Section III, relationship between dead-time and charge-sharing and body-diode conduction loss is first introduced. Then, design of CCR to provide an adaptive dead-time is presented in detail. Experimental results and discussions are shown in Section IV. Finally, conclusions are given in Section V.

II. Proposed Low-Voltage Pulse-Width Modulator

The ability of proposed modulator to directly operate at 0.9-V input comes from the method to generate the pulse-width-modulation (PWM) signal. Before introducing the proposed modulator, limitation of conventional modulator to operate at sub-1V

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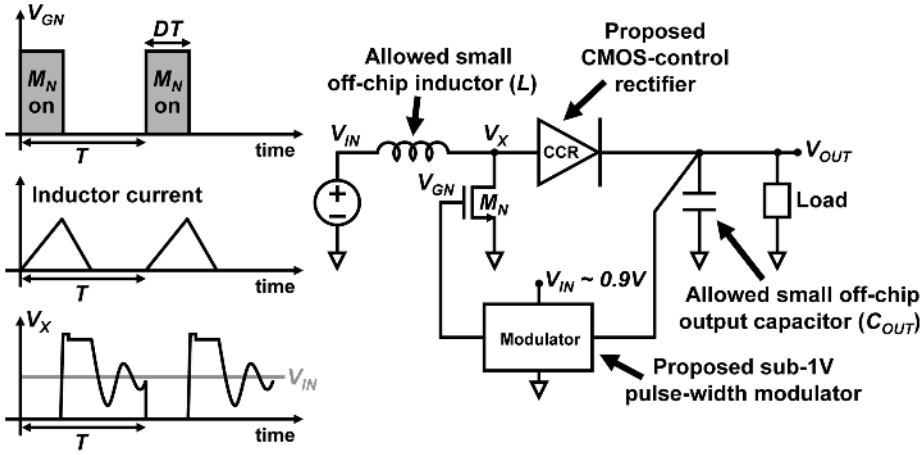

Fig. 1. Simplified schematic and timing diagram of a boost converter with both the proposed CMOS-control rectifier and the proposed sub-1V pulse-width modulator.

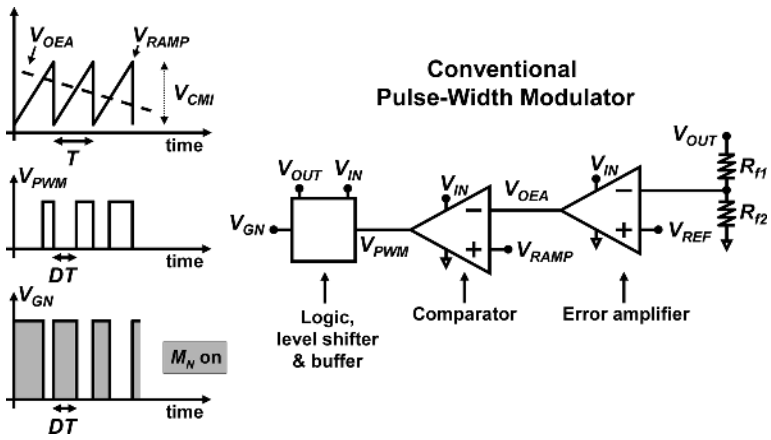

Fig. 2. Block-level schematic and timing diagram of conventional pulse-width modulator.

input is first described. Fig. 2 shows the block-level schematic and the timing diagram of conventional modulator. The PWM signal $(V_{\rm PWM})$ is generated by a comparator that compares the error amplifier output $(V_{\rm OEA})$ with a fixed amplitude ramp $(V_{\rm RAMP})$. Duty cycle (D) of the $V_{\rm PWM}$ is controlled by the voltage level of $V_{\rm OEA}$ as illustrated in Fig. 2. In order for the comparator to generate the $V_{\rm PWM}$ with wide range of duty cycle (e.g., ~1% to ~99%), the comparator is required to have proper operation at different input voltage such as different values of $V_{\rm OEA}$. In other words, the comparator used in the conventional modulator must have its common-mode-input voltage $(V_{\rm CMI})$ equal to at least the amplitude of $V_{\rm RAMP}$. However, the $V_{\rm CMI}$ is greatly reduced when the supply voltage $(V_{\rm IN})$ is scaled down. Assuming the comparator is implemented with a simple nMOS input stage. The $V_{\rm CMI}$ can be expressed by (1)

$$V_{\rm THN} + V_{\rm OVN1} + V_{\rm OVN2} < V_{\rm CMI} < V_{\rm IN} + V_{\rm THN} - |V_{\rm THP}| - |V_{\rm OVP}| \quad (1)$$

where $V_{\rm OVN1}$ and $V_{\rm OVN2}$ are the overdrive voltage of the nMOS input transistor and the nMOS tail-current transistor of the nMOS input stage, correspondingly. $V_{\rm OVP}$ is the overdrive voltage of the pMOS transistor. $V_{\rm THN}$ and $V_{\rm THP}$ are the threshold voltages of the nMOS and pMOS transistor, respectively. It is found that the $V_{\rm CMI}$ is ~50 mV at 0.9-V $V_{\rm IN}$ when the comparator is designed in a 0.35- μm CMOS process where $V_{\rm THN}$ is ~550 mV, $V_{\rm THP}$ is ~700 mV, and $V_{\rm OVN1}, V_{\rm OVN2}$, and $V_{\rm OPV}$, are designed to ~50 mV. As a ramp signal with ~50 mV amplitude is relatively difficult to produce and sensitive to noise, sophisticated comparator with wide or even rail-to-rail $V_{\rm CMI}$ is required.

In contrast to the conventional modulator, the $V_{\rm PWM}$ in the proposed sub-1V modulator is generated by a comparator that compares a fixed DC voltage $(V_{\rm DC})$, which is generated by on-chip circuit that is powered from 0.9-V $V_{\rm IN}$, to a ramp with variable amplitude $(V_{\rm RVA})$. As illustrated in Fig. 3, duty cycle of the $V_{\rm PWM}$ is now controlled by the amplitude of $V_{\rm RVA}$. The comparator in the proposed modulator is therefore able to produce the $V_{\rm PWM}$ with wide range of duty cycle at fixed input voltage that is defined by the $V_{\rm DC}$. Significance of the proposed modulator is that once the $V_{\rm DC}$ is designed within the common-mode-input-voltage range of a comparator, very simple comparator design can be used at 0.9-V $V_{\rm IN}$ to produce the $V_{\rm PWM}$ with wide range of duty cycle without encountering any problems. Moreover, as compared to the conventional modulator, operation of the proposed modulator is no longer affected by the amplitude of the ramp signal such as the amplitude of $V_{\rm RVA}$.

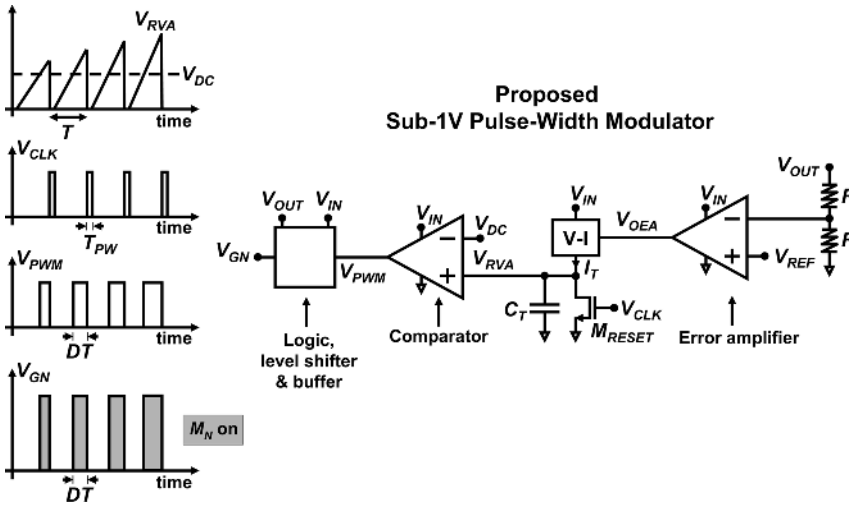

Fig. 3. Block-level schematic and timing diagram of the proposed sub-1V pulse-width modulator.

The $V_{\rm RVA}$ is generated by a voltage-to-current (V-I) converter, a timing capacitor (C_T) and a reset transistor $(M_{\rm RESET})$. The $M_{\rm RESET}$ is used to fully discharge the C_T at the beginning of each switching cycle. The switching period (T) is defined by the periodic clock signal $(V_{\rm CLK})$ with very small pulse-width $(T_{\rm PW})$. The amplitude of $V_{\rm RVA}$ is controlled by the $V_{\rm OEA}$ such that duty cycle of $V_{\rm PWM}$ can be adjusted by negative feedback to regulate the output voltage of the boost converter $(V_{\rm OUT})$.

In the following subsections, design of different blocks inside the proposed modulator is discussed. Start-up of sub-1V input boost converter with the proposed modulator is also presented.

A. Design of Error Amplifier and Comparator

Design of both the error amplifier and the comparator is based on the NMOS-input current-mirror amplifier topology. The only difference between them is that inverter chain is used in the comparator as output buffer. To make sure both of them are operated in the high-gain region, the $V_{\rm DC}$ and the reference voltage $(V_{\rm REF})$ applied to their inverting-input terminals are designed according to (1). The required $V_{\rm REF}$ under sub-1V input can be generated by different bandgap circuits [11]–[13]. Once the $V_{\rm REF}$ is defined, ratio between feedback resistors (R_{f1} and R_{f2}) can be designed with (2):

$$\frac{R_{f1}}{R_{f2}} = \frac{V_{\rm OUT}}{V_{\rm REF}} - 1 \qquad (2)$$

To minimize the finite-gain offset, gain of the error amplifier and the comparator can be improved by using transistors with channel length larger than the minimum feature size of a given CMOS technology.

B. Design of V-I Converter, Timing Capacitor and Reset Transistor

Fig. 4 shows the transistor-level schematic and the timing diagram of the proposed V-I converter that is constructed by one current source (I_B) and five MOS transistors (M_{VI1} to M_{VI5}). The current source I_B defines the maximum charging current $(I_{\rm MAXCH})$ to the timing capacitor C_T, which is implemented by on-chip PIP (polysilicon–insulator–polysilicon) capacitor. Transistors M_{VI1} and M_{VI2} operate as conventional common-source differential pair that is used to control the current going into C_T based on the input-voltage difference ($V_{\rm OEA}$ - $V_{\rm BIAS}$) where $V_{\rm BIAS}$ is generated by on-chip circuit that is powered from 0.9-V $V_{\rm IN}$. A current mirror formed by transistors M_{VI3} and M_{VI4} is used to mirror the current of M_{VI1} to the output of V-I converter. The relationship between the V-I converter output current (I_T) and the input voltage difference is the same as the conventional common-source pair [14]. Transistor M_{VI5} is used to make the drain-to-source voltage of both M_{VI1} and M_{VI2} into very close proximity so that the offset voltage of V-I converter can be reduced. The voltage $V_{\rm BIAS}$ should be designed according to (1) to make sure all transistors are in saturation region. Overdrive voltage of transistor M_{VI1} and M_{VI2} should be designed to a small value such that the differential pair can be properly operated at sub-1V supply. Simplicity of proposed V-I converter also eliminates the need of on-chip compensation capacitor required in [3], tradeoff between stability and response time is hence no longer existed in the proposed design.

The aspect ratio of reset transistor $M_{\rm RESET}$ should be designed to a large value to make sure that the timing capacitor C_T can be fully discharged within the turn-on time of $M_{\rm RESET}$ (e.g., $T_{\rm PW}$), which is very short in time compared to the whole switching period T. The value of timing capacitor C_T should be designed to a value much larger than the parasitic capacitance at the $V_{\rm RVA}$ node, which is mainly contributed by the drain capacitance of $M_{\rm RESET}$, the input capacitance of the comparator, and the output capacitance of the V-I converter. The value of C_T is 2.5 pF in this design. The ramp rate of $V_{\rm RVA}(\sim I_T/C_T)$ can hence be controlled by adjusting the magnitude of I_T. On-time of nMOS power transistor (*DT*) can be well approximated by using the fact that $T_{\rm PW}$ is much shorter in time than the switching period T. With the help of Fig. 3, expression of *DT* can be easily derived and is shown in (3)

$$DT \approx T - \frac{V_{\rm DC} \cdot C_T}{I_T}. \qquad (3)$$

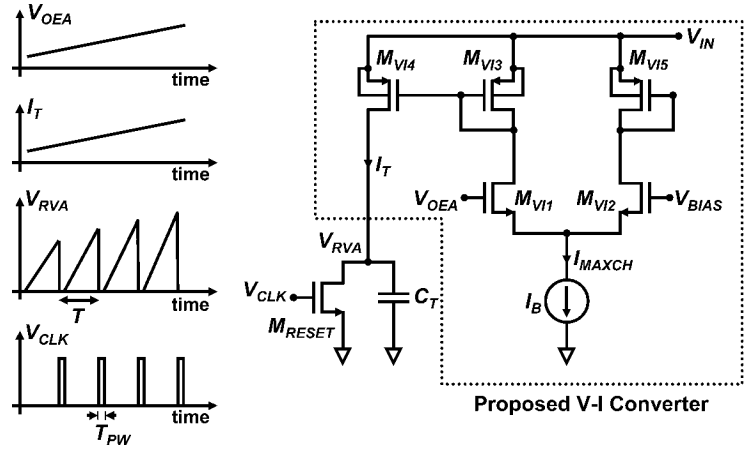

Fig. 4. Transistor-level schematic and timing diagram of the proposed V-I converter.

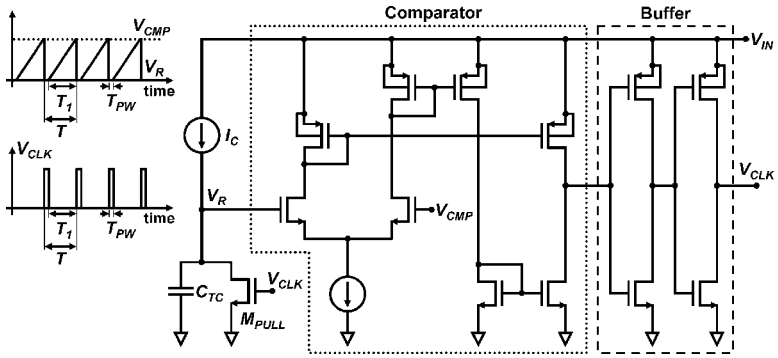

Fig. 5. Transistor-level schematic and timing diagram of clock signal generator.

As the nMOS power transistor (M_N) of the boost converter cannot be turned on for the whole switching period T, there should be a maximum on time, or in other words, a maximum duty cycle $(D_{\rm MAX})$. It can be obtained by designing the tail current $I_{\rm MAXCH}$ of the V-I converter. The required $I_{\rm MAXCH}$ for a given $D_{\rm MAX}$ can be calculated by

$$I_{\rm MAXCH} = V_{\rm DC} \cdot \frac{C_T}{T \cdot (1 - D_{\rm MAX})}. \tag{4}$$

Dependence of the duty cycle variation (δD) on the change of error amplifier output voltage $(\delta V_{\rm OEA})$ can be expressed by

$$\frac{\delta D}{\delta V_{\rm OEA}} = \frac{1}{2} g_{m\_VI2} \frac{T \cdot (1 - D)^2}{V_{\rm DC} \cdot C_T} \tag{5}$$

where g_{m_VI2} is the transconductance of transistor M_{VI2} of the V-I converter. It can be observed that the maximum value of $\delta D/\delta V_{\rm OEA}$ is occurred at zero duty cycle.

C. Design of Clock Signal Generator

Fig. 5 shows the transistor-level schematic and the timing diagram of the clock signal generator, which consists of a current source (I_C), another timing capacitor $(C_{\rm TC})$, a pull-down transistor $(M_{\rm PULL})$, a current-mirror comparator with NMOS-input stage and a buffer. The switching period T of $V_{\rm CLK}$ comprises two periods of time (T_1 and $T_{\rm PW}$). The first period of time T_1 is the time required to charge the timing capacitor $C_{\rm TC}$ from zero volt to the threshold $(V_{\rm CMP})$. The second period of time $T_{\rm PW}$, as mentioned before, is the pulse-width of the clock signal $V_{\rm CLK}$ that is defined by both the response time of the comparator and the propagation delay of the buffer. As $T_{\rm PW}$ is usually much smaller than the switching period T, the aspect ratio of pull-down transistor $M_{\rm PULL}$ should be large enough to make sure the timing capacitor $C_{\rm TC}$ is fully discharged within the period of $T_{\rm PW}$. Moreover, the switching period T can be approximated to the time T_1 and expressed as

$$T \approx \frac{V_{\rm CMP} \cdot C_{\rm TC}}{I_C}. \tag{6}$$

The threshold voltage $V_{\rm CMP}$ should be designed according to (1) to make sure all transistors of the comparator operating in saturation region.

D. Design of Supply-Voltage Multiplexer, Level Shifter and Tapered Buffer

To improve power efficiency and reduce chip area of the converter, the tapered buffer used to drive the nMOS power transistor is preferred to be powered from the 2.5-V boost converter output rather than its 0.9-V input such that the size and the conduction loss of nMOS power transistor are reduced. When 2.5 V instead of 0.9 V is used to drive the nMOS power transistor, under the same conduction loss, transistor size can be reduced by almost 6X in this design. This transistor size reduction not only significantly reduces the size of entire converter but also helps to reduce the power loss and the gate-drive delay

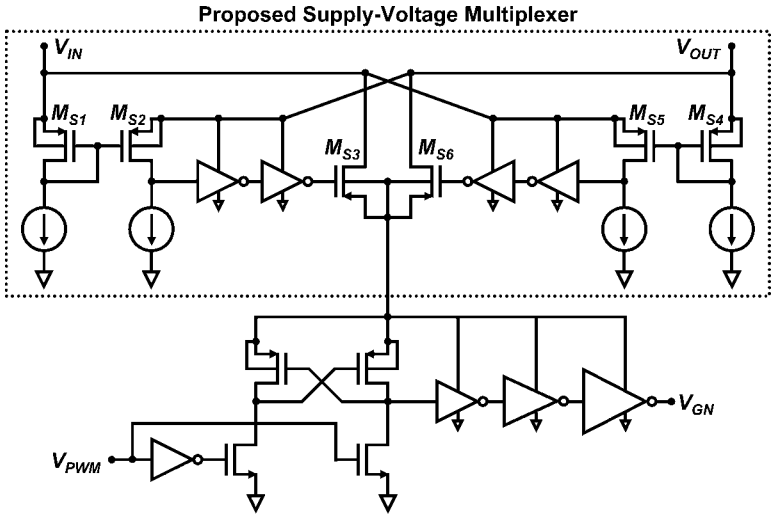

Fig. 6. Transistor-level schematic of the proposed supply-voltage multiplexer, and the conventional level shifter and tapered buffer.

caused by parasitic elements associated with the metal used by such large-size power transistor. Even this scheme gives ~1.3X increase in switching loss, almost 6X power transistor size reduction is the key to reduce chip area such that the size of entire boost converter can be small enough to fit into the recent size-constrained mobile systems. This can be achieved by using a conventional level shifter to shift the logic-one level of PWM signal $V_{\rm PWM}$ from 0.9 V to 2.5 V. As the converter output is not ready during start-up, a supply-voltage multiplexer (SVMUX) is introduced here to make sure the level shifter and the tapered buffer can be supplied from the 0.9-V input at start-up. Fig. 6 shows the transistor-level schematic of the proposed SVMUX, and the conventional level shifter and tapered buffer. The SVMUX consists of two comparators, where each of them is constructed by two constant current sources and two matched pMOS transistors, M_{S1} and M_{S2}, and M_{S4} and M_{S5}, acted as current mirrors. Outputs of these two comparators are buffered to drive the transistors M_{S3} and M_{S6}, which are used to connect either the input or the output of converter to the supply-rail of both the level shifter and the tapered buffer. When the converter output is not ready (e.g., $V_{\rm OUT} < 0.9$-V input), transistor M_{S3} is on and transistor M_{S6} is off so that both the level shifter and the tapered buffer are powered from the 0.9-V input. Once the converter output is close to 0.9 V during start-up, both transistors M_{S3} and M_{S6} are on. Both the converter input and output are hence connected through the small transistor-turn-on resistance to the supply-rail of the level shifter and tapered buffer. When the converter is ready (e.g., $V_{\rm OUT}$~2.5 V), transistor M_{S3} is off and M_{S6} is on. The level shifter and tapered buffer are then powered from the 2.5-V output. To prevent the input and the output of the converter connecting through the body diodes of transistors M_{S3} and M_{S6}, both the converter input terminal $V_{\rm IN}$ and the output terminal $V_{\rm OUT}$ are connected to the drain terminals but not the source terminals of transistors M_{S3} and M_{S6} as shown in Fig. 6. Moreover, size of transistors M_{S3} and M_{S6} are designed to make their turn-on resistance small enough such that enough current can be sourced by the tapered buffer to drive the nMOS power transistor.

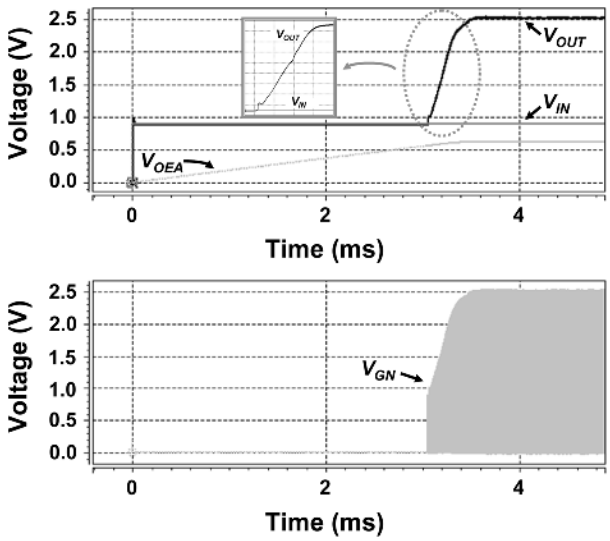

Fig. 7. Simulated start-up response of a sub-1V boost converter with the proposed modulator.

E. Start-Up of Sub-1V Modulator

The proposed modulator eliminates the need of special start-up circuits and sequence that are required in existing sub-1V boost converter designs [3], [4]. This is because all building blocks inside the proposed modulator can directly operate at sub-1V input. As a result, start-up circuit such as low-voltage oscillator used to firstly boost the converter output voltage in open-loop manner is not required. Moreover, decision circuit, which is used to switch the modulator from open-loop to closed-loop operation when the converter output is larger than certain predefined value, is no longer required.

Soft-start to reduce converter output voltage overshoot during start-up is also implemented in the proposed modulator. It is achieved by the error amplifier and the compensation capacitor. As the error amplifier output is loaded by a relatively large value compensation capacitor, the error amplifier output cannot suddenly jump to a near-supply-rail voltage even a large voltage difference is existed between its inputs at the beginning of start-up.

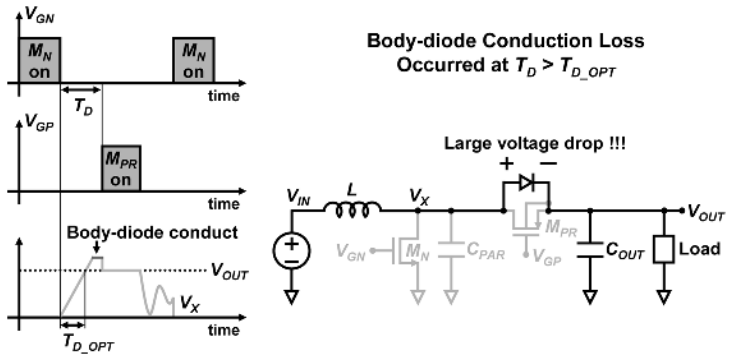

Fig. 8. Illustration of body-diode conduction loss of a boost converter.

As a result, duty cycle of the PWM signal is initially close to zero from which the converter output capacitor is charged through the proposed CCR (discussed in Section III) or body-diode of pMOS transistor if conventional rectifying switch is used. As the compensation capacitor is continuously charged by the error amplifier, duty cycle is slowly increased from zero to steady-state value. It also means that the inductor current and the converter output voltage can gradually increase to the steady-state values. Fig. 7 shows the simulation result of a sub-1V boost converter start-up with the proposed modulator. Same as aforementioned, output of error amplifier $V_{\rm OEA}$ is gradually increased from zero volt to the steady-state value. Duty cycle of the signal applied to the gate of nMOS power transistor $(V_{\rm GN})$ of the boost converter is steadily increased so that the converter output $V_{\rm OUT}$ is gradually increased without any undershoot or overshoot. With the proposed SVMUX, the peak voltage of $V_{\rm GN}$ follows the converter output $V_{\rm OUT}$ once it is larger than its input $V_{\rm IN}$.

III. Proposed CMOS-Control Rectifier

To understand and appreciate how the adaptive dead-time introduced by the proposed CCR improving the converter power efficiency, the relationships between dead-time, charge-sharing loss and body-diode conduction loss are first briefly introduced. Design of the proposed CCR is then thoroughly discussed.

A. Relationships between Dead-Time, Charge-Sharing Loss and Body-Diode Conduction Loss

To prevent shoot-through current from appearing in any synchronous switching converters, dead-time is commonly used. However, a fixed dead-time introduces extra power losses such as the charge-sharing loss and the body-diode conduction loss. This is because the fixed dead-time (T_D) is either too long or too short compared to the optimum dead-time $(T_{D\_\rm OPT})$ as shown in (7)

$$T_{D\_\rm OPT} = \frac{V_{\rm OUT} \cdot C_{\rm PAR}}{I_{L\_\rm PEAK}}, \tag{7}$$

where $C_{\rm PAR}$ is the parasitic capacitor at the switching node (V_X) of the boost converter, and $I_{L\_\rm PEAK}$ is the peak inductor current. When the load current and hence the $I_{L\_\rm PEAK}$ is large, fixed dead-time T_D normally becomes too long compared to the optimum value $T_{D\_\rm OPT}$. As illustrated in Fig. 8, the body-diode of the pMOS rectifying switch $(M_{\rm PR})$ is turned on and carries inductor current (I_L) in the remaining period of dead-time T_D. As the voltage drop of the body-diode is normally much larger than the drain-to-source voltage of a fully turn-on rectifying switch $M_{\rm PR}$, large amount of power is wasted in the form of body-diode conduction loss. As this amount of power is dissipated on the rectifying switch, its thermal stress is inevitably increased. In case the load current and hence the $I_{L\_\rm PEAK}$ is small, fixed dead-time T_D becomes too short compared to the optimum dead-time $T_{D\_\rm OPT}$. As illustrated in Fig. 9, charge stored at the output capacitor $(C_{\rm OUT})$ of the converter is shared by the parasitic capacitor $C_{\rm PAR}$ when the rectifying switching $M_{\rm PR}$ is on at the end of dead-time T_D. In other words, energy stored at the $C_{\rm OUT}$ for the load is wasted in the form of charge-sharing loss.

B. Design of Proposed CMOS-Control Rectifier

As shown by the block diagram in Fig. 10, the proposed CCR consists of a pMOS power transistor (M_P), buffers, and two specially designed comparators (A_1 and A_2) in cross-coupled connection with a coupling capacitor $(C_{\rm CCR})$. The body terminal of M_P is connected to the converter output to eliminate unwanted current flowing from the $V_{\rm OUT}$ node through the body diode to the V_X node. The CCR conducts when the V_X node voltage is larger than the converter output $V_{\rm OUT}$. Otherwise, it is off. This diode-like characteristic enables the CCR to adaptively adjust the dead-time close to the optimum value without the use of sophisticated circuits to acquire the inductor-current level and the parasitic capacitance $C_{\rm PAR}$ at the V_X node. It also enables DCM operation by eliminating the inductor current flowing in negative direction. Therefore, negative-inductor current sensor and dead-time circuit are no longer required in the boost converter with the proposed CCR. The corresponding controller design is also greatly simplified as only one gate signal is required to drive the nMOS power transistor.

However, design of the comparator used in the proposed CCR is very challenging. It is obvious that classical design with common-source-differential input and current-tail bias can not be used. The common-source-differential input imposes a common-mode-voltage limit that disables the classical comparator used in the proposed CCR. The current-tail structure introduces a very strong tradeoff between response time and quiescent-current consumption. It is important to note that the longer the response time means the longer the actual dead-time

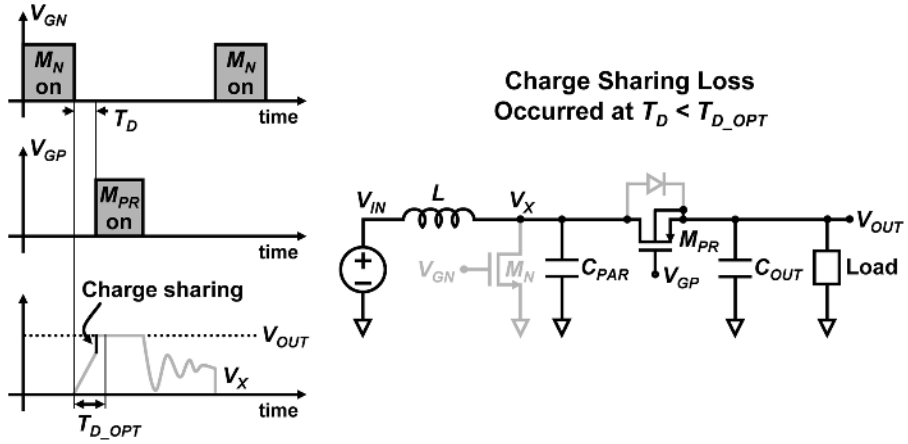

Fig. 9. Illustration of charge sharing loss of a boost converter.

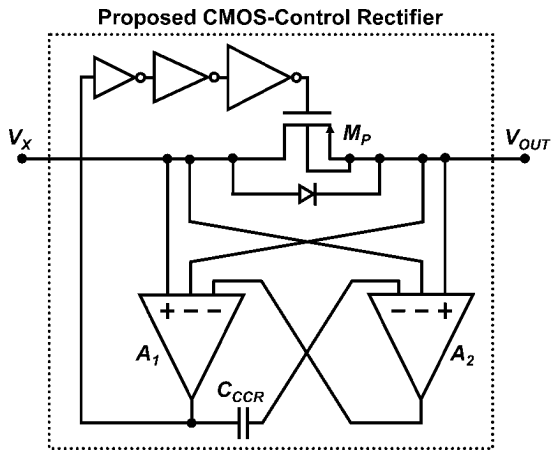

Fig. 10. Block-level schematic of the proposed CMOS-control rectifier.

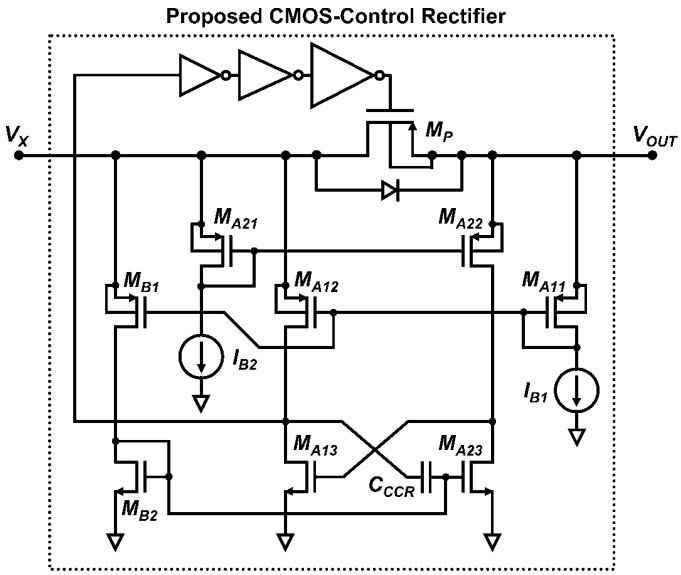

Fig. 11. Transistor-level schematic of the proposed CMOS-control rectifier.

compared to the optimum one, from which more power is lost as body-diode of M_P is forced to conduct.

To overcome the aforementioned challenge, specially designed comparator is proposed. Fig. 11 shows the transistor-level schematic of the proposed CCR in which the comparators A_1 and A_2 are constructed by constant current source I_{B1} and transistors M_{A11} to M_{A13}, and transistors M_{A21} to M_{A23} and constant current source I_{B2}, respectively. The use of source terminal of transistors $M_{A11}, M_{A12}, M_{A21}$, and M_{A22} as inputs of comparators solve the problem of common-mode-voltage limit existed in conventional design. Tradeoff between response time and quiescent-current consumption existed in conventional design is also released due to the fact that slew-rate of the proposed comparator is no longer constrained by the constant current bias. This is easily understood by considering a case that the V_X node voltage is higher than the converter output voltage $V_{\rm OUT}$, in which overdrive voltage of transistor M_{A12} is larger than that of M_{A11}. As a result, current of M_{A12} delivered to the comparator output becomes much larger than the one defined by I_{B1}, and more importantly, it is no longer limited by the constant current source of the comparator.

To enable the proposed CCR with fast on and off time, the comparator should have high slew-rate in both positive and negative direction. This is done by connecting two proposed comparators in cross-coupled connection with the help of a 0.1 pF on-chip PIP coupling capacitor $C_{\rm CCR}$. Regardless of whether the V_X node voltage is smaller or larger than the converter output $V_{\rm OUT}$, either the drain current of transistor M_{A12} or transistor M_{A22}, which is much larger than the constant current source I_{B1} and I_{B2}, can be provided to speed up the comparator response. High slew-rate in positive direction is achieved by the large drain current of M_{A12}. The large drain current of M_{A22} also quickly turns on transistor M_{A13}, which provides large discharging current to enable high slew-rate in negative direction. With the help of coupling capacitor $C_{\rm CCR}$, response time of the proposed CCR is further improved as this capacitor virtually latches these two cross-coupled comparators during transient response. Moreover, this capacitor also provides DC-isolation between the output of comparator A_1 and one of the inputs of comparator A_2. Together with transistors M_{B1} and M_{B2}, which provide DC bias to that input of comparator A_2, stable steady-state operation can be guaranteed.

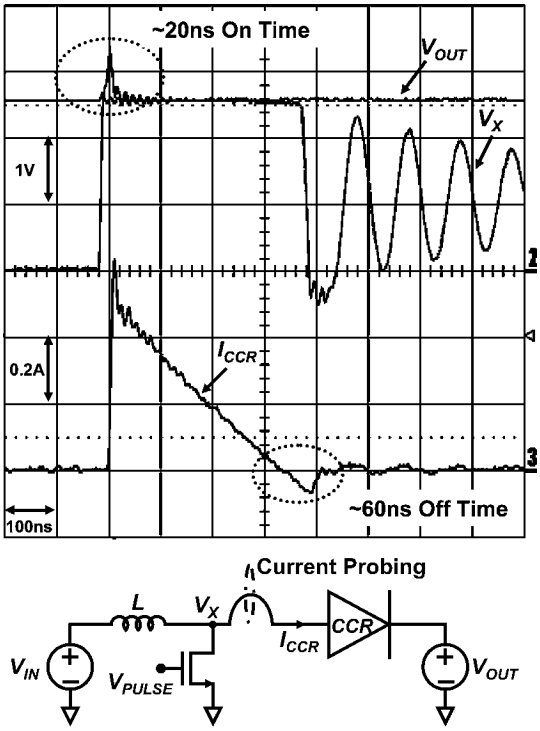

Fig. 12. Measured on and off characteristics of the proposed CMOS-control rectifier.

IV. Experimental Results and Discussions

To facilitate characterization of the proposed CCR, a stand-alone CCR has been fabricated in Austria Micro Systems (AMS) 0.35- μm 2-poly 4-metal CMOS technology. Fig. 12 shows the measured on and off characteristics of the CCR and the corresponding measurement setup. Two voltage sources, $V_{\rm IN}$ and $V_{\rm OUT}$, are set to 0.9 V and 2.5 V, respectively. Inductor (L) with $\sim$1 μH is used. The measurement is done by applying a periodic voltage pulse $(V_{\rm PULSE})$ to the gate of the nMOS power transistor. The period of $V_{\rm PULSE}$ is adjusted to ensure that the inductor current is around zero ampere at the beginning of each cycle. Peak inductor current can hence be adjusted by controlling the pulse-width of $V_{\rm PULSE}$. Once the nMOS power transistor is off, potential of V_X node is increased until the CCR is conducted. The CCR is off when the inductor current flow is changed from positive to negative direction. The measured on and off time of the CCR are $\sim$20 ns and $\sim$60 ns, respectively. This response time difference is caused by the different rate of change of V_X-node voltage. It is observed in Fig. 12 that the V_X-node voltage is quickly increased from zero volt to a level higher than the converter output $V_{\rm OUT}$ when the nMOS power transistor is off. A large voltage difference is hence instantly appeared at the inputs of the comparator of the CCR, from which the CCR is driven to turn on quickly. When the CCR is conducted, the voltage dropped across the CCR depends on the inductor current and the on-resistance of the pMOS power transistor inside the CCR. As on-resistance of power transistor is normally minimized to reduce conduction loss, the voltage dropped across the CCR is relatively small. Moreover, as shown in Fig. 12, current flowing through the CCR is decreased relatively slow. As a result, the voltage dropped across the CCR is small in magnitude and has a slow rate of change. At the instant where the current carried by the CCR is just changed from positive to negative direction, only very small voltage different is appeared at the inputs of comparator inside the CCR, and this voltage takes a relatively longer time to be increased. Therefore, the CCR takes a longer time to be turned off compared to the turn-on case. It is important to note that the measured on and off time shown above is not just the response time of the comparator but including the propagation delay of the buffer inside the CCR.

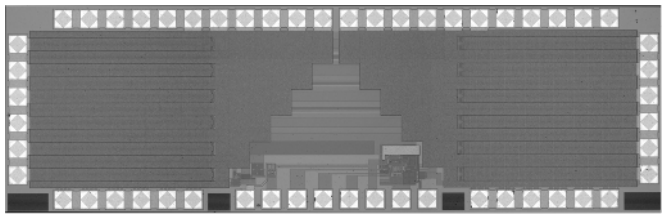

Fig. 13. Chip micrograph of the proposed boost converter.

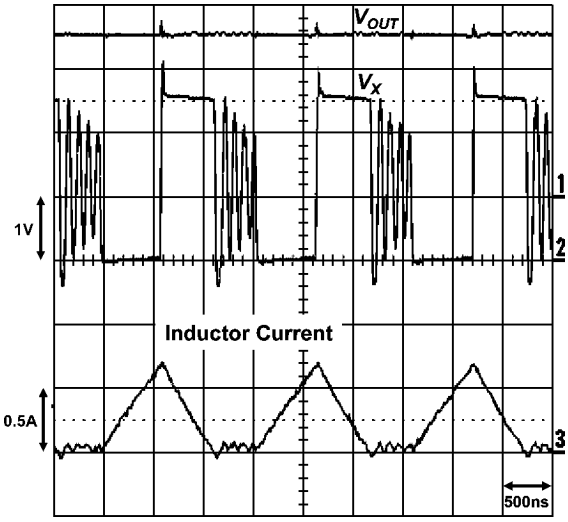

Fig. 14. Measured steady-state operation of the proposed boost converter at 100-mA output current and 1.2-V input voltage.

The boost converter with both the proposed sub-1V pulse-width modulator and the proposed CCR has also been implemented in AMS 0.35-μm 2-poly 4-metal CMOS technology. The chip area is about 3 mm^2, and the chip micrograph is shown in Fig. 13. The converter is able to provide a regulated 2.5-V output voltage and maximum load current of 100 mA at an input voltage ranged from 0.9 V to 1.2 V. A 1 μH off-chip inductor and a 4.7 μF output filtering capacitor are used to facilitate the proposed converter used in today's pocket-size or even thumb-size mobile systems. To minimize the switching loss and hence improve the light-load efficiency, switching frequency of the proposed converter is designed at the sub-MHz range, which is around 667 kHz in the proposed design. Figs. 14 and 15 show the measured steady-state operation of the proposed converter at 100-mA output, and 1.2-V and 0.9-V input, respectively. When the input is 1.2 V, the converter is operated in DCM where ringing is appeared at the V_X node when both the nMOS power transistor and the CCR are off. This unique characteristic

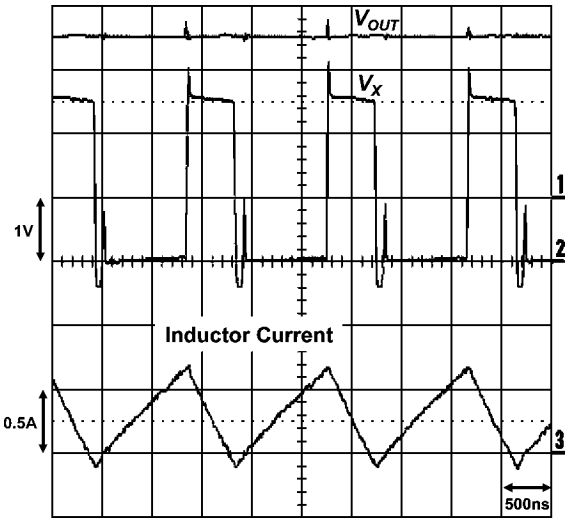

Fig. 15. Measured steady-state operation of the proposed boost converter at 100-mA output current and 0.9-V input voltage.

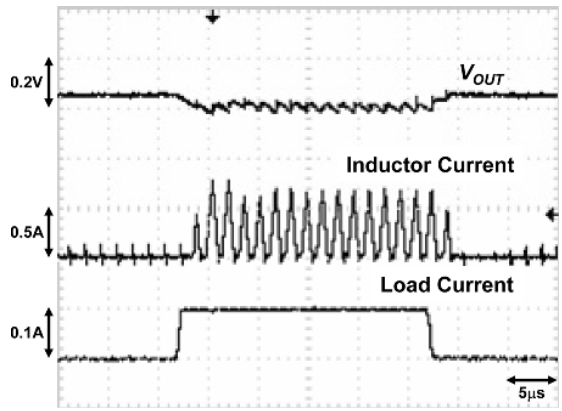

Fig. 16. Measured transient response of the output voltage and the inductor current of the proposed converter with 100-mA load current at 1.2-V input.

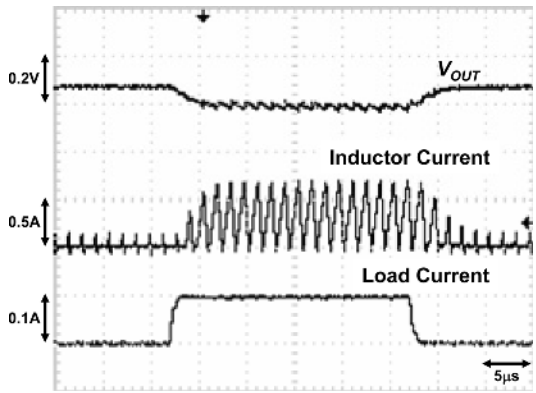

Fig. 17. Measured transient response of the output voltage and the inductor current of the proposed converter with 100-mA load current at 0.9-V input.

of DCM can be easily suppressed with a freewheel switch [15]. As shown in Fig. 15, the proposed converter is able to be directly powered from 0.9-V input, in which the converter is operated very close to the DCM/CCM boundary due to the fact that longer time is required to store energy in the inductor. Figs. 16 and 17 show the measured transient responses of the output voltage and the inductor current of the proposed converter with 100-mA

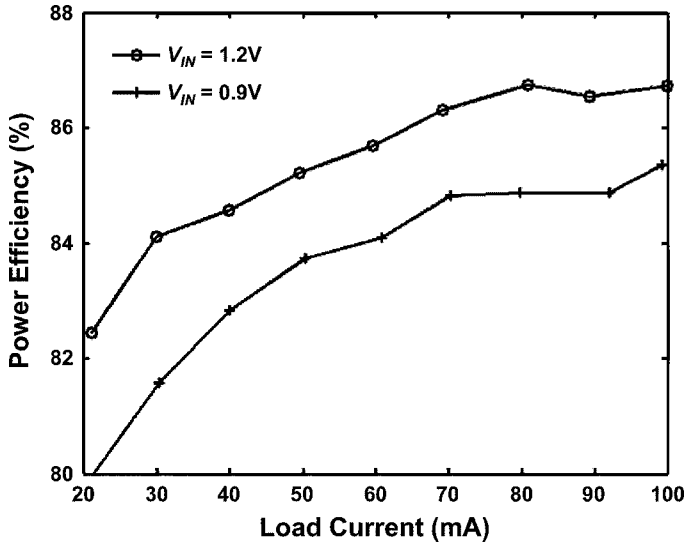

Fig. 18. Measured power efficiency of the proposed boost converter.

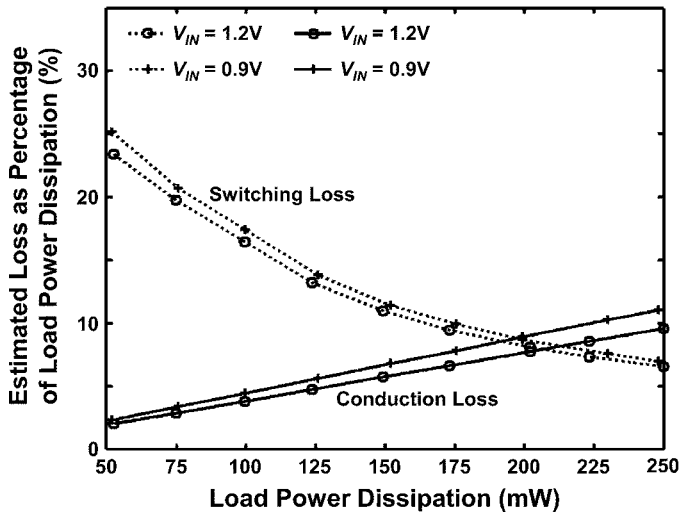

Fig. 19. Estimated power loss distribution as percentage of load power dissipation.

load step (e.g., from 0 mA to 100 mA and vice versa) at 1.2-V and 0.9-V input, respectively. It is shown that the proposed converter has stable operation under wide range of output current and input voltage. Efficiency of the proposed converter is measured and shown in Fig. 18. An estimation of power loss distribution as percentage of load power dissipation is also done according to the measured efficiency and is shown in Fig. 19. Maximum efficiency of ∼87% is achieved at 1.2-V input voltage and 100-mA output current. Even the input voltage is reduced to 0.9 V, ∼85% efficiency is still obtained at 100-mA output current. Finally, performance of the proposed boost converter is summarized in Table I.

V. Conclusion

In this work, a 0.9-V input DCM boost converter delivering 2.5-V and 100-mA output is successfully achieved with both the proposed low-voltage pulse-width modulator and the proposed CCR. The modulator enables the converter to be directly

TABLE I
SUMMARIZED PERFORMANCE OF THE PROPOSED BOOST CONVERTER

Technology	AMS 0.35-μm 2-poly 4-metal CMOS process
Input Voltage Range	0.9V – 1.2V
Output Voltage	2.5V
Maximum Output Current	100mA @ 0.9-V Input
Switching Frequency	~667kHz
Inductor & Its Equivalent-Series Resistance	1μH @ ~50mΩ
Output Capacitor & Its Equivalent-Series Resistance	4.7μF @ ~35mΩ
Maximum Power Efficiency	87% @ 1.2-V Input and 100-mA Output
Linc Regulation	~56mV/V @ 100-mA Output
Load Regulation	~0.046mV/mA @ 0.9-V Input
Chip area with pads	~3mm^2

powered from a 0.9-V input and therefore fully utilize the capacity of a single-cell NiMH battery and thus operation time of single-cell battery operated system is greatly extended. Operation of the modulator is no longer affected by the ripple and transient-induced perturbation of the converter output. Start-up design is greatly simplified compared to the designs where the modulator is powered from the boost converter output. The CCR enables adaptive dead-time to minimize the body-diode conduction loss and the charge-sharing loss such that the boost converter in this design is able to achieve 85% peak efficiency at 0.9-V input and almost 3x step-up ratio. Moreover, the CCR enables the use of microfarad range off-chip capacitor and microhenry range off-chip inductor at submegahertz switching frequency. The size of the entire boost converter can thus be greatly reduced. Light-load efficiency is also improved. More importantly, the proposed CCR is applicable in other switching converters such as buck and non-inverting buck-boost converter to provide adaptive dead-time and minimize thermal stress of rectifying switch.

REFERENCES

[1] J. Varona, A. A. Hamoui, and K. Martin, "A low-voltage fully-monolithic $\Delta\Sigma$-based class-D audio amplifier," in *Proc. 29th European Solid-State Circuits Conf. (ESSCIRC'03)*, Estoril, Portugal, Sep. 16–18, 2003, pp. 545–548.

[2] S. C. Li, V. C. C. Lin, K. Nandhasri, and J. Hgarmnil, "New high-efficiency 2.5 V/0.45 W RWDM class-D audio amplifier for portable consumer electronics," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 9, pp. 1767–1774, Sep. 2005.

[3] C. Y. Leung, P. K. T. Mok, and K. N. Leung, "A 1-V integrated current-mode boost converter in standard 3.3/5-V CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2265–2274, Nov. 2005.

[4] H. Deng, X. Duan, N. Sun, Y. Ma, A. Q. Huang, and D. Chen, "Monolithically integrated boost converter based on 0.5-μm CMOS process," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 628–638, May 2005.

[5] D. Ma, W.-H. Ki, and C.-Y. Tsui, "An integrated one-cycle control buck converter with adaptive output and dual-loop output error correction," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 140–149, Jan. 2004.

[6] E. Bonizzoni, F. Borghetti, P. Malcovati, F. Maloberti, and B. Niessen, "A 200 mA 93% peak efficiency single-inductor dual-output dc-dc buck converter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 11–15, 2007, pp. 526–527.

[7] S. K. Reynolds, "A dc-dc converter for short-channel CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 32, no. 1, pp. 111–113, Jan. 1997.

[8] P. Hazucha, G. Schorm, J. Hahn, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-MHz 80%–87% efficient four-phase dc-dc converter utilizing air-core inductors on package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, Apr. 2005.

[9] M. Alimadadi, S. Sheikhaei, G. Lemieux, S. Mirabbasi, and P. Palmer, "A 3 GHz switching dc-dc converter using clock-tree charge-recycling in 90nm CMOS with integrated output filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 11–15, 2007, pp. 532–33.

[10] T. Y. Man, P. K. T. Mok, and M. Chan, "A CMOS-control rectifier for discontinuous conduction mode switching dc-dc converters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 5–9, 2006, pp. 1408–1417.

[11] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.

[12] K. N. Leung and P. K. T. Mok, "A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.

[13] H. Lin and C. J. Liang, "A sub-1V bandgap reference circuit using subthreshold current," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'05)*, Kobe, Japan, May 23–26, 2005, pp. 4253–4256.

[14] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.

[15] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.

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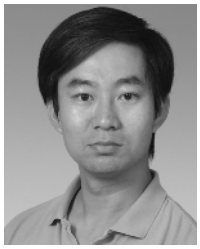

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