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# A 1.0 V, 5.4 pJ/bit GFSK Demodulator Based on an Injection Locked Ring Oscillator for Low-IF Receivers

SOONYOUNG HONG<sup>1</sup>, (Student member, IEEE), ARUP K. GEORGE<sup>1</sup>, (Member, IEEE),  
DONGGU IM<sup>2</sup>, (Member, IEEE), MINKYU JE<sup>3</sup>, (Senior Member, IEEE) AND JUNGHYUP LEE<sup>1</sup>,  
(Member, IEEE)

<sup>1</sup>Department of Information and Communication Engineering, Daegu Gyeongbuk Institute of Science and Technology (DGIST), Daegu, South Korea

<sup>2</sup>Department of Electronic Engineering, Jeonbuk National University, Jeonju-si, South Korea

<sup>3</sup>School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

Corresponding author: Junghyup Lee ([jhleel@dgist.ac.kr](mailto:jhleel@dgist.ac.kr)).

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**ABSTRACT** This paper presents an ultra-low power, low cost demodulator for gaussian frequency shift keying (GFSK) receivers that use low intermediate frequencies (IF). The demodulator employs a direct IF to digital data conversion scheme by using an injection-locked ring oscillator (ILRO) with a 1-bit flip-flop. It consumes 2.7  $\mu$ W from a 1.0 V supply at a data rate of 500 kbps achieving an energy efficiency of 5.4 pJ/bit which is 30 times better than that of the recently presented works. The demodulator also achieves 17.5 dB SNR at 0.1 % BER while operating at the same data rate. The demodulator is implemented in a 0.18  $\mu$ m standard CMOS process and occupies an active area of 0.012 mm<sup>2</sup>.

**INDEX TERMS** Demodulator, GFSK, low power, injection locked ring oscillator, low-IF, CMOS.

## I. INTRODUCTION

Gaussian frequency shift keying (GFSK) is a popular modulation scheme for short-range, multi-channel communication standards such as Bluetooth and WPAN due to its high sensitivity and superior spectral efficiency [1]. Several GFSK transceivers have been actively developed in order to implement a physical layer for wireless networks [2]. The demand for GFSK transceivers having small feature sizes and lower power consumption has increased in recent Internet-of-Things (IoT) and Medical Implanted Communication Service (MICS) applications. Consequently, research efforts have been focused on reducing the feature size as well as the power consumption of such transceivers [3-4]. GFSK transmitters can be power-efficient, as the constant envelope characteristics of the GFSK modulation allow the use of energy-efficient nonlinear power amplifiers, enabling a low-power operation without any data distortion caused by spectral regrowth [5]. However, conventionally, GFSK receivers have a complicated structure and consume larger power. Secondly, they tend to have a large size, limiting their suitability for such

size-constrained and low-power applications. To address these problems, the zero-IF and low-IF architectural flavors that integrate all filter components to a single chip are commonly used in the GFSK receivers [6]. However, the zero-IF has intrinsic issues caused by flicker noise and DC offset as well as local oscillator leakage. As a result, the low-IF is a more preferred option for enhanced signal-to-noise ratio (SNR) performance. Nevertheless, the low-IF receivers still suffer from relatively low energy efficiency due to the high frequency operation needed in detecting two different IF frequencies during the demodulation process. Therefore, in this paper, we present an ultra-low power, low cost demodulator for the GFSK receivers with a low IF that can improve the energy efficiency by more than 30 times than those of the recently presented works [7-10].

Several GFSK demodulators employing techniques such as delay line discrimination [7], zero-crossing detection [8], phase domain analog-to-digital conversion [9], and FM discrimination [10] have been reported in prior literature. The delay line discrimination approach of [7] is complex and

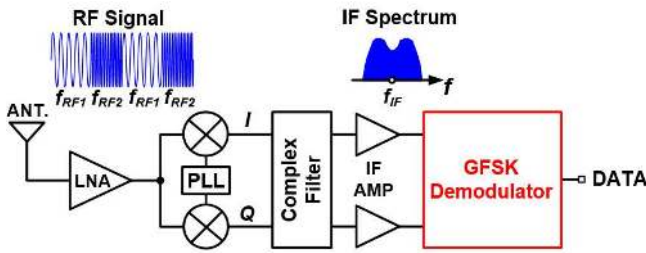


FIGURE 1. Overall structure of a GFSK receiver with a low IF.

consumes large power of about 200  $\mu$ W as it uses two voltage-controlled delay loops for its operation. Similarly, the zero-crossing technique used in [8] also has a limited suitability for low power operation as it uses a Sallen-Key filter and a differentiator whose power consumptions are 270  $\mu$ W and 180  $\mu$ W respectively. The demodulator based on the phase domain analog-to-digital converter in [9] needs several current mirrors and comparators and thus inevitably consumes over 500  $\mu$ W. The last structure with the FM discriminator [10] still consumes large power of 170  $\mu$ W due to the high sampling frequency of 32 MHz. Thus, the recent demodulators for the GFSK receivers are less suitable to be employed in low power sensor nodes or in bio-medical applications.

To solve the above-mentioned problems regarding area and power consumption, we propose an injection locked ring oscillator (ILRO) based GFSK demodulator. The GFSK demodulator for low-IF receivers presented in this paper dissipates only 2.7  $\mu$ W from a 1 V supply, equivalent to an energy efficiency of 5.4 pJ/bit at a data rate 500 kbps. The rest of this paper is organized as follows: Section II presents the proposed demodulator architecture employing an ILRO. Section III discusses the detailed ILRO operation in the demodulator for direct IF to data conversion. Section IV presents the simulation and chip measurement results before concluding this article in Section V.

## II. PROPOSED GFSK DEMODULATOR

The architecture of GFSK receivers using a low IF scheme is shown in Fig. 1. It comprises a low noise amplifier, mixers, a local oscillator, a complex filter, IF amplifiers as well as a demodulator. The RF front-end amplifies and down converts the RF input to the IF signal. The image components from the IF signal are filtered out by the complex filter, and the digital data is recovered by the demodulator. Among the various blocks of a GFSK receiver, the demodulator is one of the components that dissipate significant power and hence, minimizing it is essential in improving the overall power efficiency [8]. This paper proposes an ultra-low power, low cost GFSK demodulator using an ILRO towards achieving this end.

The proposed GFSK demodulator based on an ILRO is shown in Fig. 2. The input signal is down-converted to IF signal (A). The frequency  $f_{IF1}$  represents a data bit ‘1’ while the frequency  $f_{IF2}$  represents a data bit ‘0’. The signal A is passed through a limiter to obtain B, which has a constant

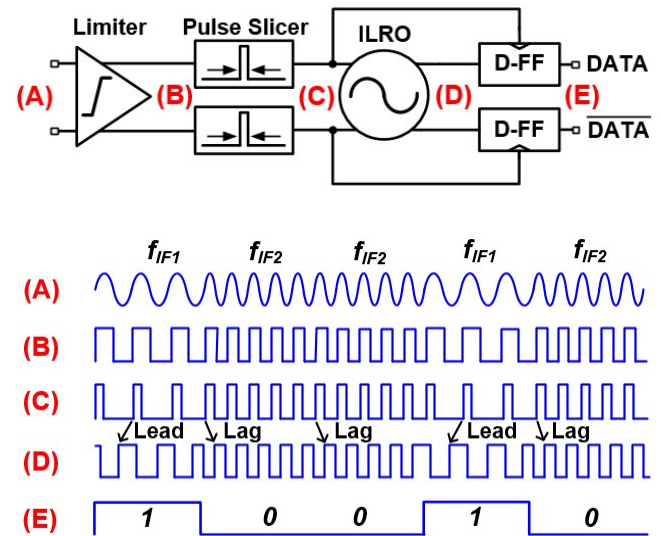


FIGURE 2. Block diagram and timing waveforms of the proposed ILRO based GFSK demodulator.

voltage swing. The pulse slicer generates an approximately 25%-width pulse output C that serves as the injection signal to the ILRO from its input B. The ILRO, once locked, maintains the phase differences between the injection input C and its output D such that C will always lead or lag D when the modulator input frequencies are  $f_{IF1}$  and  $f_{IF2}$  respectively. The flip-flop (DFF) serves as a 1-bit time-to-digital converter that samples the ILRO output D during the rising edge of the injection pulse C. Given the fixed lead/lag relationships between C and D established by the ILRO, the input data can be reliably demodulated by this approach as D will sample a logic high from the signal C when the input frequency is  $f_{IF1}$  and a logic low when the input frequency is  $f_{IF2}$ . In comparison to conventional demodulators, the proposed architecture is simple and digital-intensive while the overall power consumption is significantly lower than conventional approaches that uses analog methods.

Fig. 3(a) shows the schematic of the differential N-stage ILRO used in the proposed GFSK demodulator. Note that we use a 4-stage ILRO ( $N=4$ ) in this implementation. The injection signals  $V_{INJN}$  and  $V_{INJP}$  are complementally injected into the first nodes  $V_{1N}$  and  $V_{1P}$  by using NMOS switches. The phase-shifted outputs  $V_{OUTN}$  and  $V_{OUTP}$  are obtained from the nodes  $V_{2N}$  and  $V_{2P}$  respectively. The free running frequency of the ILRO is determined by the delay cell’s PMOS current source bias  $V_{CS}$  as shown in Fig. 3 (a). In addition, a latch circuit formed by cross-coupled inverters are added to the delay cells to minimize the rise/fall times of the ILRO node signals. The schematic of the pulse slicer used in the GFSK demodulator is shown in Fig. 3 (b). The pulse slicer makes the pulse-width of the ILRO injection signal approximately equal to the time constant  $R_1C_1$ , designed such that the pulse slicer output width is  $\sim 25\%$  of that of the free-running ILRO output. The reason for using the 25% duty-cycle will be explained in Section IV. The pulse slicer input and a delayed version of the same are

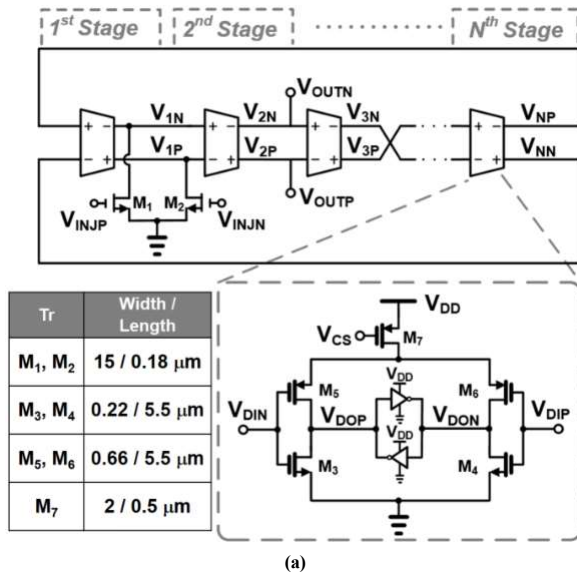


FIGURE 3. Schematics of the differential ILRO and its delay cell (a), and the pulse slicer (b).

passed through an XOR gate to generate pulses on both the rising and falling edges of the input. Only the pulse generated on the rising edge of the input goes to the output due to the AND operation.

### III. DIRECT IF TO DATA CONVERSION BASED ON AN ILRO

An ILRO, as discussed in the previous section, can enable a simple and energy efficient conversion of IF to data and is hence a key building block in the proposed GFSK demodulator. In this section, we discuss the detailed operation of the ILRO, and in particular, the transient response of the injection locking process depending on whether the injection signal is higher or lower than the free-running frequency of the VCO. We will also discuss, how this can be used for a direct conversion of the IF to its equivalent digital data. Primarily, the ILRO comprises a chain of interconnected delay cells as shown in Fig. 3 (a). As mentioned in the earlier section, the NMOS switch with the input V<sub>INJN</sub> pulls down V<sub>1P</sub> to GND when V<sub>INJN</sub> is high. Given that V<sub>INJN</sub> and V<sub>INJP</sub> are complimentary to each other, V<sub>1N</sub> remains floating as the V<sub>INJP</sub> switch gets turned off. However, since V<sub>1P</sub> and V<sub>1N</sub> are interconnected by a latch as shown in Fig. 3 (a), V<sub>1N</sub> is pulled high. The overall effect of the nodes V<sub>1P</sub> and V<sub>1N</sub> being pulled down and up is that the phase-delay contribution of the individual delay stages

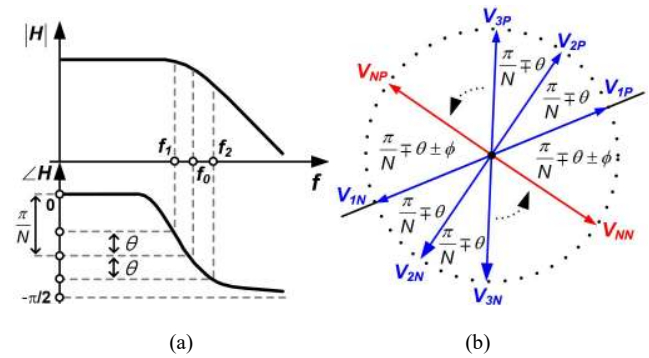


FIGURE 4. Frequency response of the delay cell (a) and a phase diagram for injection locking (b).

changes in response to the relative frequency of the injection signal to that of the free-running frequency, taking the ILRO to be locked to a frequency equivalent as that of the injection signal. To explain this, we consider the phase response of an individual delay stage when the ILRO is free-running and also when it is injection locked.

#### A. PHASE-SHIFT OF DELAY-CELLS IN AN ILRO

A delay cell in the N-stage ILRO can be modeled as a single pole amplifier, whose amplitude response rolls off at -20 dB/dec after the dominant pole and the phase difference between the input and output reaches  $-\pi/2$  radians at frequencies significantly higher the dominant pole as shown by the frequency response in Fig. 4 (a). In the ILRO, for the oscillation to sustain, the total phase shift of the loop must be a multiple of  $2\pi$  so as to meet the Barkhausen criteria [11]. To meet this, an ILRO having even number of stages, has to cross couple the inputs to one of the stages from the previous stage's outputs. In this implementation 4th delay-cell inputs are cross coupled to 3rd delay-cell outputs. In the absence of an injection signal, each non-cross-coupled delay cells of the ILRO adds a phase of  $(\pi + \pi/N)$ , while the cross coupled delay cell adds a phase of  $\pi/N$  making sure that the Barkhausen criteria is met. Note, that this phase delay responses are valid only for ILROs with even number of stages. A given delay-cell introduces an intrinsic phase reversal equivalent to  $\pi$  radians to its input signal. In addition, a variable component equal to  $\pi/N$  that depends on the number of delay stages is also added. Note that the cross-coupled stage does not add the intrinsic phase reversal to its input. Since the intrinsic phase reversal of the delay remains constant irrespective of whether the injection signal is present, it can be omitted from the rest of the analysis and is not included in the frequency response shown in Fig. 4 (a). The effect of injection locking is that the variable phase-delay of each of the delay cells changes in response to the injection signal to move the ILRO frequency to a locked state. It can be shown that once the ILRO is locked to the injection frequencies of  $f_0 \pm \Delta f$  (f<sub>1</sub> and f<sub>2</sub>), the phase shift of the delay cell changes to  $\pi/N \pm \theta$ . The overall phase-shift can be expressed as:

$$\begin{cases} (N-1)\pi + N\left(\frac{\pi}{N} - \theta\right) + \phi = 2m\pi, & \text{for } f_{INJ} < f_0 \\ (N-1)\pi + N\left(\frac{\pi}{N} + \theta\right) - \phi = 2m\pi, & \text{for } f_{INJ} > f_0 \end{cases} \quad (1)$$

where,  $\theta$  represents the amount of phase shift caused by the change in oscillation frequency as shown by the frequency response of the delay cell (Fig. 4 (a)), and  $\phi$  represents the additional amount of phase shift generated by first delay cell due to the signal injection. The factor  $(N-1)\pi$  is the sum of the intrinsic phase-shift introduced by all the delay cells in the ILRO and remains a constant. However, when injection locking occurs at a different frequency from the free-running frequency, for satisfying (1), the value of  $\mp N\theta$  must be canceled by  $\pm\phi$  so that the overall phase shift of the oscillator loop becomes  $2m\pi$  ( $m=1, 2 \dots$ ) to maintain oscillation at the input injection frequency. As shown in Fig. 4 (b), therefore, the phase shift of delay cell  $D_1$ ,  $\zeta'$ , and the phase shift of other delay cells,  $\zeta$ , when  $f_{INJ}$  is less than  $f_0$ , can be described as follows:

$$\begin{cases} \zeta = \frac{\pi}{N} - \theta, \\ \zeta' = \frac{\pi}{N} - \theta + \phi = \frac{\pi}{N} - \theta + N\theta \end{cases} \quad (2)$$

Similarly, the phase shift of delay cell  $D_1$ ,  $\psi'$ , and the phase shift of other delay cells,  $\psi$ , when  $f_{INJ}$  is greater than  $f_0$ , can be described as follows:

$$\begin{cases} \psi = \frac{\pi}{N} + \theta, \\ \psi' = \frac{\pi}{N} + \theta - \phi = \frac{\pi}{N} + \theta - N\theta \end{cases} \quad (3)$$

where,  $\theta$  according to the oscillation frequency in the lock state can be expressed as [12]:

$$\theta = \left| \tan^{-1} \left[ \tan \left( \frac{\pi}{N} \right) \frac{f_{INJ}}{f_0} \right] - \frac{\pi}{N} \right| \quad (4)$$

### B. TRANSIENT RESPONSE OF THE ILRO

To understand the concept of the injection locking process in the ILRO, we can consider the transient response of the output nodes of each of the ILRO delay cells. Several possible scenarios that show the relative alignment of an injection signal to the free-running VCO clock frequency ( $f_0$ ) and how it modifies the phase-response of the ILRO clock outputs are shown Fig. 5. The illustration only shows the effect of a single injection signal pulse. As discussed earlier, in the absence of an injection signal, each of the delay cells introduce a variable phase-delay equivalent to  $\pi/N$ . We assume that the equivalent time-delay corresponding to a phase-delay of  $\pi/N$  is represented by  $\Delta t_{DEL}$ . The effect of the injection signals  $V_{INJP}$  or  $V_{INJN}$  are that it pulls down the nodes  $V_{IN}$  or  $V_{IP}$  to GND

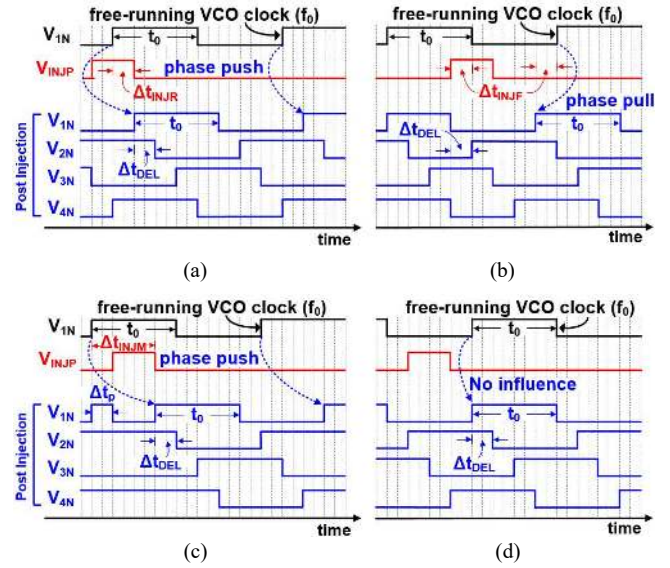
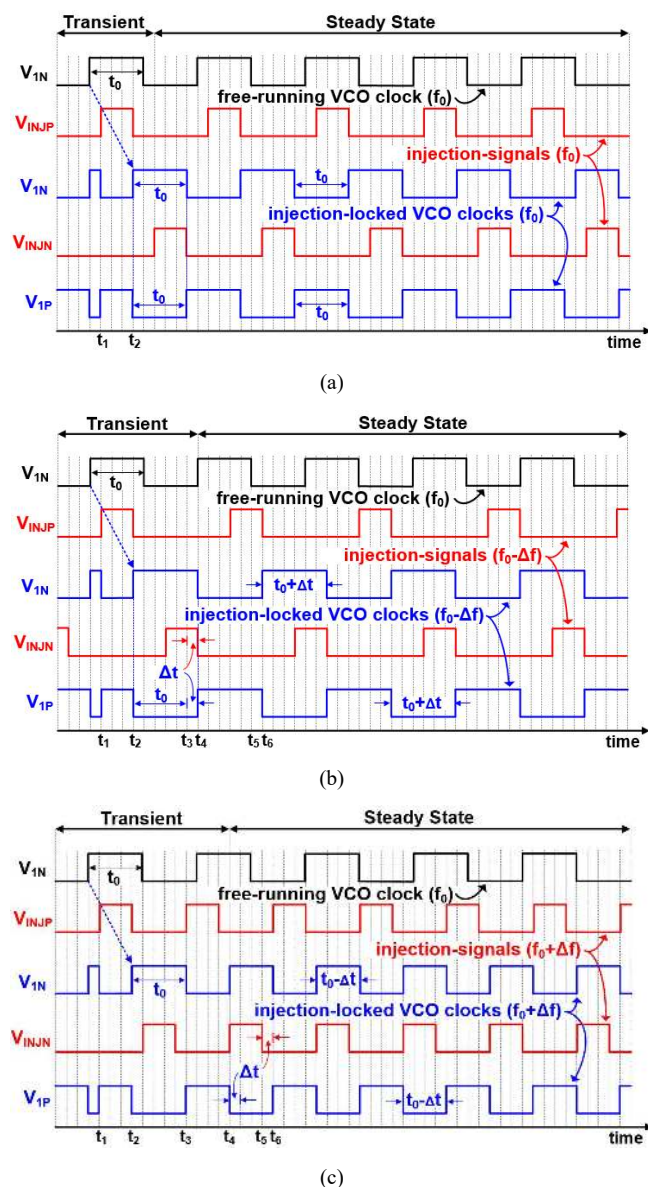


FIGURE 5. Change of 4-stage ILRO output according to injection position rising edge (a), falling edge (b), high state (c) and low state (d).

when one of them goes high. If either  $V_{IN}$  or  $V_{IP}$  are already at the GND level, the injection signal does not alter that node at all. Thus, the injection signal can affect the ILRO when both  $V_{IN}$  and  $V_{INJP}$  are high or when  $V_{IP}$  and  $V_{INJN}$  are high. The relative alignment of the injection signal and the free-running clock pulse can be summarized into four different scenarios:

- **Scenario 1:** The injection pulse  $V_{INJP}$  overlapping the rising edge of the free-running clock  $V_{IN}$  as shown in Fig. 5 (a). The overlap interval between  $V_{INJP}$  and  $V_{IN}$  is denoted as  $\Delta t_{INJR}$ .
- **Scenario 2:**  $V_{INJP}$  overlapping the falling edge of the  $V_{IN}$  as shown in Fig. 5 (b). The overlap interval in this case is denoted as  $\Delta t_{INJF}$ .
- **Scenario 3:**  $V_{INJP}$  overlapping the high-state of  $V_{IN}$  as shown in Fig. 5 (c), where the time-interval between the rising edge of  $V_{IN}$  and the falling edge of the injection signal is  $\Delta t_{INJM}$ .
- **Scenario 4:**  $V_{INJP}$  overlapping the low-state of  $V_{IN}$  as shown in Fig. 5 (d).

When the injection signal  $V_{INJP}$  overlaps the rising edge of the free-running signal  $V_{IN}$ , (Fig. 5 (a)), the low state of the  $V_{IN}$ , is retained for an additional  $\Delta t_{INJR}$  time. The result of this is that the  $V_{IN}$  pulse is delayed by  $\Delta t_{INJR}$ . In contrast, when  $V_{INJP}$  overlaps the falling edge of  $V_{IN}$ , (Fig. 5 (b)), the injection signal pulls down  $V_{IN}$  earlier by  $\Delta t_{INJF}$ , causing the  $V_{IN}$  to advance by the same time-interval. When  $V_{INJP}$  overlaps with the high-state of  $V_{IN}$ , (Fig. 5 (c)), the effect on  $V_{IN}$  is similar to that of the case shown in Fig. 5 (a), where the rising edge is delayed. However, in this case, the delay time is equivalent to the time-interval between the rising edge of  $V_{IN}$  and the falling edge of the injection signal,  $\Delta t_{INJM}$ . Effectively, this scenario



**FIGURE 6.** Injection-locking transient responses at  $f_{INJ} = f_0$  (a),  $f_{INJ} < f_0$  (b) and  $f_{INJ} > f_0$  (c).

is equivalent to resetting  $V_{IN}$  by the  $V_{INJP}$ . Note that the reset operation causes a glitch in the  $V_{IN}$  waveform, whose width is shown as  $\Delta t_p$ . If  $\Delta t_p$  is lower than the default delay time of the subsequent stages, it will not affect them as shown in Fig. 5 (c). However, if  $\Delta t_p$  is larger, this glitch would manifest in  $V_{2N}$ ,  $V_{3N}$  and also  $V_{4N}$ . Irrespective of the magnitude of  $\Delta t_p$ , the fact that the rising edge would be delayed remains the same. Finally, the  $V_{INJP}$  has no effect on  $V_{IN}$  when it overlaps with its low-state as shown in Fig. 5 (d). In a practical operating scenario, a sequence of the above four cases lead the ILRO to be locked to a frequency equal to the injection signal.

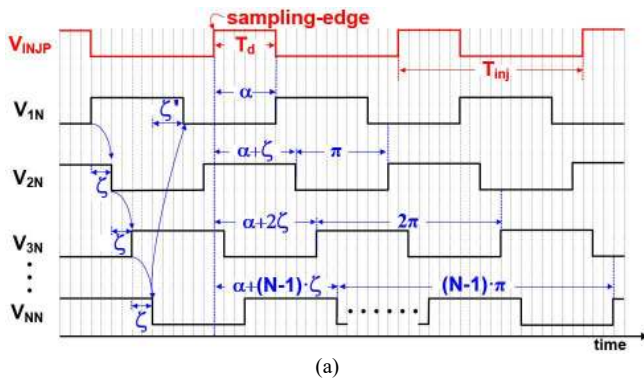
To illustrate the locking mechanism further, the transition process from a free-running state to a locked state when the injection signal is applied to the middle of high state of free-running signal (shown in Fig. 5 (c)), is shown in Fig. 6. In

practice, the relative alignment of the injection signal could possibly be any one of the scenarios mentioned in Fig. 5. However, this scenario is chosen for illustration as it involves the events shown in the other cases of Fig. 5 as will be discussed later.

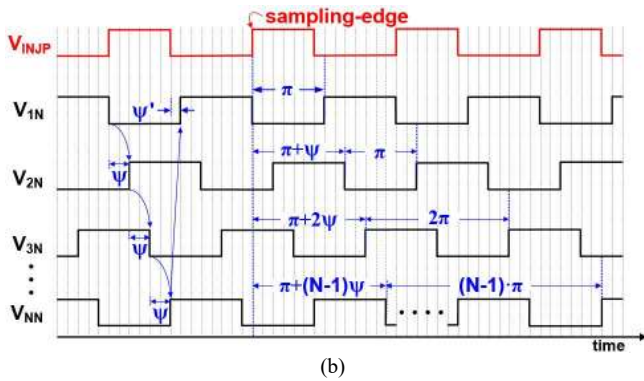
The transient operation is discussed for cases when the injection signal frequency is equal to, lower and higher than the free-running frequency of the ILRO. Fig. 6 (a) shows the transient operation when the frequency of  $V_{INJP}$  is equal to the free-running frequency of the ILRO,  $V_{IN}$ . The  $V_{INJP}$  signal resets the node voltage  $V_{IN}$  to GND at the instant  $t_1$ . As the  $V_{INJP}$  goes low, the  $V_{IN}$  node rises to a high-state at  $t_2$ , thereby delaying the rising edge of the free-running VCO clock. This is the scenario 3 of the locking process. Thereafter, the  $V_{INJP}$  or the  $V_{INJN}$  signals will not affect the ILRO operation, as they would overlap with the low-state of the  $V_{IN}$  and  $V_{IP}$ , which is the scenario 4 of the locking process. Thus, despite the phase-push introduced by  $V_{INJP}$  and  $V_{INJN}$ , the ILRO frequency remains the same. Fig. 6 (b) shows the transient operation when the frequency of  $V_{INJP}$  is lower than the free-running frequency the ILRO,  $V_{IN}$ . At the instant  $t_1$ , the  $V_{INJP}$  goes high, pulling down the  $V_{IN}$  to GND. At  $t_2$ , the  $V_{INJP}$  goes low, leaving  $V_{IN}$  floating. As a result, the rising edge of  $V_{IN}$  is delayed to the instant  $t_2$ , causing a phase-push (scenario 3). In the absence of the injection signal at  $V_{INJN}$ , the  $V_{IP}$  should have gone to a high-state at the instant  $t_3$ . However, as  $V_{IP}$  is pulled down by  $V_{INJN}$  until  $t_4$  the signal  $V_{IP}$  stays low for an extended period of  $\Delta t$ , thereby locking the ILRO to the lower injection frequency (scenario 1). Between  $t_5$  and  $t_6$ , the  $V_{INJP}$  holds  $V_{IN}$  down to GND for an additional  $\Delta t$  (scenario 1). Once a lock is achieved, the scenario 1 repeats alternatively in  $V_{IN}$  and  $V_{IP}$ . When the injection signal frequency is higher than the free running frequency of the ILRO (Fig. 6 (c)), a phase-push happens and delays the rising edge of the  $V_{IN}$  to  $t_2$  (scenario 3). Between  $t_2$  and  $t_4$ ,  $V_{INJN}$  and  $V_{INJP}$  go high without influencing the current state of  $V_{IP}$  and  $V_{IN}$  respectively as they are already at GND (scenario 4). However, at  $t_4$ ,  $V_{INJN}$  pulls down  $V_{IP}$  to GND, causing the  $V_{IN}$  to rise to a high-state instantaneously (scenario 2). The overall effect of this is that the period is reduced by  $\Delta t$ , thereby locking the ILRO to the injection frequency that is higher than the free-running frequency. Once locked, the scenario 2 repeats alternatively in  $V_{IN}$  and  $V_{IP}$ . In summary, the complimentary injection signals  $V_{INJP}$  and  $V_{INJN}$  introduces a phase-push/pull along with the widening or shortening of the ILRO outputs leading it to be locked with a frequency lower or higher than the nominal ILRO operating frequency.

### C. PHASE RELATIONSHIPS OF THE ILRO

Fig. 7 shows the output waveform of each node of N-stage ILRO in the steady state after injection locking. When the ILRO is locked to an injection signal frequency that was originally lower its free-running frequency as shown Fig. 7 (a), the phase-delay between the successive edges between  $V_{NN}$  and  $V_{IN}$  becomes equal to  $\zeta_i = \pi/N - \theta + \phi$  as shown by



(a)



(b)

FIGURE 7. Phase-relationships with the sampling edge at  $f_{INJ} < f_0$  (a) and  $f_{INJ} > f_0$  (b).

TABLE I  
SAMPLING STATE ACCORDING TO THE PHASE DIFFERENCE

Output Stage	$f_{INJ} < f_0$ or $f_{INJ} > f_0$	
Even	$PD_k > k\pi$	Low
	$PD_k < k\pi$	High
Odd	$PD_k > k\pi$	High
	$PD_k < k\pi$	Low

equation (2). However, the delay between the successive edges of the other stages such as between  $V_{1N}$  and  $V_{2N}$ ,  $V_{2N}$  and  $V_{3N}$  and so on remains at  $\zeta = \pi/N - \theta$ . The output is obtained by sampling one of the ILRO outputs using the injection locking clock. The fixed relative-phase relationship between the injection signal and the locked ILRO outputs enable latching one of the outputs at the sampling edge such that the output is registered as logic-high or logic-low. To explain this and to develop a closed form expression, the phase difference (PD) between the sampling edge of the input signal  $V_{INJP}$  and the successive rising edges of ILRO delay cell outputs  $V_{kN}$  can be obtained as follows:

$$PD_k = \alpha + (k - 1) \cdot \left( \pi + \frac{\pi}{N} - \theta \right) \quad \text{for } f_{INJ} < f_0 \quad (5),$$

where  $k$  denotes the index of the stage from which the output is taken. In (5),  $\alpha$  denotes a phase equivalent to a duty-cycle of

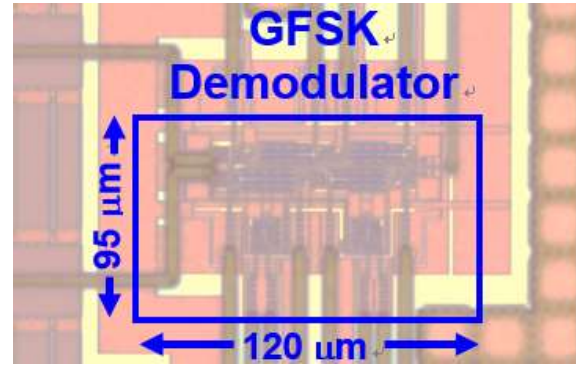


FIGURE 8. Chip micrograph.

$T_d \times 2\pi / T_{inj}$ . Similar to this, a definite phase-relationship exists between  $V_{INJP}$  and  $V_{NN}$ , when the injection signal frequency is higher than the free-running ILRO frequency as shown in Fig. 7 (b). The phase-delay between the successive edges between  $V_{NN}$  and  $V_{1N}$  becomes equal to  $\psi' = \pi/N + \theta - \phi$  from equation (3). However, the delay between the successive edges of the other stages such as between  $V_{1N}$  and  $V_{2N}$ ,  $V_{2N}$  and  $V_{3N}$  and so on becomes at  $\psi = \pi/N + \theta$ . In this case, however, the PD between the sampling edge of the input signal  $V_{INJP}$  and the successive rising edges of ILRO delay cell of outputs  $V_{kN}$  can be shown as:

$$PD_k = \pi + (k - 1) \cdot \left( \pi + \frac{\pi}{N} + \theta \right) \quad \text{for } f_{INJ} > f_0 \quad (6)$$

Using the relationships (5) and (6), an appropriate ILRO output can be sampled as the demodulator output as shown in Table I. Due to the injection locking, a well-defined phase-relationship is established between  $V_{INJP}$  and the ILRO outputs  $V_{kN}$  and  $V_{kP}$ , where  $k$  refers to the state from which the outputs are taken. As shown in Table I, for an even stage, ( $k=2, 4, \dots$ ) if the total phase difference between the sampling edge and the rising edge of  $k^{\text{th}}$  delay cell output is greater than  $k\pi$ , the output will be sampled as active low. On the contrary, if the phase difference is less than  $k\pi$ , the output will be sampled as active high. If the outputs are taken from the odd numbered stages ( $k=1, 3, \dots$ ) and the overall phase difference between the sampling edge and the rising edge of  $k^{\text{th}}$  delay cell output is higher than  $k\pi$ , the output will be sampled as active high. If the phase difference is lower than  $k\pi$ , the output will be sampled as active low.

Finally, as observed from (5) and (6), the sampled output state in the cases when  $f_{INJ}$  is greater or lower than  $f_0$  depends on the duty-cycle of injection signal. As shown in Table I and using  $N=4$  and  $k=2$  (values used by this design as discussed later), the DFF samples the low-state when the duty-cycle is over 38 % and the high-state when the duty-cycle is less than 38 % when  $f_{INJ}$  is lower than  $f_0$ . However, when  $f_{INJ}$  is higher than  $f_0$ , the DFF is always sampled as a logic-low as shown by (6) and Table I. Therefore, in this paper, a duty-cycle of 25 % is used so as to provide a margin of 13 % from the maximum

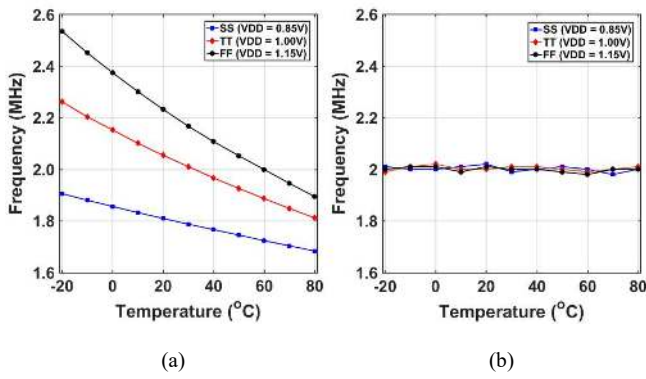


FIGURE 9. Change of free-running frequency of ILRO according to PVT (a) before calibration (b) after calibration.

TABLE II  
POWER BREAKDOWN OF THE DEMODULATOR

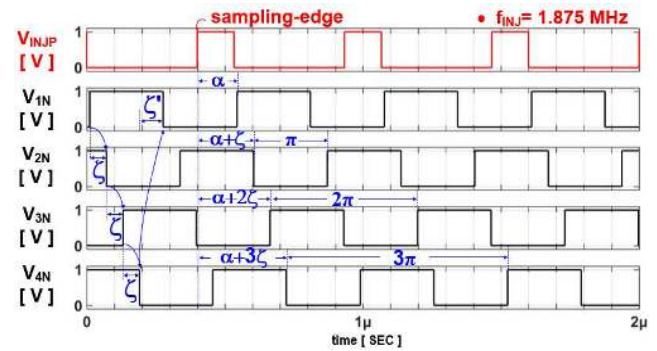
Limiter	220 nA
Pulse Slicer	560 nA
ILRO	1.5 $\mu$ A
Latch	270 nA
DFF	150 nA
<b>Total Power</b>	<b>2.7 <math>\mu</math>W</b>

allowable duty cycle where the sampled outputs remain complimentary to each other.

#### IV. SIMULATION AND MEASUREMENT RESULTS

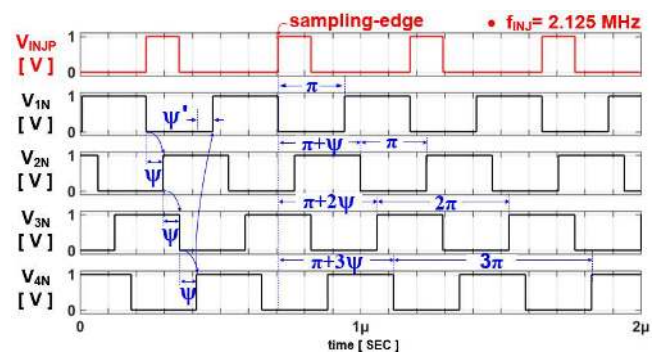
Fig. 8 shows the chip micrograph of the proposed GFSK demodulator. The demodulator is implemented in a 0.18  $\mu$ m standard CMOS process and occupies an active area of  $95 \times 120 \mu\text{m}^2$ . The proposed demodulator consumes an average current of 2.7  $\mu$ A from a 1.0 V supply. The power breakdown of the receiver is shown in Table II. The most of power is consumed by the ILRO. The demodulator frequency has to be chosen to strike a balance between power consumption and the transient settling time of the ILRO to get to a locked state. For this reason, 2 MHz was selected for the design goal of power consumption under 3  $\mu$ W and 500 kbps data-rate. The ILRO used in the demodulator has 1.4 MHz (1.3 ~ 2.7 MHz) lock range.

The proposed demodulator is vulnerable to PVT variation due to the open-loop operation of the ILRO. Deviation of the free-running frequency from the IF frequency of the receiver degrades the BER performance of the demodulator. Such effects can be minimized by using an external reference clock and a frequency locked loop (FLL) using a replica VCO [13]. This implementation, however, does not include an on-line calibration circuit to mitigate the PVT effects. The free-running frequency of ILRO is tuned to the IF frequency used



Parameter	$\zeta$	$\zeta'$	$\theta$	$\phi$	$PD_2$	Sampling state
Phase [ $^\circ$ ]	43.2	50.4	1.8	7.2	313.2	High

(a)



Parameter	$\psi$	$\psi'$	$\theta$	$\phi$	$PD_2$	Sampling state
Phase [ $^\circ$ ]	46.8	39.6	1.8	7.2	406.8	Low

(b)

FIGURE 10. Simulation results of 4-stage differential ILRO at  $f_{INJ} < f_0$  (a) and  $f_{INJ} > f_0$  (b).

in the receiver by adjusting  $V_{CS}$ . Fig. 9 shows the change of ILRO's free-running frequency due to PVT variations and results of calibration. The free-running frequency of ILRO in proposed demodulator is changed from 1.7 to 2.55 MHz over a temperature and supply ranges of  $-20^\circ\text{C}$  to  $80^\circ\text{C}$  and 0.85 V to 1.15 V respectively along with three different process corners, as shown in Fig. 9 (a). However, by adjusting  $V_{CS}$ , the free oscillation frequency can be moved closer to 2 MHz for various process corners such as FF ( $V_{DD}=1.15\text{ V}$ ), TT ( $V_{DD}=1.0\text{ V}$ ), SS ( $V_{DD}=0.85\text{ V}$ ) as shown in Fig. 9 (b).

Fig. 10 shows the Cadence Spectre simulation results that plot the phase differences between injection signal and the output signal of each of the delay stages. The free-running frequency of ILRO is designed at 2 MHz and an approximately 25 % duty cycled injection signal is used. Fig. 10 (a) shows the output signal of each node in the injection locked state with the 1.875 MHz injection

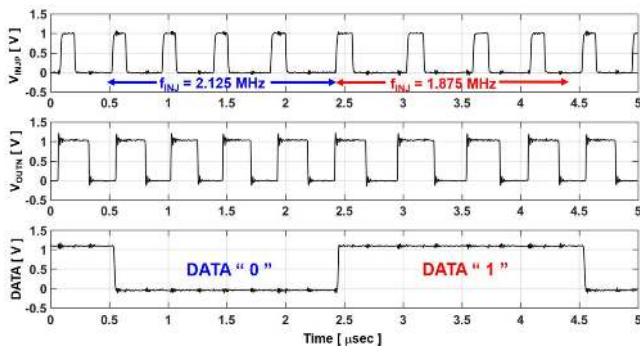


FIGURE 11. Measured GFSK demodulator responses.

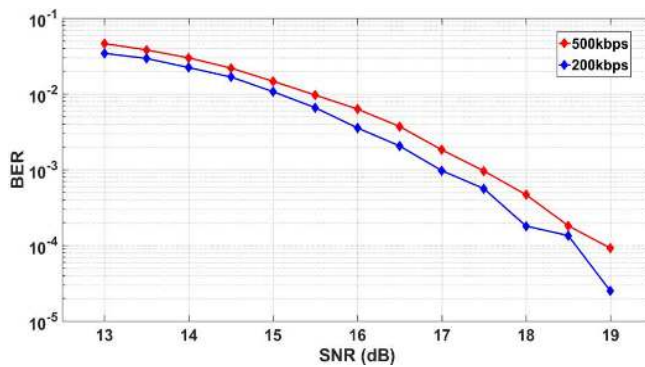


FIGURE 12. Measured BER performances of the GFSK demodulator.

signal. From simulation, it can be seen that the phase shift of the delay cell has a phase shift  $\zeta$  is  $43.2^\circ$  and  $\zeta'$  is  $50.4^\circ$ . Thus, the values  $\theta$  and  $\phi$  can be evaluated as  $1.8^\circ$  and  $7.2^\circ$  respectively. When ILRO is locked to the 2.125 MHz signal as shown in Fig. 10 (b), the phase shift  $\psi$  is  $46.8^\circ$  and  $\psi'$  is  $39.6^\circ$ . In this case also, the values  $\theta$  and  $\phi$  can be evaluated as  $1.8^\circ$  and  $7.2^\circ$  respectively as expected from (2), (3) and (4). In this implementation, the outputs are taken from the second stage delay cells. When the injection frequency is lower than the free-running frequency, based on the simulation results, the phase difference of the second delay cell output and the injection signal is  $313.2^\circ$  from (5). In other words, the rising edge of second stage delay cell output is  $46.8^\circ$  ahead of the sampling edge of  $V_{INJP}$ . Since  $PD_2$  is lower than  $360^\circ$  (or  $2\pi$ ), the output is sampled as logic-high. When the injection frequency is higher than free-running frequency, the phase difference  $PD_2$  is  $406.8^\circ$  from (6). The rising edge of second stage delay cell output is  $46.8^\circ$  lag to  $V_{INJP}$ . Since  $PD_2$  is higher than  $360^\circ$  (or  $2\pi$ ), the output is sampled as logic-low.

Fig. 11 shows the measured input and output waveforms of the ILRO in the proposed demodulator and the data waveform demodulated through the D-flip flop using and injection signal of 25 % duty cycle. It can be seen that when the injection frequency is 2.125 MHz, the output is sampled as a logic-low. Similarly, when the injection frequency is 1.875 MHz, the output is sampled as a logic-high. In order to measure the BER performance, GFSK signal with AWGN (Additive White

TABLE III  
PERFORMANCE COMPARISON

	[7]	[8]	[9]	[10]	This work
Tech [ $\mu\text{m}$ ]	0.18	0.18	0.18	0.13	0.18
Supply [ V ]	0.5	1.8	1.8	1.2	1.0
Max. Data-rate [ Mbps ]	1	1	0.25	1	0.5
IF [ MHz ]	3	3	2	1	2
SNR [ dB ]	18.7	16.5	16.7	14.4	17.5 @ 0.5 kbps 16.9 @ 0.2 kbps
Power [ $\mu\text{W}$ ]	200	918	630	170	2.7
Energy Efficiency [ pJ/bit ]	200	918	2520	170	5.4
Area [ $\text{mm}^2$ ]	0.36	0.08	0.14	0.05	0.012

Gaussian Noise) and frequency deviation of  $\pm 125$  kHz is applied to the demodulator by using signal generator, SMW200A of ROHDE & SCHWARZ. As shown in Fig. 12, the demodulator achieves an input SNR of 17.5 dB equivalent to a BER of 0.1 % at a data rate of 500 kbps. At 200 kbps, the SNR improves to 16.9 dB.

Table III compares the performance of recently proposed GFSK demodulators with the proposed architecture. In comparison to [4]-[7] the proposed demodulator consumes significantly lesser power achieving energy efficiency at least 30 times better. The overall silicon area is 4 times smaller, thanks to its simple structure arising from the ILRO based approach. The energy efficiency and the area can be further improved by implementing the proposed modulator in a more advanced process node due to its digital intensive nature.

## V. CONCLUSION

In this paper, a novel GFSK demodulator based on an injection ring oscillator suitable for low-IF receiver architecture is presented. The proposed approach is digital-intensive enabling ultra-low power operation. The measured results show that the proposed demodulator can accurately demodulate GFSK signals with a simple structure. Furthermore, ultra-low power consumption and small active area of the architecture enables its use in many low power low cost wireless communication systems for IoT and MICS applications.

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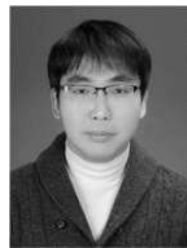


**SOONYOUNG HONG** (S’17) received the B.S. and M.S. degrees in electrical engineering from the Chungnam National University, Daejeon, South Korea, in 2006 and 2008, respectively. He is currently working toward the Ph.D. degree in information and communication engineering from the Daegu Gyeongbuk Institute of Science and Technology (DGIST). His current research interests include wireless transceiver design for ultra-low power applications using CMOS technologies. He is also interested in sensor interface circuits for wireless sensor network (WSN).



**ARUP K. GEORGE** (S’12-M’17) received the B.Tech. degree in electronics and communication engineering from Cochin University of Science and Technology, India, in 2003. He was a senior staff engineer at Nvidia Graphics India, developing image and video firmware for their mobile platform SoCs. He received the M.Sc. degree in Electronics and Communication Engineering with Distinction from the University of Glasgow, Glasgow, U.K., in 2010. He received the Ph.D. degree in Electrical and Electronic

Engineering from Nanyang Technological University, Singapore. Currently, he is a Research Professor at the Department of Information and Communication Engineering at Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea. His research interests include sensor interface circuits for ultra-low-power biomedical and sensor node applications.



**DONGGU IM** (S’09-M’13) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2004, 2006, and 2012, respectively. From 2006 to 2009, he was an Associate Research Engineer with LG Electronics, Seoul, Korea, where he was involved in the development of universal analog and digital TV receiver ICs. From 2012 to 2013, he was a Post-Doctoral Researcher with KAIST, where he was

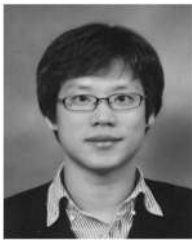
involved in the development of the first RF SOI CMOS technology in Korea with SOI business team in National NanoFab Center (NNFC), Daejeon, Korea, and was responsible for the design of antenna switch, digitally tunable capacitor, power MOSFETs, and ESD devices. In 2013, he joined the Texas Analog Center of Excellence (TxACE), Department of Electrical Engineering, University of Texas at Dallas, as a Research Associate, where he developed ultra-low-power CMOS radios with adaptive impedance tuning circuits. In 2014, he joined the Division of Electronics Engineering, Chonbuk National University, Jeollabuk-do, Korea, and is now an Associate Professor. His research interests are CMOS RF/mm-wave ICs and system design for wireless communications.



**MINKYU JE** (S’97-M’03-SM’12) received the M.S. and Ph.D. degrees, both in Electrical Engineering and Computer Science, from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1998 and 2003, respectively.

In 2003, he joined Samsung Electronics, Giheung, Korea, as a Senior Engineer and worked on multi-mode multi-band RF transceiver SoCs for GSM/GPRS/EDGE/WCDMA standards. From 2006 to 2013, he was with Institute of Microelectronics (IME), Agency for Science, Technology and Research (A\*STAR), Singapore. He worked as a Senior Research Engineer from 2006 to 2007, a Member of Technical Staff from 2008 to 2011, a Senior Scientist in 2012, and a Deputy Director in 2013. From 2011 to 2013, he led the Integrated Circuits and Systems Laboratory at IME as a Department Head. In IME, he led various projects developing low-power 3D accelerometer ASICs for high-end medical motion sensing applications, readout ASICs for nanowire biosensor arrays detecting DNA/RNA and protein biomarkers for point-of-care diagnostics, ultra-low-power sensor node SoCs for continuous real-time wireless health monitoring, and wireless implantable sensor ASICs for medical devices, as well as low-power radio SoCs and MEMS interface/control SoCs for consumer electronics and industrial applications. He was also a Program Director of NeuroDevices Program under A\*STAR Science and Engineering Research Council (SERC) from 2011 to 2013, and an Adjunct Assistant Professor in the Department of Electrical and Computer Engineering at National University of Singapore (NUS) from 2010 to 2013. He was an Associate Professor in the Department of Information and Communication Engineering at Daegu Gyeongbuk Institute of Science and Technology (DGIST), Korea from 2014 to 2015.

Since 2016, he has been an Associate Professor in the School of Electrical Engineering at Korea Advanced Institute of Science and Technology (KAIST), Korea. His main research areas are advanced IC platform development including smart sensor interface ICs and ultra-low-power wireless communication ICs, as well as microsystem integration leveraging the advanced IC platform for emerging applications such as intelligent miniature biomedical devices, ubiquitous wireless sensor nodes, and future mobile devices. He is an author of 5 book chapters and has more than 290 peer-reviewed international conference and journal publications in the areas of sensor interface IC, wireless IC, biomedical microsystem, 3D IC, device modeling and nano-electronics. He also has more than 50 patents issued or filed. He has served on the Technical Program Committee and Organizing Committee for various international conferences, symposiums and workshops including IEEE International Solid-State Circuits Conference (ISSCC), IEEE Asian Solid-State Circuits Conference (A-SSCC) and IEEE Symposium on VLSI Circuits (SOVC). He is currently working as a Distinguished Lecturer of IEEE Circuits and Systems Society.



**JUNGHYUP LEE** (S'04-M'11) received the B.S. degree in electrical and electronics engineering from Kyungpook National University, Daegu, Korea, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2005 and 2011, respectively. In 2011, he joined the Institute of Microelectronics, Agency for Science, Technology, and Research (A\*STAR), Singapore, where he was engaged in

the development of high-speed wireless transceivers for biomedical applications and reference clock generators. Since 2016, he is an Assistant Professor at the Department of Information and Communication Engineering at the Daegu Gyeongbuk Institute of Science and Technology (DGIST), Daegu, South Korea. His research interests include mixed-signal and analog circuits for low-power biomedical devices and PVT tolerant circuits.

He has served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC).