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A 1.1 V 25 ppm/°C Relaxation Oscillator with 0.045%/V Line Sensitivity for Low Power Applications

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Abstract: A fully-integrated CMOS relaxation oscillator, realized in 40 nm CMOS technology, is presented. The oscillator includes a stable two-transistor based voltage reference without an operational amplifier, a simple current reference employing the temperature-compensated composite resistor, and the approximated complementary to absolute temperature (CTAT) delay-based comparators compensate for the approximated proportional to absolute temperature (PTAT) delay arising from the leakage currents in the switches. This relaxation oscillator is designed to output a square wave with a frequency of 64 kHz in a duty cycle of 50% at a 1.1 V supply. The simulation results demonstrated that the circuit can generate a square wave, with stable frequency, against temperature and supply variation, while exhibiting low current consumption. For the temperature range from −20 °C to 80 °C at a 1.1 V supply, the oscillator' output frequency achieved a temperature coefficient (T.C.) of 12.4 ppm/°C in a typical corner in one sample simulation. For a 200-sample Monte Carlo simulation, the obtained T.C. is 25 ppm/°C. Under typical corners and room temperatures, the simulated line sensitivity is 0.045%/V with the supply from 1.1 V to 1.6 V, and the dynamic current consumption is 552 nA. A better figure-of-merit (FoM), which equals 0.129%, is displayed when compared to the representative prior-art works.

Keywords: relaxation oscillator; voltage reference; composite resistor; current reference; temperature compensation; cross-coupled pair; delay drift compensation

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1. Introduction

With the rapid development of wearable electronics and IoT (Internet of things), the demand of an on-chip and low-power oscillator has received much attention in the research. Low power consumption is especially important for IoT devices because of the real-time clock which has to stay awake all the time, even when other circuits are in sleep mode [1]. Although the crystal oscillator can provide an accurate signal with high stability, it is relatively expensive and occupies a large area with high current consumption [2]. For small size, the on-chip oscillators, such as ring oscillators and relaxation oscillators (ROSC), are widely used. Regarding to the ring oscillator, despite its simple architecture and low-power consumption under low oscillation frequency, the circuit is sensitive to process, supply, and temperature (PVT) variation [3]. This leads to a significant variation in the output frequency. Although other ring oscillators [4–6] can achieve relatively low sensitivity for output frequency, the power consumption is large. Hence, it may not be suitable for providing a stable clock using the standalone ring oscillator topology. Several reported works [7–11] have shown that the relaxation oscillator can provide a good tradeoff between frequency stability, temperature variation, and supply variation while occupying at reasonably small area. Thus, the relaxation oscillator is preferred as on-chip oscillator for those applications that require good stability with low cost and moderate precision. For example, the switched-capacitor based sensor interfaces [12,13] usually employ a low-frequency clock to control the sampling and charge transfer action in the circuits. Moreover, for the design of an instrumentation amplifier, ROSC can be applied for chopping amplifiers [14,15] to provide

the chopping signal for modulating the signal to high frequency for amplification and translating it back to baseband for analog signal processing.

Figure 1 depicts the plot of the T.C. and line sensitivity of representative relaxation oscillators against the power consumption. As can be seen, it shows a tradeoff relationship among the performance parameters in context of the frequency stability and the power consumption [16]. The same goes for line sensitivity. In order to realize a lower T.C., one previous work [17] adopted the error feedback to achieve temperature-dependent delay cancellation, while another one [18] utilized the second-order compensation with a charge pump and filter. However, these complex designs led to avoidable high power consumption. Although other designs [16,19] reduced the power to a relatively small value, their thermal stability is slightly weakened due to the timing error and the temperature-sensitive current reference, respectively. Regarding the line sensitivity, there are works [8,10] utilizing high-gain operational amplifiers to minimize the effect from the supply variation, but at the cost of higher current consumption. Although other works [9,20] employed lowered the supply voltage as well as the bias current to reduce power, the circuit topologies were subject to higher supply sensitivity. Therefore, it is challenging to achieve a good stability of output frequency with relatively low power consumption in the ROSC design.

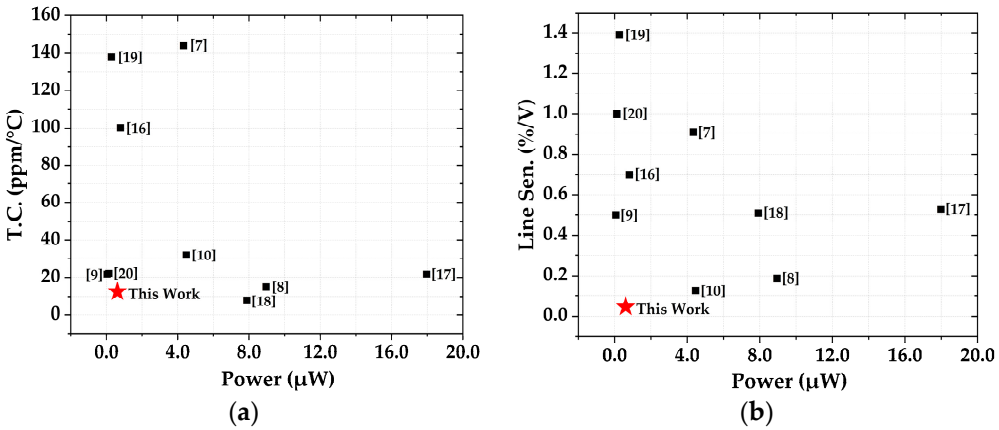
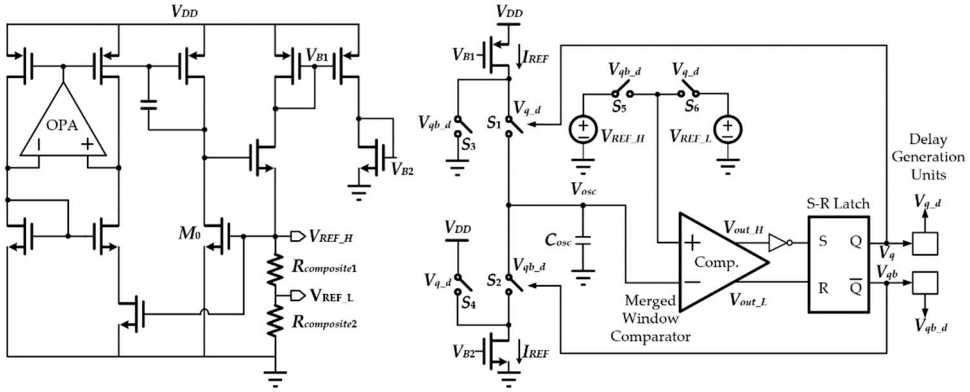


Figure 1. Tradeoff performance of reported relaxation oscillators: (**a**) T.C. versus power; (**b**) line sensitivity versus power.

In this paper, an improved relaxation oscillator with simple circuit topology is presented. As illustrated in Figure 1, the proposed ROSC features excellent stability against temperature and supply variation while achieving relatively low power consumption. This is achieved by using a simple delay drift compensation technique to enhance the thermal stability, in conjunction with the design of a simple V-I converter, which is based on two-transistor-type circuit topology to provide good immunity against the fluctuation of supply voltage change. Section 1 provides the introduction. Several representative prior-art relaxation oscillator designs are described in Section 2. Section 3 describes the design and implementation of the proposed relaxation oscillator. Section 4 presents the results and discussions. This is followed by the conclusion in Section 5.

2. Review of Reported Relaxation Oscillator

A low temperature coefficient relaxation oscillator [8] with a merged window comparator is shown in Figure 2. There are two different reference voltages (V_{REF_H} and V_{REF_L}) in the reported work. V_{REF_H} is connected to the non-inverting input of the comparator, and the voltage (V_{osc}) across the capacitor is initially zero. The capacitor (C_{osc}) is first charged by I_{REF} until V_{osc} reaches V_{REF_H}. Then C_{osc} starts to discharge with constant current I_{REF} while V_{REF_L} is connected to the comparator. When V_{osc} is lower than V_{REF_L}, C_{osc} is charged, and V_{osc} is again compared with V_{REF_H}. The delay generation units prevent the oscillator from entering metastability.



(**a**) (**b**)

Figure 2. A CMOS relaxation oscillator with a merged window comparator: (**a**) reference generator; (**b**) block diagram.

The voltage reference is based on the architecture improved from the threshold monitoring circuit [21] that can effectively compensate for the temperature effect. Moreover, the reference current is also derived from the same reference voltage, in association with the optimized series/parallel composite resistor. As a result, this leads to the output frequency with low T.C. The merged window comparator is able to cancel out the offset of the comparator arising from the component mismatch effect. As such, this allows the T.C. of output frequency to maintain a good value, even if there is a 10 mV offset in the analog-based comparator, for example. However, the transistor M_0 in the reference generator needs to work in a saturation region, thus, for reliable temperature compensation, the current flowing through it is not allowed to be reduced to a small value. At this juncture, an operational amplifier is also utilized to provide a high loop gain to minimize the circuit sensitivity with respect to the supply variation. This suggests an additional current consumption source. Therefore, high current consumption becomes the main limitation of this circuit technique.

Another relaxation oscillator [9] that provides good a T.C. of output frequency while maintaining low power consumption, is depicted in Figure 3. This oscillator starts when ϕ is logic low. At the beginning, current I_2 flows though resistor R to generate the reference voltage at the non-inverting input of the comparator, and capacitor C_1 is charged by constant current I_1. After the voltage across C_1 becomes bigger than the reference voltage, ϕ transits to logic high; thus, the capacitor C_2 begins to be charged, and the reference voltage is connected to the inverting input of the comparator until the charging operation for C_2 is completed to make ϕ logic low again.

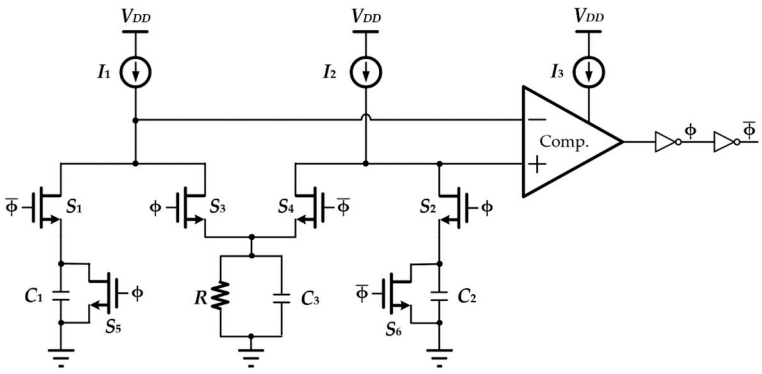


Figure 3. A Relaxation Oscillator with Ultra-Low Power Consumption.

In this work, the currents I_1 and I_2 can be reused at different phases, and only one comparator [22] is needed. All the currents, including the bias current for the comparator, can be achieved from one current source, hence the current consumption is minimized. Because the reference voltage is connected to different inputs of the comparator at different

phases, the offset of the comparator increases the period at one phase, while decreasing the period at another phase. Thus, the offset can be cancelled out as long as the two capacitors are identical and the two charging currents are assumed the same. However, because of the restricted drain-to-source voltage headroom for each transistor working in a low supply environment, the transistor is subject to more stressing, resulting in not having good matching characteristics. On top of that, the mismatch effect between I_1 and I_2 is unavoidable. The current mismatch leads to the residual offset of the comparator that cannot be cancelled out completely. Ultimately, an error in the reference voltage exists between the different phases.

Another relaxation oscillator [10], with a self-chopped technique to achieve good stability against temperature and supply variations, is depicted in Figure 4. A current-mode comparator [23] is used to compare the voltage (V_r) across the composite resistors and the voltage (V_c) across the capacitor. Initially, V_c, V_{cmp}, and V_{rst} are logic low, and the capacitor is charged by constant current I_r until V_c becomes larger than V_r to change V_{cmp} from low to high, which causes V_{rst} to transition to high to discharge the capacitor. After the discharge action has been completed, V_{cmp} and V_{rst} become low to allow the current I_r to charge the capacitor again.

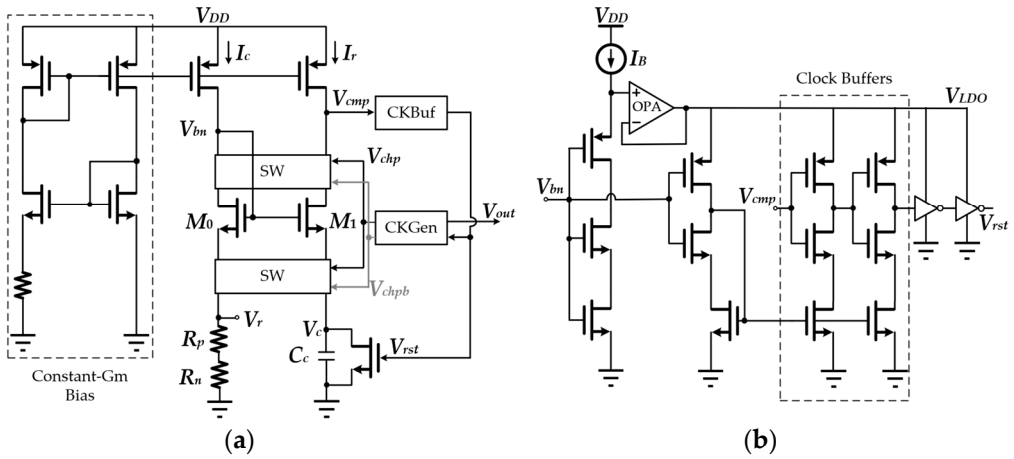


Figure 4. A self-chopped relaxation oscillator with adaptive supply generation: (**a**) block diagram; (**b**) clock buffer.

In this design, the ratio between I_c and I_r is independent of temperature and supply variations, and the temperature effect on the metal-oxide-metal (MoM) capacitor is negligible. In addition, the offset voltage in transistors M_0 and M_1 can be cancelled out by flipping M_0 and M_1 at every half cycle. Therefore, a good T.C. and good line sensitivity of the output frequency can be obtained due to good thermal stability through the use of a stable composite resistor and capacitor, in conjunction with offset cancellation using the chopping technique. However, it may be difficult to reduce the current consumption due to the operational amplifier which exhibits good transient response for powering the fast-switching clock buffers and the need for a complicated replica-biasing circuit. Hence, this design also suffers from the problem of relatively high supply current consumption.

3. Proposed Relaxation Oscillator

3.1. Topology of the Relaxation Oscillator

The relaxation oscillator, which makes use of the reported topology [24], is depicted in Figure 5. The major difference is that of the design and implementation of the current reference I_{REF}, while the lower supply current consumption is further addressed in the proposed work. The oscillator comprises a reference generator, two comparators (Comp. 1 and Comp. 2), an S-R latch, four switches, and two capacitors (C_1 and C_2). The reference generator generates a stable reference voltage (V_{REF}) and a reference current (I_{REF}), charging two capacitors with a constant current.

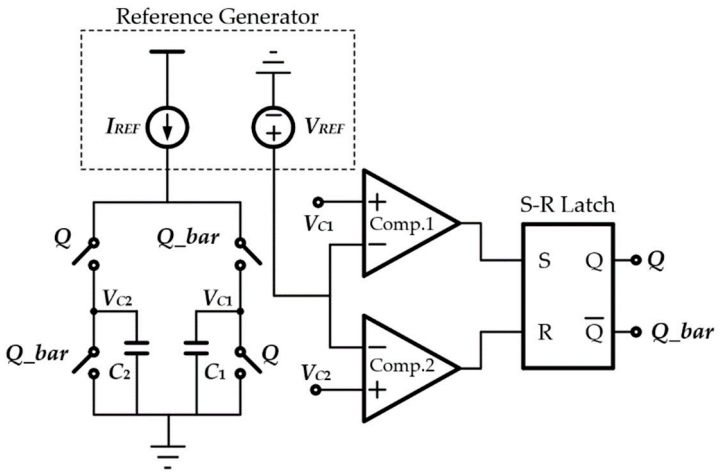


Figure 5. Block diagram of relaxation oscillator.

Note that the relaxation oscillator circuit starts when Q is logic low, and the voltages across two capacitors are initially zero. At the beginning, the outputs of two comparators are low, and C_1 is charged by I_{REF}. After the voltage (V_{C1}) across C_1 reaches V_{REF}, the output of Comp.1 transits to high, which allows Q to become high and Q_bar to become low. Then C_1 starts to discharge, while C_2 is charged by I_{REF}. The inputs of the SR latch are both low when I_{REF} is charging C_2, so that the outputs of the SR latch remain constant until the voltage (V_{C2}) rises to V_{REF}. At this juncture, Q transits to low, while Q_bar transits to high, allowing C_1 to be charged again and C_2 to discharge. The output Q of the SR latch will generate a rail-to-rail square wave with the desired frequency. As capacitors are charged by a constant current, the duration of the high level and low level of the square wave are dependent on the charging time of each capacitor; hence, the 50% duty cycle can be achieved by using two identical capacitors. The output frequency can be expressed as

$$f_{ROSC} = \frac{I_{REF}}{2CV_{REF}} \tag{1}$$

where f_{ROSC} is the output frequency, and C is the capacitance of C_1 and C_2. From (1), the accuracy of the output frequency is dependent on the accuracy of V_{REF} and I_{REF}. From the design considerations, the reference generator and the comparator are the key components in circuit design. Two nonideal effects exist in the relaxation oscillator circuit. They are the delay and offset of the comparator. Regarding the comparator's delay, it is not critical because of the low frequency specification and the moderate precision requirement in its application. With a careful designing of the comparator, the temperature-dependent delay of the comparator can be minimized to cause less impact to the circuit, and ultimately, on the output frequency. Pertaining to the comparator's offset, it is also addressed in the design phase with an appropriate choice of critical device sizes so that the offset effect to the circuit is acceptable, without significantly jeopardizing the oscillator's performance.

3.2. Reference Generator

The reference generator, which provides both the reference voltage (V_{REF}) and the reference current (I_{REF}), is depicted in Figure 6. The reference voltage generator is based on the two-transistor topology [25] and the cascode current mirror. This is achieved by employing voltage-to-current and current-to-voltage conversions to produce V_{REF}. This is then followed by another voltage-to-current converter with a composite resistor [26] and V_{REF} to generate the reference current I_{REF}.

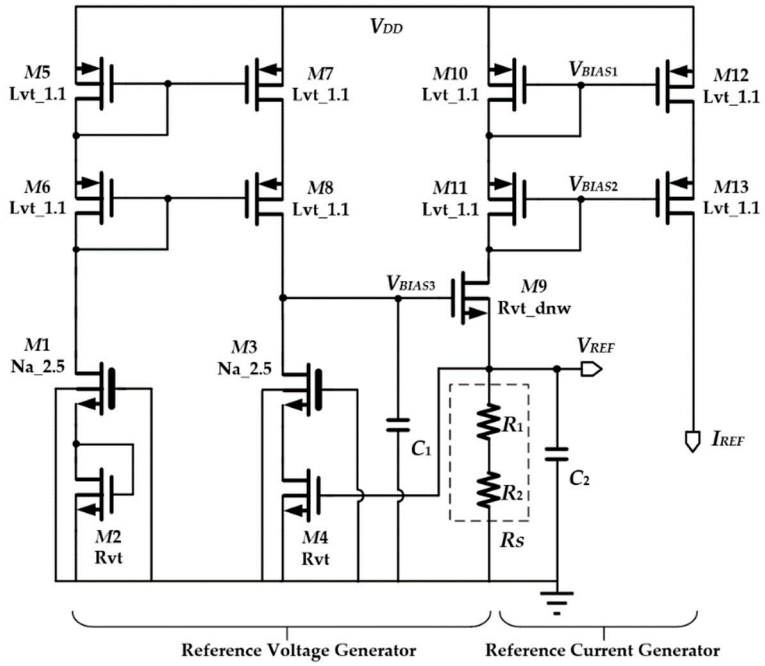


Figure 6. Proposed reference voltage and reference current generator.

Regarding the reference voltage generator, M_1, M_2, M_3, and M_4 work in the weak inversion region, where M_1 and M_3 are identically designed native transistors with a negative threshold voltage, whereas M_2 and M_4 are identical standard transistors. It is given that, for a sub-threshold biased MOSFET, its drain current is

$$I_{sub} = \mu C_{OX}(\eta - 1){V_T}^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left[1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right] \tag{2}$$

where μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, η is the subthreshold slope factor, V_T is the thermal voltage, W is transistor's channel width, L is transistor's channel length, V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage, and V_{DS} is the drain-to-source voltage. When V_{DS} is larger than 100 mV (4 V_T), the effect of V_{DS} on I_{sub} is negligible; hence, the current I_{sub} can be approximated as

$$I_{sub} \approx \mu C_{OX}(\eta - 1){V_T}^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \tag{3}$$

Since the currents in M_1 and M_2 are the same, we can obtain

$$\begin{aligned} I_{sub} &= \mu_1 C_{OX1}(\eta_1 - 1){V_T}^2 \frac{W_1}{L_1} \exp\left(\frac{V_{GS_1} - V_{TH1}}{\eta_1 V_T}\right) \\ &= \mu_2 C_{OX2}(\eta_2 - 1){V_T}^2 \frac{W_2}{L_2} \exp\left(\frac{V_{GS_2} - V_{TH2}}{\eta_2 V_T}\right) \end{aligned} \tag{4}$$

The current of M_1 and M_2 is the same as that of M_3 and M_4 due to the identical current copying action in the cascode current mirror M_5–M_8. Hence, the V_{GS} of M_2 is identical to that of M_4, which is the V_{REF}. When the gates of M_1 and M_3 are connected to a ground, it suggests that the V_{GS} of M_1 and M_3 are identical negative reference voltages. Thus, V_{REF} can be obtained as

$$V_{REF} = -V_{GS1} = V_{GS2} = \frac{\eta_1 \eta_2}{\eta_1 + \eta_2}(V_{TH2} - V_{TH1}) + \frac{\eta_1 \eta_2}{\eta_1 + \eta_2} V_T \ln\left(\frac{\mu_1 C_{OX1} W_1 L_2}{\mu_2 C_{OX2} W_2 L_1}\right) \tag{5}$$

In this design, the first-order temperature effect on V_{TH} is given as [7]

$$V_{TH} = V_{TH0} - \kappa T \tag{6}$$

where V_{TH0} is the threshold voltage at room temperature (300 K), and κ is the temperature coefficient of the threshold voltage. Therefore, the T.C. of V_{REF} is as follows:

$$TC_{V_{REF}} = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T} = \frac{(\kappa_1 - \kappa_2) + \frac{k}{q} \ln\left(\frac{\mu_1 C_{OX1} W_1 L_2}{\mu_2 C_{OX2} W_2 L_1}\right)}{(V_{TH20} - V_{TH10}) + (\kappa_1 - \kappa_2) T + \frac{k}{q} T \ln\left(\frac{\mu_1 C_{OX1} W_1 L_2}{\mu_2 C_{OX2} W_2 L_1}\right)} \tag{7}$$

where k is the Boltzman constant, and q is the electronic charge. In (7), the temperature effect on μ is ignored. By selecting appropriate aspect ratios of M_1 and M_2, while M_3 and M_4 remain the same size as M_1 and M_2, respectively, the temperature compensation can be achieved to permit V_{REF} in the first-order temperature compensation. Finally, it yields

$$V_{REF} = \frac{\eta_1 \eta_2}{\eta_1 + \eta_2} (V_{TH20} - V_{TH10}) \tag{8}$$

In addition, the V_{REF} has a good power supply rejection (PSR) at low frequency. Since the effect of ΔV_{DD} on the flowing currents, M_2 and M_4 are negligible, as long as their V_{DS} values are larger than 100 mV, while the transistors have a long channel length to reduce the drain-induced barrier lowering (DIBL) effect on V_{TH1}~V_{TH4}. Besides, the negative feedback formed by M_3, M_4, and M_9 can further stabilize V_{REF}.

For the reference current, it is produced by V_{REF} driving a temperature-compensated composite resistor (R_s). Of particular note, R_s comprises the series connection of an n-poly resistor (R_n) and a p-poly resistor (R_p), where R_n is PTAT and R_p is CTAT. The T.C. of R_p, R_n, and R_s are given as follows:

$$TC_{Rp} = \frac{1}{R_p} \frac{\partial R_p}{\partial T} \tag{9}$$

$$TC_{Rn} = \frac{1}{R_p} \frac{\partial R_n}{\partial T} \tag{10}$$

$$TC_{Rs} = \frac{1}{R_p + R_n} \frac{\partial (R_p + R_n)}{\partial T} \tag{11}$$

Substituting (9) and (10) into (11), TC_{Rs} can be rewritten as

$$TC_{Rs} = \frac{R_p}{R_p + R_n} TC_{Rp} + \frac{R_n}{R_p + R_n} TC_{Rn} \tag{12}$$

where TC_{Rp} is negative and TC_{Rn} is positive. Thus, TC_{Rs} can be made zero when choosing R_p/R_n equal to $|TC_n/TC_p|$. This indicates that R_s can be independent of the first-order temperature effect. Therefore, the temperature-insensitive reference current (I_{REF}) can be obtained with the temperature-insensitive voltage and the composite resistor.

$$I_{REF} = \frac{V_{REF}}{R_s} = \frac{\eta_1 \eta_2 (V_{TH20} - V_{TH10})}{(\eta_1 + \eta_2)(R_p + R_n)} \tag{13}$$

Moreover, since R_s is independent of V_{DD}, V_{REF} is insensitive to the change in V_{DD}. As a result, I_{REF} is also insensitive to the supply variations.

As seen in Figure 6, the capacitor C_1 is used as a frequency compensation for the negative feedback loop which is formed by M_3, M_4, and M_9. In addition, the capacitor C_2 is used to stabilize V_{REF} when the switches in Figure 4 are turned on and off. This is because the voltage change will be coupled to the gate of M_9 by the parasitic capacitors.

The current mirror pairs M_5–M_8 and M_{10}–M_{13} have a long channel length to reduce the current mismatch.

The 1.1 V supply voltage of this reference generator can ensure that all transistors still work in the proper region when there is a 10% supply voltage drop, but if the supply continuously decreases below 1 V, there will not be adequate V_{DS} headroom for the current mirror pair in Figure 6 at the SS corner under a low temperature, due to the increase in V_{TH}.

Finally, the size of each component pertaining to Figure 5 in the reference generator is listed in Table 1.

Table 1. Size of components in the reference generation.

Component	Size	Component	Size
$M_{1,3}$	10/15 (μm/μm)	$M_{10,12}$	28/12 (μm/μm)
M_2	2.04/1 (μm/μm)	$M_{11,13}$	7/2 (μm/μm)
M_4	2.05/1 (μm/μm)	R_1	433.3 kΩ
$M_{5,7}$	5/4 (μm/μm)	R_2	1.366 MΩ
$M_{6,8}$	6/2 (μm/μm)	C_1	1.5 pF
M_9	1.5/1 (μm/μm)	C_2	4 pF

3.3. Comparator

The comparator in Figure 7 shows an OTA topology using dual cross-coupled load pairs and a cascode arrangement to boost the overall gain. The front differential stage, which makes use of the cross-coupled load pairs, M_3–M_6 and M_{13}–M_{16}, is used to produce gain enhancement as well as to reduce the delay in the comparator, the outputs of which are followed by the current mirror high-gain stage consisting of M_7–M_{12} and M_{15}–M_{20}. Finally, the CMOS inverter, formed by M_{23} and M_{24}, aims to sharpen the output square waveform and provide the driving capability of the comparator.

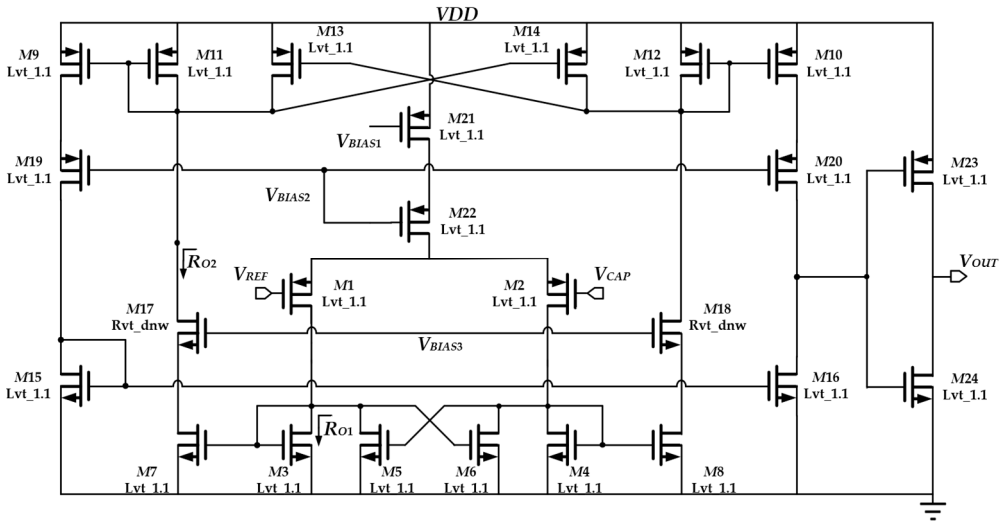


Figure 7. Proposed comparator.

Considering the cross-coupled pairs M_3–M_6, the aspect ratio of M_3 is larger than that of M_5. In small-signal analysis, the output impedance is obtained as

$$R_{O1} = \frac{r_{O3} + r_{O5}}{(g_{m3} - g_{m5})(r_{O3} + r_{O5}) + 1} \approx \frac{1}{g_{m3} - g_{m5}} \tag{14}$$

where g_{mi} is the respective transistor's transconductance and r_{Oi} is the respective transistor's output resistance, with i = 3 or 5. From (14), R_{O1} is increased from $1/g_{m3}$ to $1/(g_{m3}–g_{m5})$ to increase the voltage gain because of the positive feedback allowing M_5 to behave as a negative resistance. When there is a voltage change on the drain of M_3,

the positive feedback introduced by M_5 can accelerate this change, causing faster output response to reduce the delay in the comparator.

The four cascode transistors M_{17}–M_{20} are used to reduce the effect of supply variation ΔV_{DD} on the delay in the comparator. For M_7 and M_{17} in small-signal analysis, the change in V_{DS7} caused by ΔV_{DD} can be approximated as [27]

$$\Delta V_{DS7} \approx \frac{\Delta V_{DD}}{g_{m17} r_{O17}} \tag{15}$$

As interpreted from (15), it indicates that the change in V_{DS} on M_7–M_{10} can be ignored when V_{DD} varies. This means the current change in each branch caused by channel length modulation and DIBL can be minimized with cascode transistors. Moreover, the bias current for the comparator is directly copied from I_{REF}, with the cascode current mirror in different ratios. This avoids the need for an extra bias branch, which would cause an increase in supply current consumption.

In fact, when the constant bias current is applied to the comparator, the delay in the comparator is reduced with an increasing temperature. From (3) and (6), the V_{GS} of the MOS transistor working under weak inversion is expressed as

$$V_{GS} = \eta V_T \ln\left[\frac{I_{sub}}{\mu C_{OX}(\eta - 1)V_T^2 \frac{W}{L}}\right] + V_{TH0} - \kappa T \tag{16}$$

It can be observed that the V_{GS} exhibits CTAT behavior. M_3 is in the diode connection, meaning that V_{DS3} is equal to V_{GS3}. When the temperature increases, V_{DS3} (or V_{GS3}) in the diode-connected topology is significantly reduced with respect to V_{DS7}. Thus, the mismatch between the drain-to-source voltage of the transistors can lead to a rising current to allow for the delay in the comparator to decrease from 285.3 ns to 278.8 ns as the temperature increases, as shown in Figure 8. This feature is particularly useful for the delay compensation arising from the observation of the increase in delay through the leakage current of the switches, as depicted in Figure 4. As a result, the thermal stability of the oscillator circuit is enhanced. This will be further discussed in the next subsection. Of particularly note, the leakage current in the advanced technology node can be a serious issue.

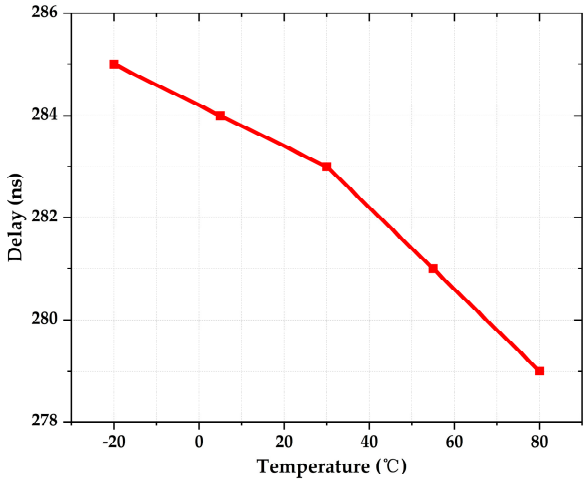


Figure 8. Temperature characteristics of delay in comparators.

Since offset is critical in the comparator design, the Monte Carlo simulation, with 400 samples for the offset evaluation, is shown in Figure 9. This result indicates that the mean offset of the comparator is 0.37 mV, and its standard derivation is 5.63 mV. As observed, the offset is minimized by sizing the input transistor pair and the cross-coupled pairs with a long channel length ($L > 4L_{min}$). Although the parasitic capacitors

in the large-size transistors will enlarge the response time, the delay, which is around 0.28 µs, including the hysteresis, contributes 3.6% of the oscillation period. Therefore, it is considered acceptable, with a low output frequency and a moderate precision requirement. Based on the result, the comparator offset cancellation scheme is not implemented in this work. The sizes of each component pertaining to the comparator in Figure 6 are given in Table 2.

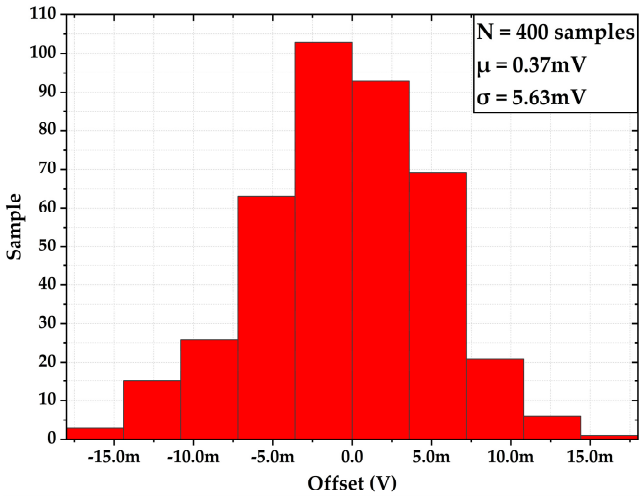


Figure 9. Monte Carlo simulation of the comparator's offset.

Table 2. Size of the components in the comparator.

Component	Size	Component	Size
$M_{1,2}$	1/0.6 (µm/µm)	$M_{15,16}$	0.5/0.6 (µm/µm)
$M_{3,4}$	1/1.2 (µm/µm)	$M_{17,18}$	0.3/0.3 (µm/µm)
$M_{5,6}$	0.8/1.2 (µm/µm)	$M_{19,20}$	0.3/0.3 (µm/µm)
$M_{7,8}$	0.5/0.6 (µm/µm)	M_{21}	20/12 (µm/µm)
$M_{9,10}$	0.5/0.6 (µm/µm)	M_{22}	5/2 (µm/µm)
$M_{11,12}$	1/1.2 (µm/µm)	M_{23}	0.36/0.12 (µm/µm)
$M_{13,14}$	1.2/1.2 (µm/µm)	M_{24}	0.12/0.12 (µm/µm)

3.4. Leakage Current in Switches and Delay Compensation

The four switches controlling the charging and discharging actions, as depicted in Figure 5, are arranged in the inverted style, as shown in Figure 10.

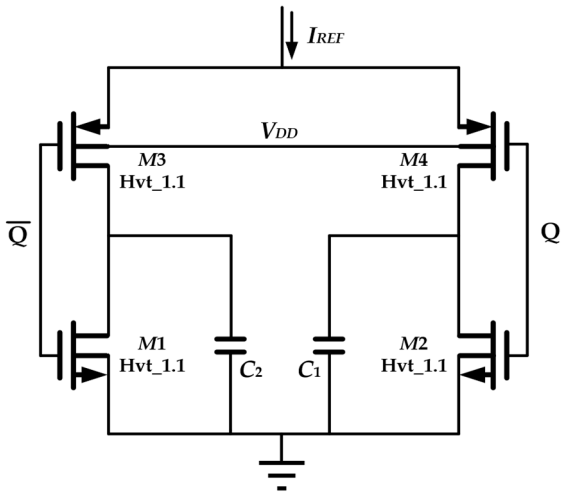


Figure 10. Four transistor switches for charging and discharging the matched capacitor pair.

Since I_{REF} is quite small, the leakage currents in the advanced technology node, flowing through the switch transistors, can be significant when charging C_1 and C_2. With the increase in temperature, the delay caused by the transistor switches is increased from 1.9 ns to 9.8 ns, as shown in Figure 11, and this effect is particularly pronounced. Therefore, this will cause the reduction in the output frequency. Thus, according to the reverse short-channel effect, high threshold-voltage transistors with the smallest channel length can be used as switches. This is also in conjunction with introducing the body effect in pmos to maximize the threshold voltage. Finally, the leakage current effect can be reduced by introducing the CTAT delay, as discussed in Section 3.3, such that the output frequency can be kept constant. The size of each transistor and capacitor shown in Figure 10 are given in Table 3.

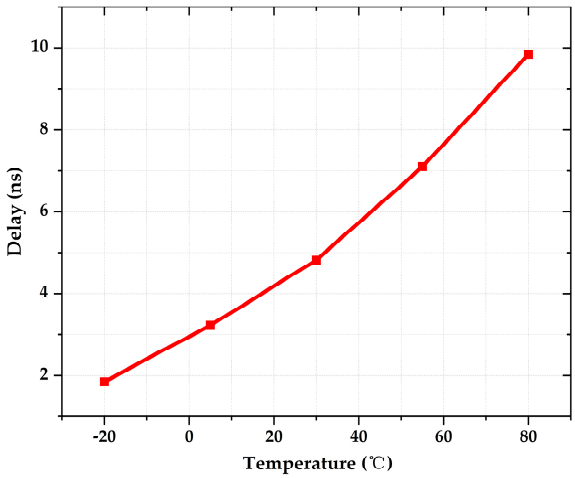


Figure 11. Temperature characteristics of the delay in transistor switches.

Table 3. Size of components in Figure 10.

Component	Size	Component	Size
$M_{1,2}$	0.12/0.04 (μm/μm)	$C_{1,2}$	1.49 pF
$M_{3,4}$	0.36/0.04 (μm/μm)		

4. Results and Discussions

The proposed ROSC, with leakage current compensation, is simulated using TSMC-40 nm CMOS process technology. The output frequency is 64.59 kHz at V_{DD} = 1.1 V under room temperature, and the transient simulation result of the output signal is depicted in Figure 12. All analog-biased transistors in the proposed ROSC work in the subthreshold region, the bias current of the comparators can be made small for low frequency design, and the current derives from the dedicated I_{REF} instead of from the addition of an extra current source. This permits the current consumption of 552 nA at room temperature in a typical corner. However, there is always a performance tradeoff between I_{REF} and low current consumption.

Figures 13 and 14 illustrate the respective simulation results of the output frequency against the temperature variation from −20 °C to 80 °C at different supply voltages and process corners. The T.C. of the output frequency of the proposed ROSC is obtained as 12.4 ppm/°C, 13.3 ppm/°C, and 21.8 ppm/°C at the TT corner, SS corner, and FF corner, respectively, at a 1.1 V supply. Regarding the 1 V supply, the obtained T.C. is 14.3 ppm/°C, 26.7 ppm/°C, and 22.2 ppm/°C, respectively. Of particular note, the T.C. is observed with some degradation at the 1 V supply with respect to that of the 1.1 V supply at the SS corner. This is mainly because the transistors in the reference generator are stressed under limited V_{DS}. Therefore, the proposed ROSC can still work properly when the supply is slightly lower than 1.1 V. Considering the operation margin, 1.1 V is regarded as the minimum

supply voltage for the oscillator. Regarding the low T.C. values achieved by the ROSC with respect to those of prior-art works, the T.C. improvement is attributed to the compensation for the delay drift resulting from temperature, as seen in Figures 8 and 11. By calculation, without the delay compensation, this T.C. will increase to about 19.1 ppm/°C.

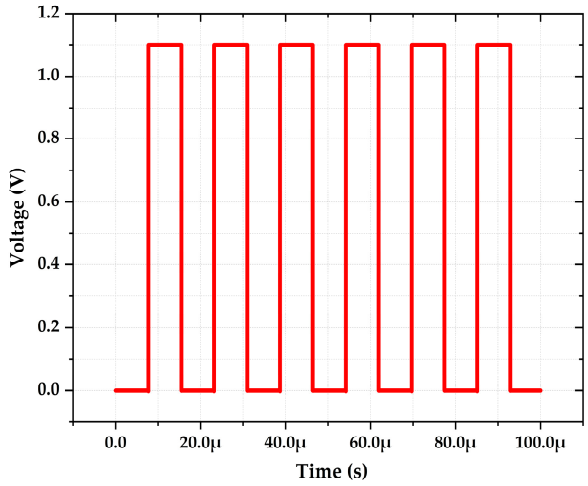


Figure 12. Output signal in time domain.

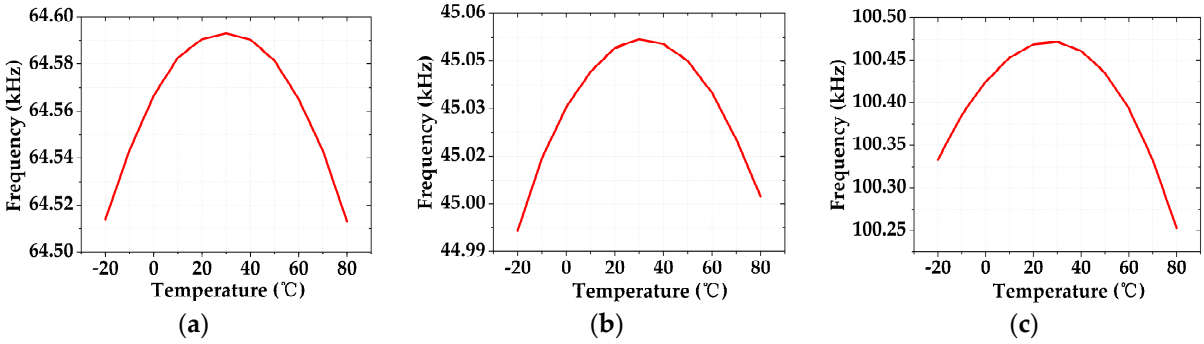


Figure 13. Temperature characteristic of output frequency at different process corners under the 1.1 V supply: (**a**) @TT corner; (**b**) @SS corner; (**c**) @FF corner.

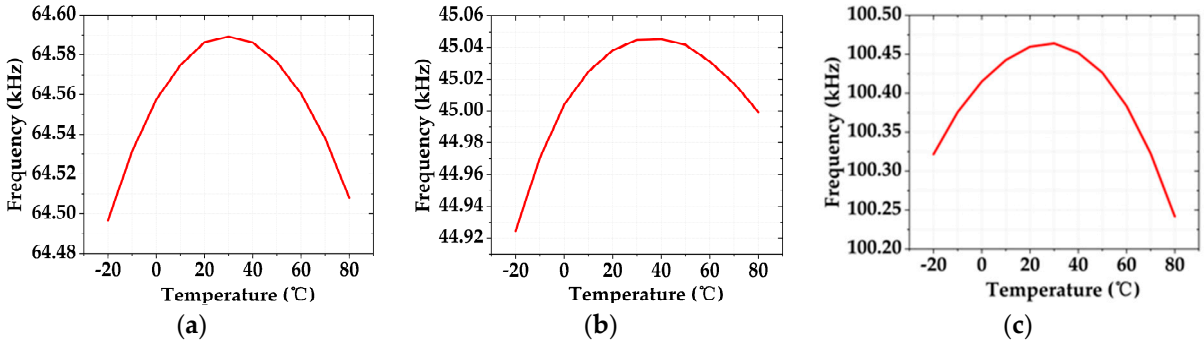


Figure 14. Temperature characteristic of output frequency at different process corners under the 1 V supply: (**a**) @TT corner; (**b**) @SS corner; (**c**) @FF corner.

Considering the parasitic effect arising from the layout issues, some model capacitors ranging from a few tens to one hundred fF are intentionally added to the critical points in each comparator, reference generator, and SR latch. The comparator displays relatively higher sensitivity due to the low bias current, while there is no significant effect from other nodes. Figure 15 shows the simulated temperature characteristic of output frequency with

intentionally added parasitic capacitors in the design under the TT corner. Of particular note, the estimated capacitance from the routing for each comparator is around 18fF. Therefore, the total capacitance of several model capacitors being added in each comparator is modeled as 20 fF. The output frequency changes from 64.59 kHz to 64.04 kHz, and the T.C. is degraded from 12.4 ppm/°C to 13.7 ppm/°C. This confirms that the potential parasitic effect arising from the layout made no significant impact on the current simulation results, without incorporating layout due to the low-frequency design. Additionally, the silicon area of this design is approximated as about 4x the total active area of the components. This yields about 0.0234 mm^2, or 153 µm × 153 µm.

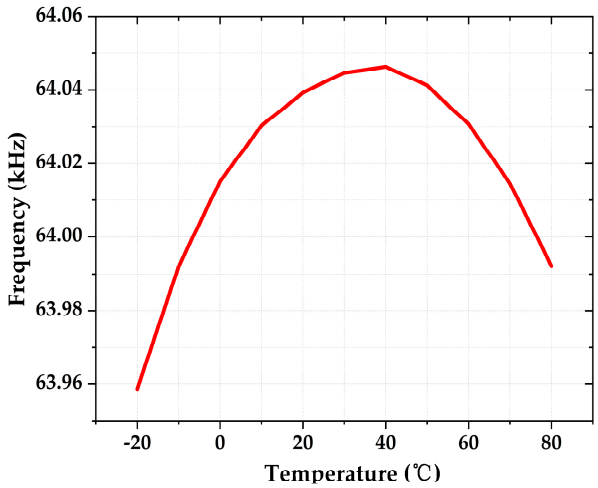


Figure 15. Temperature characteristic of output frequency with simulated parasitic capacitors at the TT corner.

The T.C. results of Monte Carlo simulation used to verify the impact of mismatch and process variations are shown in Figure 16. There are 200 samples simulated, and each sample is simulated with 11 temperature points, from −20 °C to 80 °C, resulting in 2200 points in total. The T.C. varies from 9.35 ppm/°C to 77.13 ppm/°C, with an average value of 25 ppm/°C and a standard deviation of 11.1 ppm/°C, where 75% of the samples present a T.C. smaller than 30 ppm/°C. This confirms that the output frequency of the proposed ROSC exhibits good stability under temperature change.

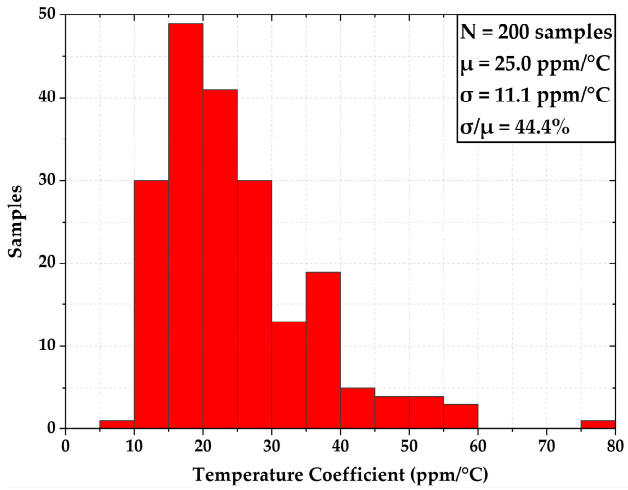


Figure 16. Monte Carlo simulation of output frequency T.C.

The supply dependence of the output frequency is depicted in Figure 17. The line sensitivity of the output frequency achieves 0.045%/V, 0.059%/V, and 0.081%/V at the TT corner, SS corner, and FF corner, respectively, from a 1.1 V to 1.6 V supply, which is

attributed to V_{REF} with good PSR at low frequency and the cascode transistors shielding the variation of supply in the comparators to stabilize the response time.

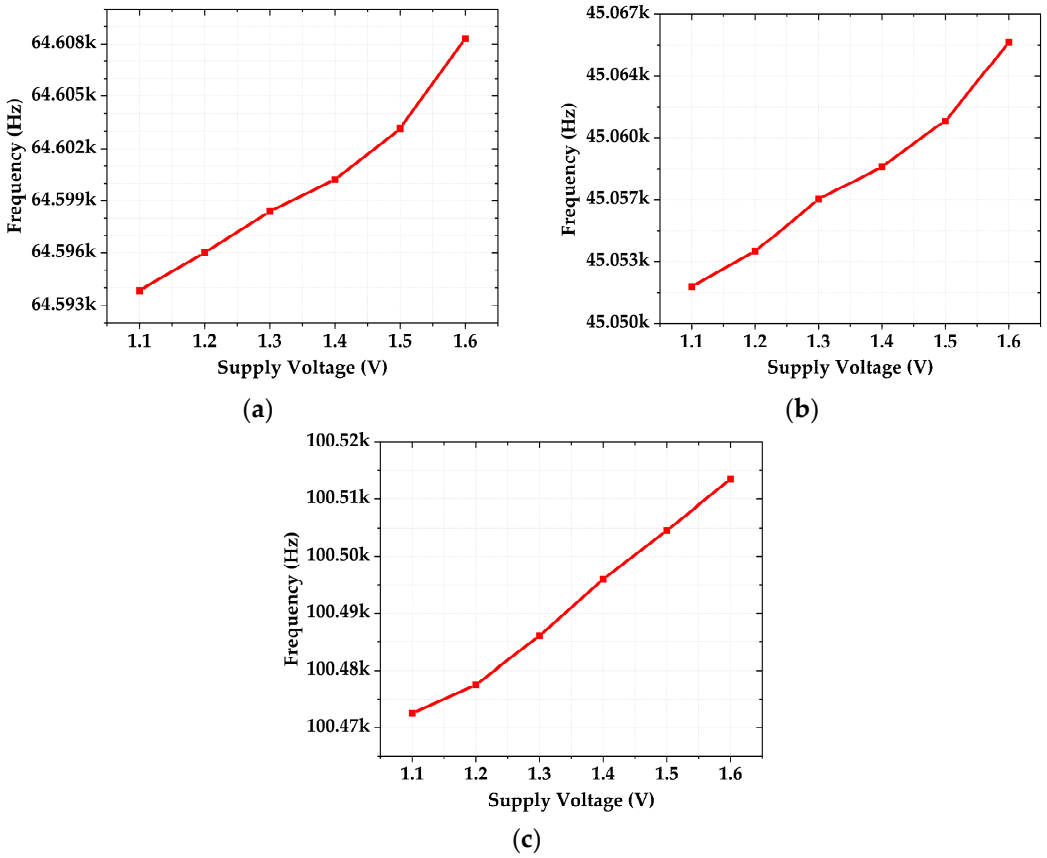


Figure 17. Supply dependence of output frequency at different process corners: (**a**) @TT corner; (**b**) @SS corner; (**c**) @FF corner.

The Monte Carlo simulation of the output frequency, with process variation and mismatch at different temperatures, is shown in Figure 18. The average values of the output frequency under different temperatures remain almost the same: 64.84 kHz, 64.95 kHz, and 64.9 kHz, with the standard deviation of 6.42 kHz, 6.42 kHz, and 6.41 kHz at −20 °C, 30 °C, and 80 °C, respectively. This yields the average process sensitivity (σ/μ) of 9.88%. The output frequency is eventually dependent on the value of the composite resistor *Rs* in Figure 6 and the capacitors C_1 and C_2 in Figure 10. The process variation displays the moderate value, which is targeted for moderate precision applications. However, to cater to a precision design, this can be achieved by trimming the passive MoM capacitors C_1 and C_2, which are less affected by temperature.

The performance of the proposed ROSC is compared to that of the previously reported representative works using advanced process technology nodes, as shown in Table 4, and with longer channel length technology nodes, as shown in Table 5. It can be seen that the proposed relaxation oscillator, with the dynamic current consumption of 552 nA at a 1.1 V supply voltage, exhibits the best T.C. for one sample. The same goes for the Monte Carlo 200-sample result, with process variation and mismatch. Regarding line sensitivity, the proposed work a displays lower value due to the use of the cascode current mirror plus the two-transistor-based voltage reference topology, which has the feature of small line sensitivity.

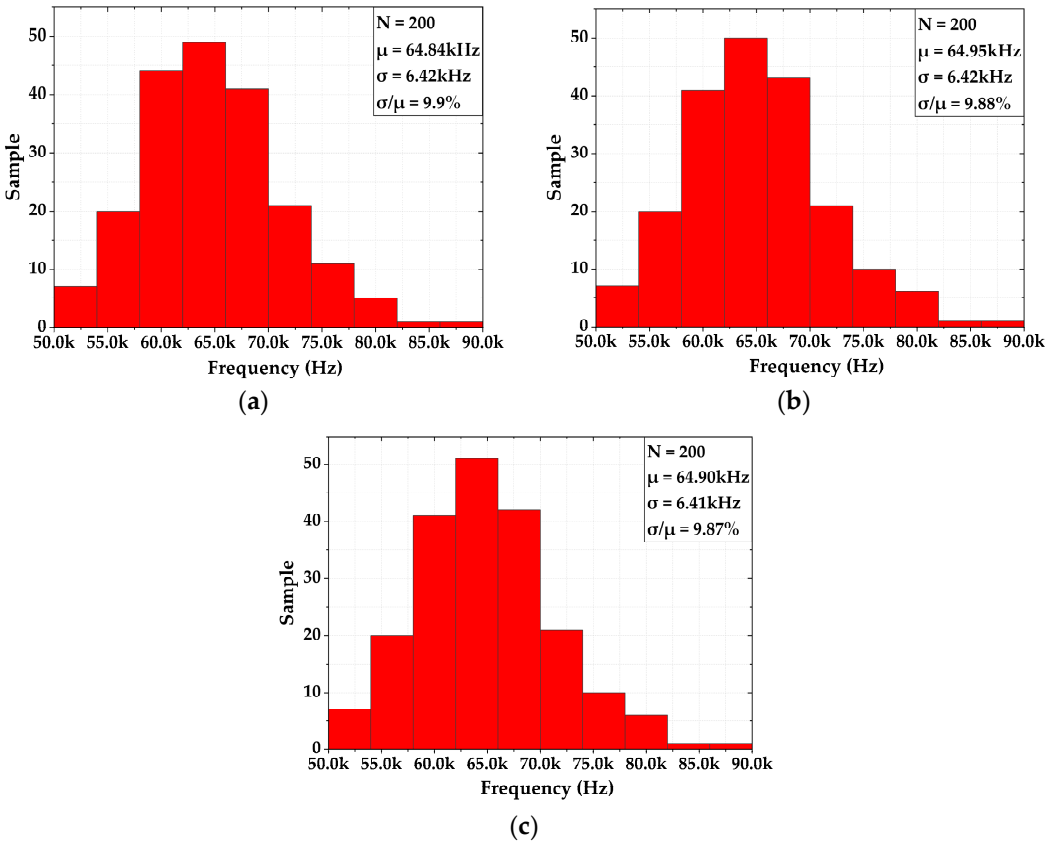


Figure 18. Monte Carlo simulation of output frequency: (**a**) @−20 °C; (**b**) @30 °C; (**c**) @80 °C.

Table 4. Performance comparison with previously reported ROSC works in advanced technology nodes.

Parameter	[7] 2016	[8] 2017	[9] 2020	[10] 2012	[19] 2017	[20] 2013	This Work
Technology	65 nm	65 nm	40 nm	60 nm	65 nm	65 nm	**40 nm**
Frequency (kHz)	64.4	64.2	32.7	32.7	32.5	18.5	**64.6**
Supply Voltage (V)	1.2	1.2	0.6	1.6	1.2	1	**1.1**
Current_TT (μA)	3.6	7.47	0.067	2.8	0.225	0.12	**0.55**
T.C._TT (ppm/°C)	144	14.7	21.7	32.4	138	22	**12.4**
T.C._MC (ppm/°C)	NA	NA	35.5	NA	NA	NA	**25**
Temp. Range (°C)	−20–100	−20–100	−40–125	−20–100	−40–80	0–90	**−20–80**
Line Sens. (%/V)	0.91	0.188	0.5	0.125	1.39	1	**0.045**
Process Sen. (σ/μ)% without trimming	3.66	NA	11.73	NA	10.4	NA	**9.86**
FoM (%)	1.549	0.169	0.247	0.344	1.54	0.32	**0.129**
Result	Simulated	Simulated	Simulated	Measured	Simulated	Measured	Simulated

The process sensitivity of the output frequency is comparable and can be improved by trimming the two capacitors. To evaluate the stability of the output frequency, with both temperature and supply variations, a figure-of-merit (FoM), including the temperature coefficient and the line sensitivity [9], is defined as

$$FoM = T.C. \times 100\ ^{\circ}\mathrm{C} + Line.Sens. \times 10\%V_{DD\min} \quad (17)$$

where T.C. is the one sample value at the typical corner. The FoM of the proposed ROSC is 0.129%, which displays the best result when compared to the prior-art works shown in Table 4. Therefore, the proposed design can offer a stable frequency while providing a good

tradeoff between stability and power consumption. Finally, in view of the larger leakage current, as well as the lower transistor intrinsic gain in this 40 nm technology with respect to those of technology nodes having a longer channel length, the frequency stability of the proposed work, as shown in Table 5, also shows excellent FoM. This demonstrates the usefulness of the circuit.

Table 5. Performance comparison with previously reported ROSC works employing technology nodes with longer channel length.

Parameter	[1] 2013	[23] 2010	[28] 2014	[29] 2007	This Work
Technology	180 nm	350 nm	180 nm	350 nm	**40 nm**
Frequency (kHz)	32.55	3.3	28	80	**64.6**
Supply Voltage (V)	1	1	1.2	1	**1.1**
Current_TT (µA)	0.47	0.066	0.033	1.06	**0.55**
T.C._TT (ppm/°C)	120	260	95.5	842	**12.4**
T.C._MC (ppm/°C)	NA	NA	NA	NA	**25**
Temp. Range (°C)	−40–100	−20–80	−20–80	0–80	**−20–80**
Line Sens. (%/V)	1.1	3.5	3	2.5	**0.045**
Process Sen. (σ/µ)% without trimming	1.39	NA	NA	3.95	**9.86**
FoM (%)	1.31	2.95	1.255	8.67	**0.129**
Result	Measured	Measured	Measured	Simulated	Simulated

5. Conclusions

This paper presents a 40 nm CMOS relaxation oscillator with low-current consumption. It features simple topology that comprises a two-transistor-based voltage reference generator and a simple current reference generator with a temperature-compensated composite resistor. Moreover, the comparators are designed with a CTAT delay to counteract the PTAT delay contributed by the effect of the leakage current in switches, thus improving the thermal stability of the output frequency.

The simulation results confirmed that the proposed ROSC displayed excellent output frequency stability against the changes in temperature and supply voltage. Therefore, the proposed work is suitable for low-power applications that require an oscillator with a stable frequency and moderate precision.

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