7.6   A 1.23pJ/b 2.5Gb/s Monolithically Integrated Optical Carrier-Injection Ring Modulator and All-Digital Driver Circuit in Commercial 45nm SOI

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Integrated photonic interconnect technology presents a disruptive alternative to electrical I/O for many VLSI applications. Superior bandwidth-density and energy-efficient operation can be realized through dense wavelength-division multiplexing (DWDM) and lower transmission losses. There are two main paths towards an integrated platform. Hybrid/heterogeneous designs [1-3] enable each component to be custom-tailored, but suffer from large packaging parasitics, increased manufacturing costs due to requisite process flows, and costly 3D integration or microbump packaging. Monolithic integration mitigates integration overheads, but has not penetrated deeply-scaled technologies due to necessary process customizations [4]. The first monolithic integration of photonic devices and electronic-photonic operation in sub-100 nm (45 nm SOI process with zero foundry changes) is demonstrated in [5]. This paper presents a monolithically integrated optical modulator with a new all-digital driver circuit in a commercial 45nm SOI process. The waveform-conditioning driver circuit enables the carrier-injection modulator to operate at 2.5Gb/s with an energy-cost of 1.23pJ/b, making it ~4× faster and more energy-efficient than the previous monolithically integrated driver/modulator presented in [5].

The double-data-rate (DDR) modulator and driver circuit (Fig. 7.6.1) are fabricated as part of a 5M-transistor integrated platform for optical I/O. Light from an off-chip laser couples onto the die through vertical grating couplers and propagates through on-chip silicon waveguides. Fed by two 31b on-chip pseudo-random bit sequence (PRBS) generators, the DDR modulator circuit drives the modulator device to imprint data onto a particular wavelength-channel. A digital snapshot checks the validity of the generated data. The optically-modulated data is brought off-chip through a vertical grating coupler and measured using an optical oscilloscope.

The optical modulator device is a resonant ring with rib waveguide carrier-injection phase shifters, identical to the one in [5], implemented using a combination of the gate polysilicon and body silicon layers in the process front-end. The device cross-section and transfer function are illustrated in Fig. 7.6.2. The optical 3dB bandwidth of the device is 45GHz. Modulation is achieved by tuning the ring in and out of the wavelength-channel through carrier injection. Due to long carrier lifetimes in single-crystalline Si, this device has an electrical 3dB bandwidth of approximately 250MHz that limits the data-rate in [5] to 600Mb/s at an energy cost of 4.2pJ/b. The driver we present in this work overcomes this bandwidth limitation through optimized drive conditioning with the same optical device design and 1950µm^2 area footprint.

The DDR driver circuit (Fig. 7.6.3) is designed as an all-digital push-pull driver circuit with configurable drive strengths, sub-bit-time pre-emphasis [6] and split supplies, operating over a range of drive current profiles required for a wide variety of optical devices. The split power supply and level-shift drivers allow an exploration of the tradeoffs between energy-cost and extinction ratio without increasing the power consumption of the back-end. Unlike previous work on sub-bit pre-emphasis based on [6], where different voltage values are used to pre-emphasize the modulator drive, in this work we change the on-resistance of the modulator driver connected to a fixed supply voltage.

The highly configurable driver back-end controls four independent drive heads, each providing a configurable drive strength and specialized biasing regime. As illustrated in Fig. 7.6.4, combination of drive segments A and B provides the strongest drive constituting the sub-bit current pre-emphasis needed for fast injection of carriers into the modulator, on a "0" to "1" transition. Reduced-strength segment B then maintains the lower current levels necessary for keeping the carriers inside the modulator during a logic "1", making-up for the carri-

ers lost in recombination. On a "1" to "0" transition, segment D provides a fast reverse-bias period to enable the discharge of carriers from the modulator. After the brief discharge period, the modulator is weakly forward-biased into sub-threshold through segment C, in order to lower the on-resistance of the modulator intrinsic region and enable faster turn-on "0" to "1" transient. In combination with forward and reverse-bias sub-bit pre-emphasis, the weak subthreshold forward biasing is the key to speeding up the device by an order of magnitude above its operating bandwidth.

The effect of subthreshold forward bias with segment C is illustrated in Fig. 7.6.5, where both rise- and fall-time transients are sped-up with respect to the previous regime of operation [5] in which the short reverse bias period is followed by driver cut-off. The optical eye diagram (Fig. 7.6.5) demonstrates fully-monolithic multi-gigabit electro-optic modulation in 45nm technology. We achieve an open eye at 2.5Gb/s, roughly 10× the bandwidth of the modulator device, at better than 3dB extinction ratio and modulator loss of 3dB at VDD of 1.1V and HVDD of 1.5V. The shown 1550nm band 2.5Gb/s eye diagram generated from the on-chip PRBS is mainly limited by the lower power of the laser and the higher noise of the optical amplifier.

To study the trade-off between energy-cost and performance, the modulator driver's high-supply voltage (HVDD) is swept and the extinction ratio recorded for a fixed insertion loss (Fig. 7.6.6). Despite relatively weak on-state drive (weak B driver), the energy-cost is still dominated by the modulator diode current, with energy-efficiency improving at higher data rate. The pre-driver cost is 130fJ/b. As the strength is increased, the modulator ring's optical response is shifted further from the wavelength-channel, increasing the extinction ratio. The modulator is able to achieve extinction ratios better than 3dB across voltages compatible with the process, at insertion loss of 3dB. If the insertion loss is increased, a superior extinction ratio can be achieved since the Lorentzian response becomes steeper near the resonance. In practice, this increase in loss maps back to the laser and system power.

This work demonstrates a monolithically-integrated 2.5Gb/s optical modulator with an all-digital driver circuit, operating with an energy-cost of 1.23pJ/bit and better than 3dB extinction ratio in a commercial 45nm SOI process. The modulator and its photonic platform spearhead the realization of dense and energy-efficient communication fabrics with the potential to exceed projected future demands.

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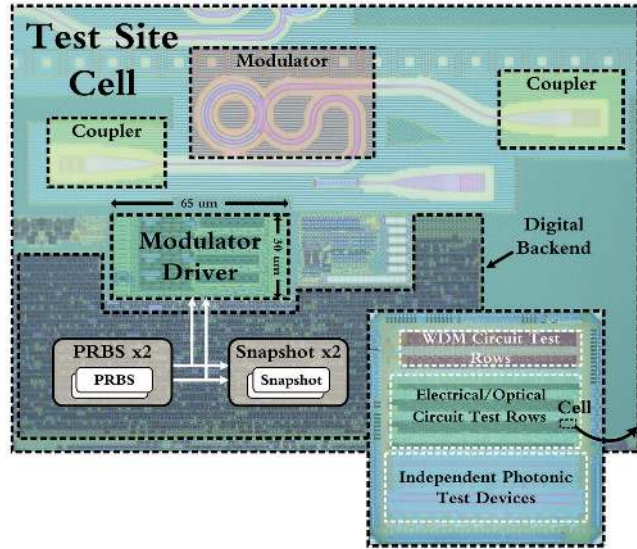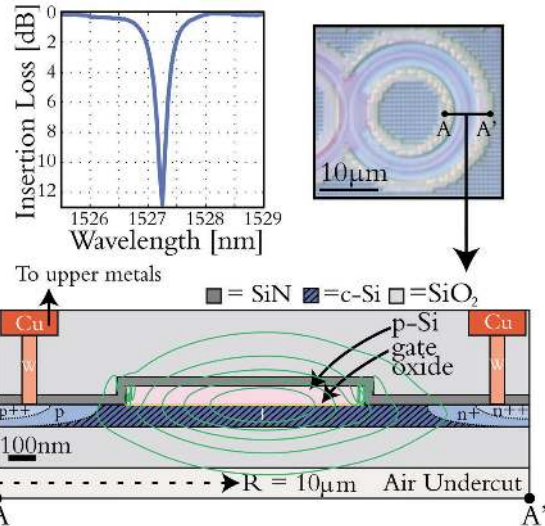
Figure 7.6.1: Modulator test site.

Figure 7.6.2: Optical modulator device connected to the modulator driver circuit.
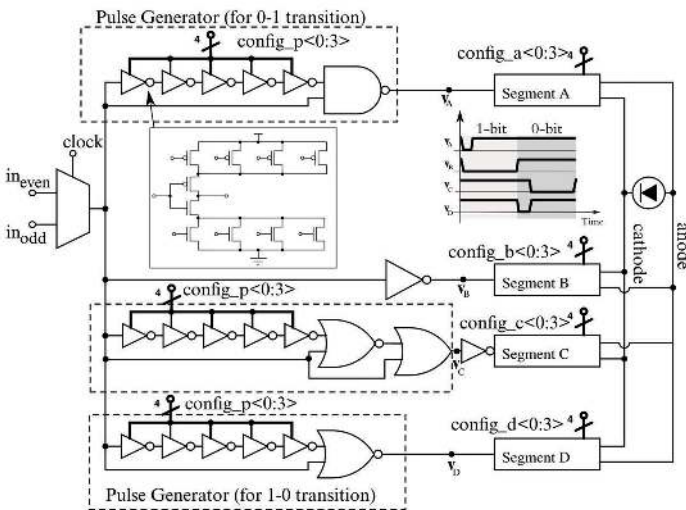
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Figure 7.6.3: Configurable, all-digital modulator driver circuit with split supplies and sub-bit pre-emphasis.
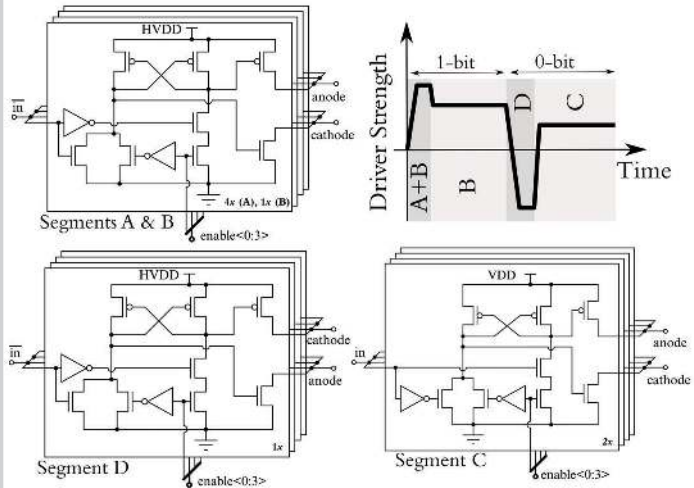

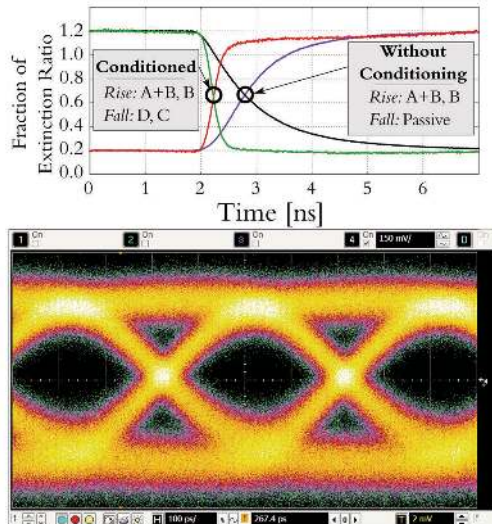Figure 7.6.4: Detailed schematics of the modulator driver heads.

Figure 7.6.5: Effect of sub-bit-time pre-emphasis and subthreshold forward-biasing on bit transition edges and eye diagram at 2.5Gb/s.
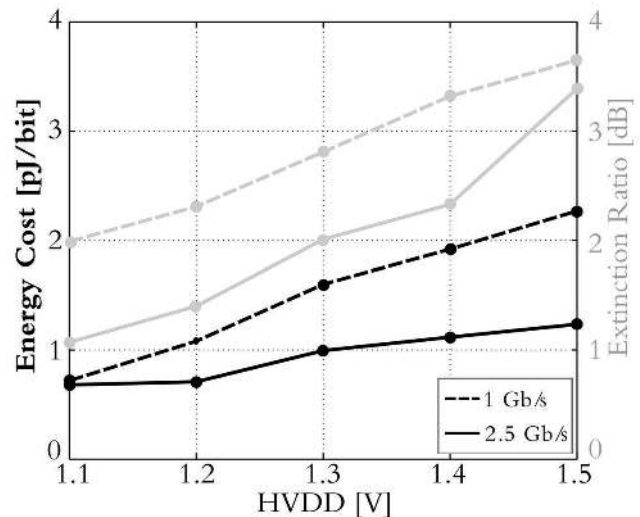

Figure 7.6.6: Energy-cost and effect of circuit drive strength on extinction ratio for a fixed insertion loss.
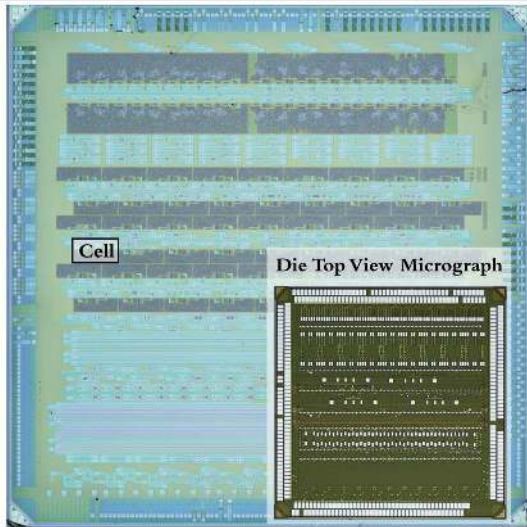
Figure 7.6.7: 2.9mm x 2.9mm die photo as viewed from the backside after substrate removal. Top view micrograph of fabricated die is shown in the inset.