TP 12.5 A 1.4GHz Differential Low-Noise CMOS Frequency Synthesizer using a Wideband PLL Architecture

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The growing importance of wireless media for voice and data communications is driving a need for higher integration in personal communications transceivers to achieve lower cost, smaller form factor, and lower power dissipation [1]. One approach to this problem is to integrate the RF functionality in low-cost CMOS technology together with the baseband transceiver functions. This in turn requires integration of the frequency synthesizer with enough isolation from supply noise to allow it to coexist with other on-chip transceiver circuitry and still meet the phase noise performance requirements of the application. This differential synthesizer for block-down-convert receivers achieves improved levels of phase noise and supply rejection performance through the use of fully-differential architecture and a wide-bandwidth PLL.

In conventional double-conversion receivers, the RF synthesizer utilizes a low-phase-noise VCO coupled to a reference oscillator by a low bandwidth synthesizer loop. The low bandwidth is desirable to minimize spurious tones in the output frequency spectrum that result from the frequency comparison process. One consequence of the low bandwidth is that the phase noise of the overall synthesizer is dominated by the phase noise of the VCO. Because of the limited Q of varactor-tuned tank circuits implemented with on-chip components, realization of low-phase-noise synthesizers required in the most demanding applications using this conventional approach has proven a difficult challenge.

An alternative approach is to use a wide bandwidth PLL to closely couple a noisy on-chip VCO to a clean reference. The phase noise contribution from the on-chip VCO to the output within the synthesizer control bandwidth is thus suppressed. Because wide PLL bandwidth requires a high comparison frequency, this type of synthesizer is most amenable to the synthesis of a few widely-spaced frequencies, and is thus most compatible with block-down-convert receiver architectures such as the wideband IF double-conversion architecture [2]. In these architectures, the entire signal band at RF is mixed down to the IF with a fixed RF frequency synthesizer, and a variable frequency synthesizer at IF is used to tune the desired channel from IF to the baseband. Because this second synthesizer is at a much lower frequency, minimization of its phase noise contributions is much easier.

Because noise from the VCO is suppressed in wideband PLL architectures, other noise sources become more important in overall synthesizer performance. Noise from the crystal oscillator reference, divider, and phase/frequency detector become the most important contributors within the loop bandwidth and are referred to the output enhanced in effect by the divider ratio N. For this reason, a low-noise latch clocked by the VCO is added at the output of the divider to remove the noise from divider itself.

The concepts described above are embodied in a prototype in 0.35µm 2-poly 5-metal CMOS, intended as the first LO in a multi-standard wireless transceiver. The loop is fully differential. The VCO is differentially controlled and the latch at the output of the divider is differentially clocked by the VCO. The loop bandwidth is 8MHz.

A circuit diagram of the differentially controlled VCO with differential output is shown in Figure 12.5.1. The on-chip resonator consists of spiral inductors using three layers of metal connected in parallel and varactors using p+/nwell junctions partitioned into small units. The differential control path is implemented with four varactors connected as shown with differential controls. Capacitance changes of D1 and D2 due to common-mode control voltage perturbations are first-order compensated by opposite changes of D3 and D4. The oscillation frequency to the first order depends only on the differential controls rather than the common-mode control voltage.

Spurious tones resulting from the frequency comparison process do not get much attenuation by the loop filter because of the wide loop bandwidth. Matching of the current sources in the charge pump is critical in minimizing these tones. Figure 12.5.2 shows the circuit diagram of the differential charge pump with active loop filter. Full swing UP and DN signals from the phase/frequency detector (PFD) output are used to completely turn off the switches to minimize the leakage current and hence mismatch of the leakage current. An active loop filter is used so that the steady-state charge pump differential output is always zero even when a large control voltage is required to drive the VCO. A common-mode feedback (CMFB) circuit sets the charge pump output common-mode at a level so that the matching between the current sources in the charge pump is maximized. This CMFB loop is connected only when all four switches in the charge pump are off, which is true for a portion of the frequency comparison period at the PFD. Hence, this CMFB is a sampled-data circuit. A separate continuous-time CMFB circuit sets the loop filter common mode output to be the same as the VCO common mode output to maximize the VCO tuning range.

The prototype produces three RF frequencies, e.g., 1.3824GHz, 1.4688GHz, and 1.5552GHz, while achieving -118dBc/Hz phase noise at 100kHz and -56dBc spurious tone at 86.4MHz. When a 0.8MHz 200mV peak-to-peak sinewave is added to the supply, the synthesizer generates a -42dBm tone. This translates to -32dB effective PSRR. Measured PSRR for other frequencies is shown in Figure 12.5.5. When the 200mV tone is present, synthesizer phase noise at 100kHz degrades to -116dBc/Hz. The complete synthesizer dissipates 84mW from a 3.3V supply. Figure 12.5.7 shows a summary of chip performance.

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References:

[1] Gray P.R., and Meyer R.G., "Future Directions in Silicon IC's for RF Personal Communications," *Proceedings, 1995 Custom Integrated Circuits Conference*, pp. 83-90, May 1995.
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[5] Chien, G., and Gray, P.R., "A 900MHz Local Oscillator using a DLL-based Frequency Multiplier Technique for PCS Applications," *ISSCC Digest of Technical Papers,* Feb. 2000.

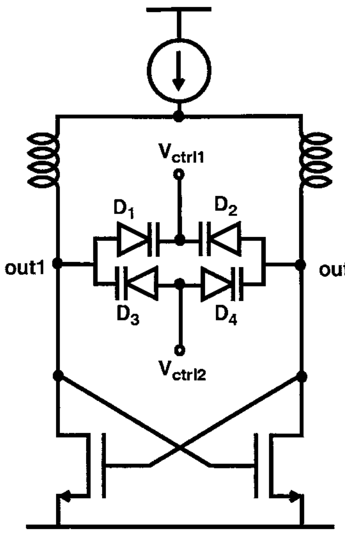

Figure 12.5.1: Differentially controlled VCO.

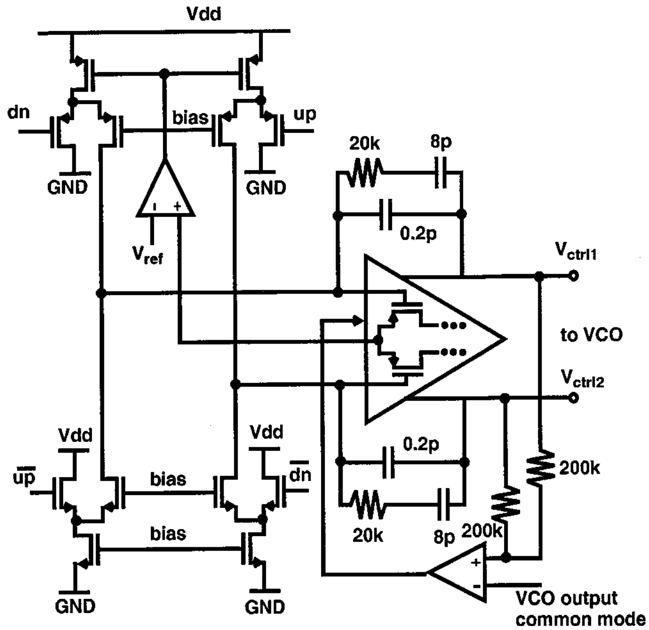

Figure 12.5.2: Differential charge pump with active loop filter.

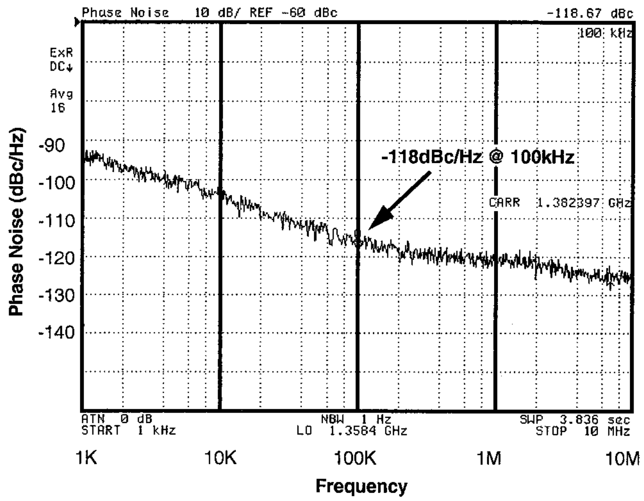

Figure 12.5.3: Measured phase noise performance.

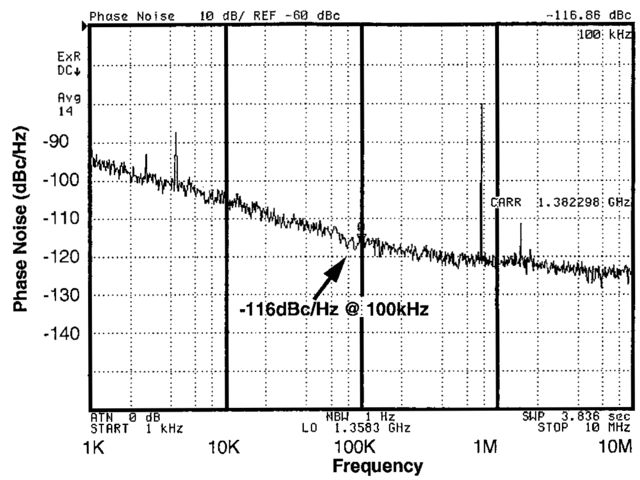

Figure 12.5.4: Measured phase noise with an 800kHz. 200mV peak-to-peak sinewave applied to the power supply.

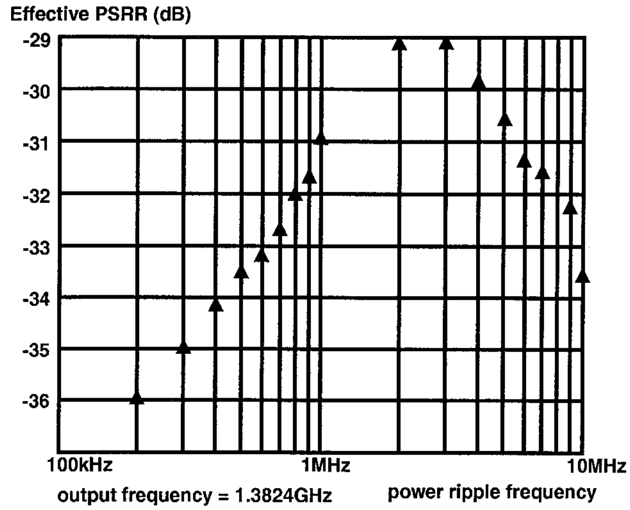

Figure 12.5.5: Effective PSRR vs. power ripple frequency.

Power	VCO	39.55mW
	CP,PD,DIV,Buffer	44.5mW
	Total	84.05mW
Phase Noise	@100kHz	-118dBc/Hz
	@1MHz	-120dBc/Hz
	@3MHz	-123dBc/Hz
Spurious	@86.4MHz	-56dBc
Effective PSRR	with 200mV p/p, 0.8MHz sinewave on supply	-32dB
Die Size	2260μm x 1860μm	
Process	0.35μm CMOS, 5-metal, 2-poly	

Figure 12.5.7: Performance summary at 25°C.

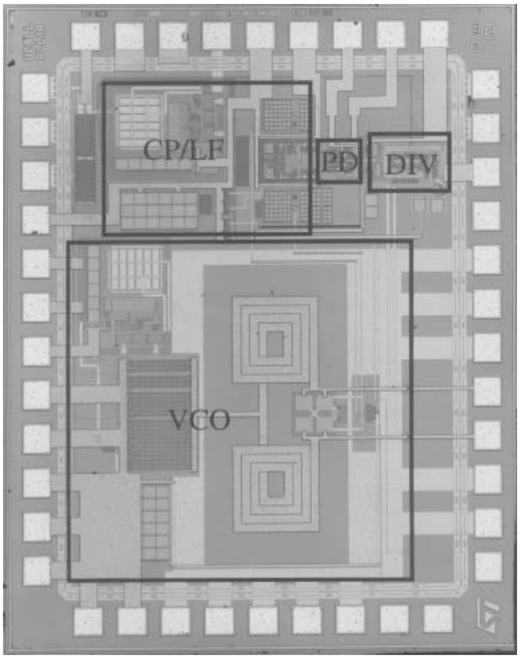

Figure 12.5.6: Die micrograph.

