A 1.5V, 1.5GHz CMOS Low Noise Amplifier

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ABSTRACT

A 1.5 GHz low noise amplifier for a Global Positioning System (GPS) receiver has been implemented in a 0.6µm CMOS process. This amplifier provides a forward gain of 22dB with a noise figure of only 3.5dB while drawing 30mW from a 1.5V supply. To the authors' knowledge, this represents the lowest noise figure reported to date for a CMOS amplifier operating above 1GHz.

Introduction

The demand for portable, inexpensive GPS systems motivates the investigation of low-noise front end techniques in standard CMOS processes. It has been shown that sub-micron CMOS devices exhibit excess thermal noise [1][2]. Nonetheless, recent work has demonstrated the viability of CMOS low noise amplifiers (LNA's) at frequencies as high as 900MHz [3]. In this paper, we present an LNA suitable for GPS applications which has been fabricated through MOSIS in a 0.6µm CMOS process.

LNA Design

The primary goal in the design of an LNA is to achieve the lowest possible noise figure with reasonable power. This task is somewhat constrained by the need to present a real 50Ω impedance at the input to properly terminate the off-chip source. The reactive input impedance of the MOS device can be converted into the necessary real resistance by means such as dual-feedback, resistive termination, and inductive source degeneration. Dual-feedback techniques are commonly used at lower frequencies where loop gain requirements are easily satisfied. Resistive termination is simple, but has the disadvantage of placing a lower bound of 3dB on the achievable noise figure. In this work, we have employed inductive source degeneration combined with input tuning to provide a narrow-band 50Ω input impedance. The principle of operation may be demonstrated as follows.

Fig. 1 illustrates the common-source input stage of the LNA. A straightforward analysis of the input impedance shows that

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_s$$

Note that L_s contributes a real term to the input impedance through interaction with C_{gs} and g_{m1}. By choosing L_g+L_s to resonate with C_{gs}, the impedance will look real at frequencies near the input resonance. In our implementation, L_s is supplied by parasitic package inductance.

The noise figure of the LNA can be approximated using the equivalent circuit illustrated in Fig. 2. Noise contributed by subsequent stages may be neglected if the first stage possesses sufficient gain. Elements R_l and R_g represent losses due to inductor resistance and gate resistance, respectively. The transconductance of the input stage is given by

$$G_{m,\,eff} = g_{m1}Q_{in} = \frac{g_{m1}}{\omega C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{\omega R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)}$$

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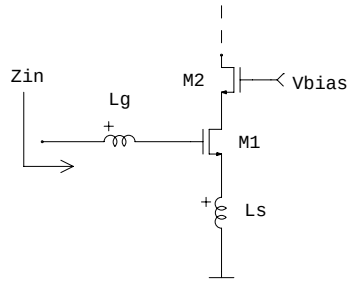

Fig. 1 Common-source input stage

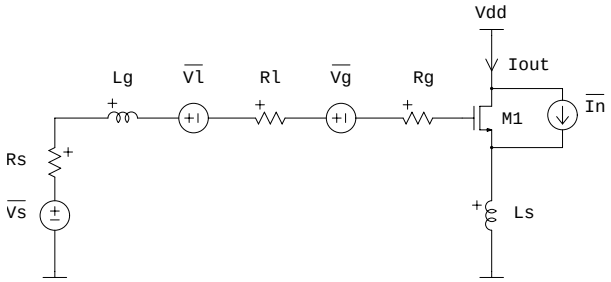

Fig. 2 Equivalent circuit for input stage noise calculations

where Q_{in} is the effective input Q of the circuit. Note that R_l and R_g have been neglected relative to R_s. This expression is valid at resonance where the signal voltage across C_{gs} is equal to Q_{in} times the input signal. It is worth noting that the overall transconductance is apparently independent of g_{m1}, the intrinsic device transconductance. This fact leads to an important implication for noise figure, as will be shown momentarily.

Several noise sources contribute significantly to the output noise of the LNA. The source resistance, inductor parasitic resistance, gate resistance, and NMOS channel noise are the most significant. Of these sources, the channel noise current is the most problematic. This noise current is commonly expressed as [2]

$$\overline{i_n^2} = 4kTB\gamma g_{d0}$$

where g_{d0} is the zero-bias drain conductance, and γ is a function of bias. Experimental studies have shown that γ may be as high as 2 to 3 for short channel devices operating in saturation. This value generally increases with increasing drain bias. The increased value of γ over the long channel value of 2/3 is evidently due to hot electrons in the channel [1]. In terms of γ, the output noise current due to the channel thermal noise is

$$\overline{i_{out}^2} = \frac{\overline{i_n^2}}{\left(1 + \frac{\omega_T L_s}{R_s}\right)^2} = \frac{4kTB\gamma g_{d0}}{\left(1 + \frac{\omega_T L_s}{R_s}\right)^2}$$

The noise figure is given by the total output noise power divided by the noise power at the output due to the input source. Including the contributions of inductor loss and gate resistance,

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega}{\omega_T}\right)^2$$

(neglecting the contribution of subsequent stages). Note that the noise figure improves by *minimizing* the size of the input device, contrary to intuition. This also implies that high power dissipation is not necessary for good noise performance. However, LNA linearity degrades as g_{d0} decreases because the signal level across C_{gs} increases. So, reducing g_{d0} is most effective in applications where linearity requirements are modest. In addition, as g_{d0} decreases, L_g must increase to maintain the same resonant frequency. Hence, the inductor loss increases, limiting the improvement available through reduction in g_{d0}.

It is also important to note the role of technology improvements in this topology. The channel noise term is inversely proportional to ω_T^2. Based on the measured performance of this amplifier, noise figures of about 1.6dB should be attainable at 900MHz using a similar topology. We may also expect 0.3µm CMOS technologies to permit noise figures of around 1dB at 1.5GHz.

Experimental Results

An LNA based on this topology has been fabricated in a 0.6µm CMOS process. A complete schematic is shown in Fig. 3. Simulation models were unavailable during the design of the LNA, so a flexible topology was chosen. A single 7nH spiral inductor acts as a tuned load to the first stage, resonating against the gate capacitance of M3 and the drain capacitance of M2. An open-drain stage drives a 50Ω load off-chip. The amplifier uses the test instrument itself as the load.

The input device is biased through an off-chip bias tee. The gate inductance L_g is formed by package inductance in series with a 4nH spiral inductor. After fabrication, we discovered that the input resonance occurred at a higher frequency than the peak gain, so shunt capacitance was added to adjust the input resonance to 1.5GHz. This permitted an input VSWR of 1.38 at 1.5GHz.

Using this system, the measured gain of the LNA was 22dB and the measured noise figure was 3.5dB at 30mW power dissipation. About half of the power (15.2mW) is used in the output driver and could be reduced by re-sizing M3 without impairing the noise performance of the LNA. Spice simulations using models supplied after fabrication predict a noise figure of 1.7dB, which implies that γ is approximately 2.6 for the input device of this amplifier. This value of γ is comparable to results reported in [1].

Fig. 4 illustrates the measured S21 of the amplifier. The dip in S21 at 1.35GHz may be attributed to poor reverse isolation (a peak in S12 occurs at 1.4GHz). An IP3 measurement yielded -9.3dBm (input-referred), as shown in Fig. 5. Additionally, the noise figure was measured for various values of Vcc with a fixed input bias. The result is shown in Fig. 6, indicating a minimum noise figure of 3.3dB.

Conclusion

We have demonstrated a 1.5GHz LNA fabricated in a standard 0.6µm CMOS process. To the authors' knowledge, the measured noise figure of 3.5dB is the lowest noise figure reported to date for a CMOS amplifier operating above 1GHz. This work thus demonstrates that modern CMOS processes are suitable for low noise applications above 1GHz, despite the presence of excess channel noise.

Acknowledgments

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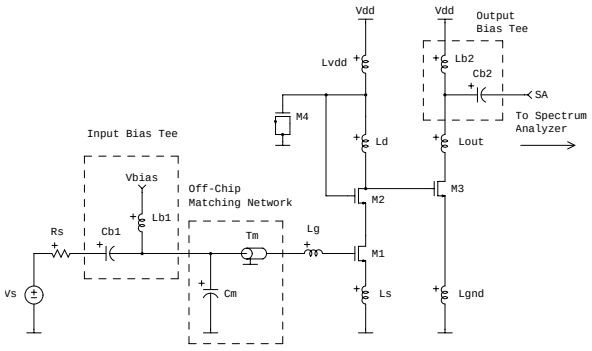

Fig. 3 Complete LNA schematic, including off-chip elements

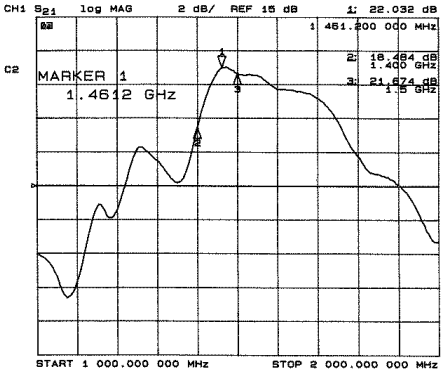

Fig. 4 Measured S21 of the LNA

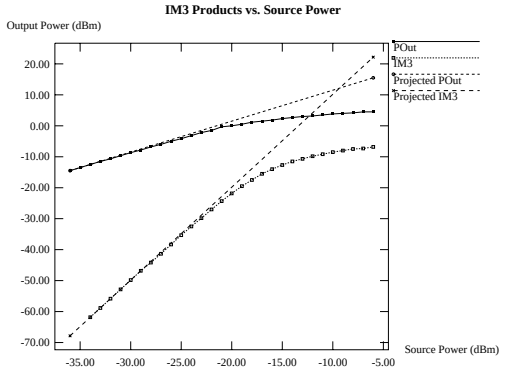

Fig. 5 LNA Intermodulation products and IP3

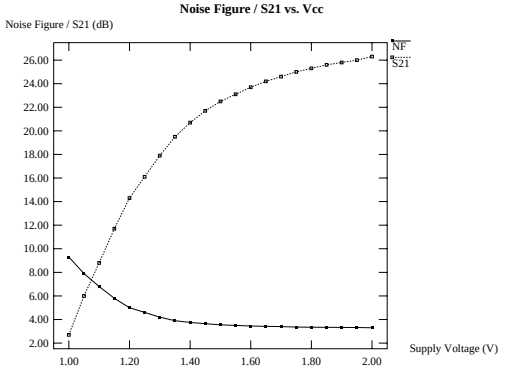

Fig. 6 Noise Figure and S21 vs. Vcc, Vbias=1.0V