# A 1.6 GS/s, 16 Times Interleaved Track & Hold with 7.6 ENOB in 0.12 μm CMOS

Simon M. Louwsma, Ed J.M. van Tuijl, Maarten Vertregt*, Peter C.S. Scholtens*, Bram Nauta

IC-Design Group, MESA+ Research Institute, University of Twente, Enschede, the Netherlands
*Philips Research, Eindhoven, the Netherlands
S.M.Louwsma@utwente.nl

## Abstract

*A 1.6 GS/s Track and Hold circuit that produces 16 interleaving, 100 MS/s voltage buffered output signals is presented. The achieved SFDR for a 950 MHz full scale input signal is 50 dB. Phase alignment is better than 2 ps and aperture uncertainty is less than 0.8 ps (RMS). The chip includes two Analog to Digital Converters and a Switching Matrix to accommodate measurement of all sampled output signals and their timing relation. Chip area is 0.14 mm$^2$ excluding the AD Converters. The chip is made in a 0.12 μm, 1.2 V CMOS Process. Power consumption of the interleaving T/H circuit is 32 mW.*

## 1. Introduction

For analog to digital conversion at samplerates above 1 GS/s, typically flash [1] converters are used. The resolution of these converters is limited, because each extra bit would require 4 to 8 times more gate area resulting in excessive input capacitance and power consumption. For embedded applications flash converters are therefore practically limited to 6 bits of accuracy; however for applications like cable-TV, higher resolutions are needed. For lower speeds, alternative architectures are widely available (like pipeline converters) which enable higher resolutions and have a higher efficiency. If accuracy of more than 6 bits is needed, combined with samplerates in the GS/s-range, interleaving multiple (pipeline) ADCs is a good option. In [2] an 8 bit 20 GS/s ADC is reported, consisting of 80 interleaved pipeline converters. Although the performance is impressive, the power consumption of 10 W is too high for embedded applications. An important part of an interleaving ADC is the front-end T/H. In [3] and [4] GS/s-range track and hold circuits are presented, but they are all in bipolar technology, do not accommodate interleaving, and can not be embedded in standard CMOS. In this paper we present a 1.6GS/s interleaving track and hold with only 32mW of power consumption for application in a 16 times interleaved ADC architecture aiming at 8 bit performance.

## 2. Architecture

A schematic overview of the architecture of our test-chip is shown in Figure 1. The circuit consists of 16 separate track and hold (T/H) circuits. Because analog off-chip measurement is difficult, a switching network and 2 ADCs are integrated to enable on-chip analog measurement. The switching network can connect each of the 16 T/H outputs to each of the ADCs. In this way linearity, offset, gain and time (phase) accuracy of the individual T/H circuits can be verified. The measurement method will be explained in section 5.

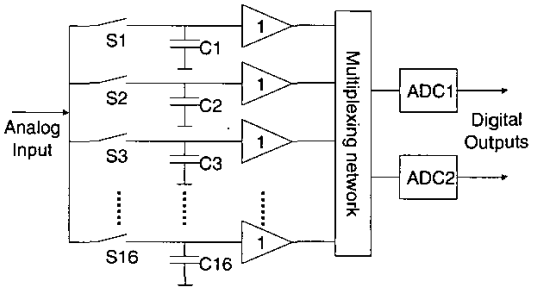


*Figure 1: Architecture of the chip realization*

To create an interleaving T/H, the switches have to be opened one after another. The timing diagram is shown in Figure 2. The arrow at the bottom indicates one subsample period that contains 16 clockperiods of the 1.6 GHz sample clock. The track time is 4 clock periods (2.5 ns), while the hold time is 12 clock periods (7.5 ns). The asymmetry between track and hold relaxes the ADC requirements. Furthermore, at each moment in time only 4 instead of 8 sample capacitors are connected to the input, which results in less input load capacitance and increases the input bandwidth. Decreasing the track time even further would result in incomplete settling.

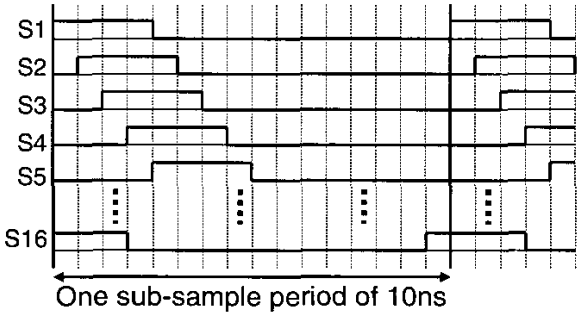


*Figure 2: Timing of the switches in a 16 times interleaving Track and Hold*



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During each clock period one T/H circuit is switched into the hold mode (e.g. T/H1) and another is switched into the track mode (in this case T/H5). This last event generates a voltage spike at the input, because a capacitor with a previously sampled value is connected to the input. To avoid the influence of this spike (on T/H1), the switches in trackmode close after the switches in holdmode have been opened.

## 3. Circuit design / Implementation

A single ended version of a complete channel is shown in Figure 3. The switches are implemented using a single NMOST without bootstrapping. Although bootstrapping would result in a lower and more constant ON-resistance, it is not needed in order to reach the target accuracy of 8 bit. The sampling capacitors are 100fF to limit kT/C noise, but also to limit distortion as will be described later in this section.

The chip has a differential clock input to decrease crosstalk and reject ground bounce. The clock lines are terminated on-chip with 50 Ω to ground. The clock-buffer consists of an N-type differential pair with current mirror followed by three inverters to generate steep edges in order to minimize the effects of circuit jitter.

Each differential T/H output can be connected to each of the two ADCs. As shown in Figure 3, this is accomplished by switching blocks consisting of two transmission gates and a switch to ground. This switch is included to prevent capacitive crosstalk between the channels. The matrix is controlled by an external bus signal. The timing of the ADCs can also be controlled. When for example the next sampler is selected, to keep pace the ADC timing must be delayed by one clockperiod.

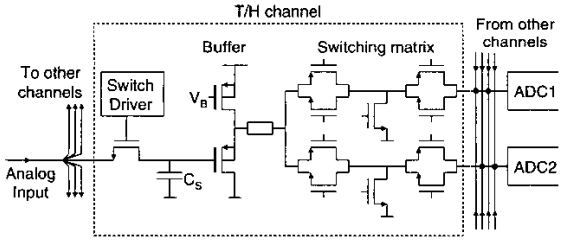


*Figure 3: A single ended T/H channel*

The ADCs are well-proven pipeline converters which were available in an analog library. They have a resolution of 10 bits which is enough to measure the accuracy of the T/H. The ADCs will not be discussed further, because they only serve the measurement purpose. The digital outputs are Low Voltage Differential Signalling (LVDS) buffers to minimize crosstalk from the digital outputs. Due to proper pin layout the crosstalk to the input pins is small and only common mode.

### 3.1 Switch-driver

With an fs of 1.6GS/s, the switches have to be opened 625 ps after each other. When the timing is not accurate, distortion products at multiples of fs/16 around the frequency of the input signal will appear, degrading the SINAD. To accomplish accurate timing, the circuit shown in Figure 4 is used. The circuit is a modified master/slave flipflop. The digital input D dictates whether the sample switch should be opened or closed on the next rising edge of the clock. Jitter of this signal does not influence the moment of the switch transition, because it is re-clocked by the master-clock running at fs. With this circuit it is possible to generate the clock scheme with interleaving and non-equal sample- and holdtimes. The critical, jitter generating path from clock-edge to sampling switch is kept as short as possible, minimizing aperture uncertainty due to noise and matching accuracy. As discussed in the previous section, some delay is needed when going from track- to holdmode. This is accomplished by varying the ratio of the PMOST and NMOST of the transmission gate and of the inverters A and B.

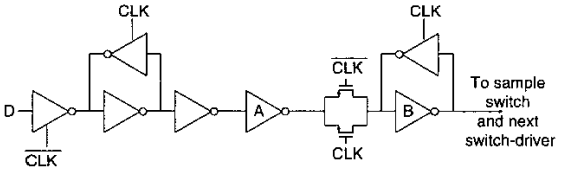


*Figure 4: Switch-driver circuit*

To generate the clock scheme as shown in Figure 2, a circuit generating a 4-out-of-16 signal is connected to the D input of switchdriver 1. The output of switchdriver 1 has the same shape as the input, but is delayed by one clockperiod. This signal is connected to the D input of switchdriver 2 and so on.

### 3.2 Buffer

The hold buffer is shown in Figure 3. It consists of a PMOST source follower, because this simple circuit has a large bandwidth and still enough linearity for 8 bit. The external biasing of the PMOST current sources is common to all buffers. A source follower has a DC level shift between its input and output. Offsets between the buffers result in distortion components in the combined digital output stream. The offsets should be smaller than half an LSB, which is 1 mV for 8 bits of accuracy. For the 0.12 μm technology the required gate area would be 352 $\mu m^2$ per buffer (3σ value).

Due to the nonlinear input capacitance of the buffer harmonic distortion is generated. To reduce this distortion the total capacitance can be linearized by connecting a linear (plate) capacitor in parallel. Simulation shows that this capacitance has to be about 5 times larger than the gate capacitance in order to get enough linearity for 8 bit. This would result in a load of about 0.7 pF * 5 per T/H, making the total input load 14pF. As the input is terminated with a 50 Ω resistor on-chip, the resulting input bandwidth would be limited to 270 MHz. This is far below the target, and therefore another solution is chosen. Much smaller source followers are used, which do not meet the matching

criteria. The offsets must then be calibrated, which is feasible [2] and is expected to have low power consumption, because only a DC calibration is needed. In this design the calibration is not yet implemented. The resulting input bandwidth including all parasitics is 3.5 GHz.

When the bandwidth of the buffer is a few times larger than the input frequency, the output of the buffer will follow the input. With the load of the ADC, which can be as high as 2pF, this results in huge power consumption. However for correct operation of the T/H and ADC such a high bandwidth is not needed, because the samplerate of the ADC is the input samplerate divided by the interleaving factor. Choosing the bandwidth of the buffer much lower than the maximum input frequency saves a lot of power. This has some consequences: when sampling a high frequency input signal the output can not follow the input signal completely. After the sampling moment the output settles to its final value. Thus after the sampling, the voltage over capacitor $C_{GS}$ of the source follower changes, which results in charge redistribution. This changes the voltage on the sampling capacitor and the final output value of the buffer, which introduces distortion due to the nonlinearity of $C_{GS}$. A poly-Si resistor is placed between the buffer and the output load (the ADC input), increasing the bandwidth of the buffer. Now the output can follow the input of the buffer and the distortion is reduced. A simulation result showing this behavior is shown in Figure 5. The dashed line is the voltage at the output of the buffer, following the input; the solid line is the voltage at the input of the ADC, with just enough bandwidth for correct settling.

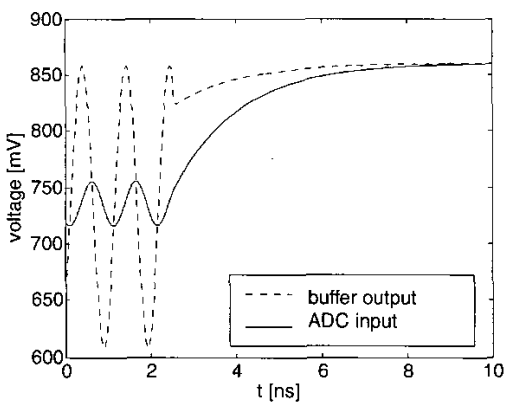


*Figure 5: Simulation result showing the behavior of the increased bandwidth at the output of the buffer.*

All circuits are quasi-differential so each T/H circuit contains 2 channels in a symmetrical layout. This symmetry and the choice of PMOS transistors (source connected to the N-well) in the source followers guarantees a good rejection of the common mode (ground) bounce.

## 4. Layout

Matching properties between the different T/Hs have to be good. Differences in phase, gain or timing will be depicted as tones related to multiples fs/16. To accomplish good matching a symmetrical bus structure is used as shown on the chip photograph in Figure 6. From the central point in the middle on the left, 16 busses with exactly the same length are connected to the T/H circuits. A layout of one of the T/H circuits is shown in Figure 7. The circuits all have the same orientation to minimize mismatch.

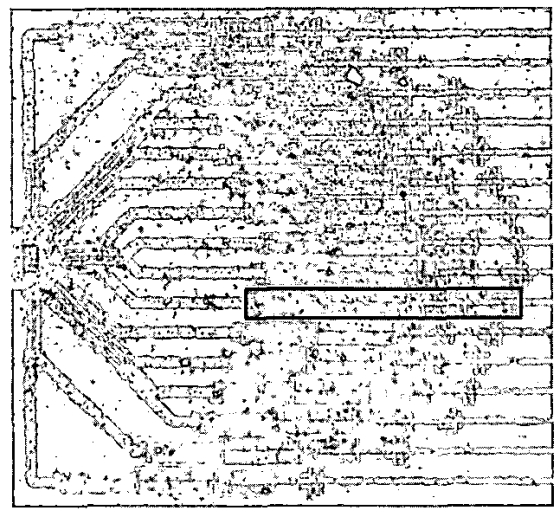

*Figure 6: Chip photograph showing the T/H core. Dimensions: 400 μm x 350 μm*

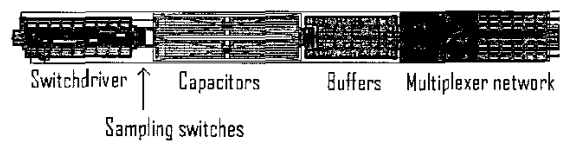


*Figure 7: Layout of a single T/H channel*

A cross section of the bus is shown in figure 8. The bus does not only contain the differential input signal, but also the differential clock signal and the supplies of the buffer that drives the switch. Differences in these are minimized and sampling time offsets are reduced. Another advantage of the bus structure is that both the clock and the input signals are shielded, lowering crosstalk between these two.

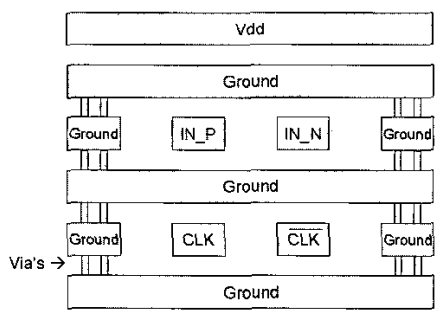


*Figure 8: Cross section of the bus structure*

## 5. Experimental results

The T/H is designed for a 2 GHz sampling frequency, implying a subsampling frequency of 125 MHz. The integrated ADCs however are limited to 100 MS/s, so testing was limited to 1.6 GS/s. Most measurements however were performed at 1280 MS/s in order to get an ENOB of 9.2 of the converters instead of 7.7 at 1.6 GS/S. The performance of a single channel of the distributed T/H is determined by connecting it to one of the ADCs. In figure 9 SFDR, -THD, SNR and SINAD/ENOB are shown as a function of the input frequency at a samplerate of 1280MS/s. The input amplitude at the chip is $0.5V_{PP,\ Differential}$ but varies slightly due to cable losses. This is visible as a ripple in SFDR and -THD.

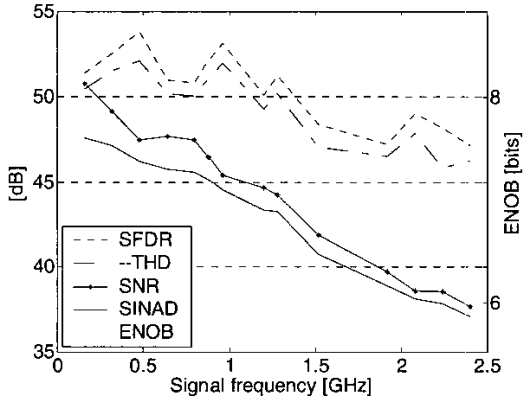


*Figure 9: SFDR, SNR, -THD, SINAD and ENOB of one T/H for different input frequencies. Fs = 1.28 GHz*

The effective resolution bandwidth (ERBW) is 1 GHz, starting from an initial 7.6 ENOB performance at 100MHz signal frequency. Beyond the ERBW, gradual and graceful degradation is observed up to 2.4GHz. Similar performance is measured for different channels and different samples. At high frequencies the SNR drops due to the influence of clock-jitter and at low frequencies the SNR is dominated by circuit noise. From calculations it follows that the jitter is about 0.9ps RMS. This jitter stems from the external clock generator, the external signal generator, and from the T/H circuit. The jitter of the clock generator is specified at 0.8ps RMS, so the jitter contribution of the circuit is small.

In order to determine the voltage offsets between the channels, all different T/H channels were measured with the same ADC. The measured offsets are within ± 4 LSBs at 8 bit level. These are as expected and quite large, so offset calibration is needed. With this setup also the gain difference between the channels can be determined. The gain matching between the channels is ± 0.37dB, which is worse than expected. The cause of this is still under investigation.

The time alignment of the different channels was measured using the following setup. E.g. ADC1 is connected to T/H1 and ADC2 connected to T/H9. For good measurement accuracy an input signal close to the Nyquist frequency is used. From the outputs of both ADCs FFTs were calculated and the phase difference between the input signals was determined. Subtracting the phase differences due to the interleaving, the phase error and therefore the time-error can be calculated. Calculation of this phase error is very accurate because it is the average over 16,000 samples in an FFT, so the phase error due to jitter is averaged out. The RMS value of all channel offsets is 1.0 ps. The determined offset values can be used to investigate the behavior of a 16 times interleaved T/H with timing-offsets. A reconstructed FFT shows an SFDR of 44dB for an input signal at the Nyquist frequency. This will give some performance degradation, so calibration of this DC phenomenon can be considered. Measurements on other samples give comparable results.

In general a T/H consumes a large part of the total power of a complete ADC. To be able to place the power consumption of this interleaving T/H in perspective, a Figure of Merit is calculated in a similar way as for ADCs: FoM = P/(2^ENOB*fs). When leaving the gain and voltage offsets out of consideration, the FoM for this T/H is 0.1 pJ/Conversion. ADCs with samplerates in the order of 2GS/s have a FoM of well over 1 pJ/C. Combined with 16 moderate speed ADCs, which can have a FoM below 1pJ/C [5] this can result in a power efficient, high speed, high resolution ADC.

## 6. Conclusions

In this paper an interleaving T/H is presented. It consumes 32mW of power, has an ENOB of 7.6 bits and an ERBW of 1 GHz. The capacitive input load is smaller than 1pF and the FoM is 0.1 pJ/C.

Combining this interleaving T/H with efficient moderate speed converters can result in a high speed, high resolution ADC with low power consumption, making it very attractive for embedding in future applications.

## 7. Acknowledgements

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## 8. References

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