A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors

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***Abstract*— A completely integrated 1.8-GHz low-phase-noise voltage-controlled oscillator (VCO) has been realized in a standard silicon digital CMOS process. The design relies heavily on the integrated spiral inductors which have been realized with only two metal layers and without etching. The effects of high-frequency magnetic fields and losses in the heavily doped substrate have been simulated and modeled with finite-element analysis. The achieved phase noise is as low as −116 dBc/Hz at an offset frequency of 600 kHz, at a power consumption of only 6 mW. The VCO is tuned with standard available junction capacitances, resulting in a 250-MHz tuning range.**

***Index Terms*—CMOS analog integrated circuit, integrated inductor, phase noise, voltage-controlled oscillator.**

I. Introduction

DUE to the ever-growing importance of the mobile telecommunications market, the need for small, cheap, and low-power RF circuit components cannot be underestimated. By putting more and more functions on the same die, the feasibility of the single-chip transceiver has already been demonstrated [1]–[4]. One of the major challenges in the design of a cheap transceiver system is the frequency synthesis of the local oscillator (LO) signal.

Indeed, the specs for, e.g., the GSM or DCS-1800 system, require the ability to detect very small signals while very strong unwanted signals are present in the adjacent channels. If the LO signal in the receiver path has too much power at frequencies away from the wanted carrier signal, these strong interfering signals will also be mixed down, which will result in a contamination of the wanted received signal. A similar problem arises in the transmit path [5].

Frequency synthesis is usually done using a phase-locked loop (PLL). The general block diagram of a PLL is shown in Fig. 1. The feedback action in the loop causes the output frequency to be N times the reference frequency. This reference signal can be generated by a very stable, low-frequency crystal oscillator. The spectral purity of the synthesized signal will largely depend on the quality of the VCO signal [6]. Therefore, to ensure a LO with very low phase noise, a high-quality *LC*-tank is needed for the oscillator. Up to now, RF designers always had to use some external elements for this tank. If the required specs can be achieved with an internal *LC*-tank, this will aid in designing a low-cost transceiver system.

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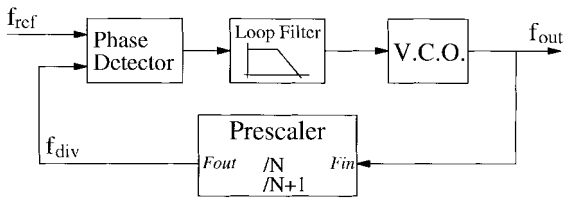


Fig. 1. PLL-based frequency synthesizer.

More recently, the possibilities of standard CMOS technologies for RF telecommunication circuit blocks have been proven in the design of low-noise amplifiers (LNA's) [7], down-conversion mixers [8], upconvertors [9], voltage-controlled oscillators (VCO's) [10], prescalers [11], [12], etc. Since the baseband signal processing is also done in this cheap technology, these designs have proven CMOS to be a promising candidate as the technology for future single-chip transceiver IC's.

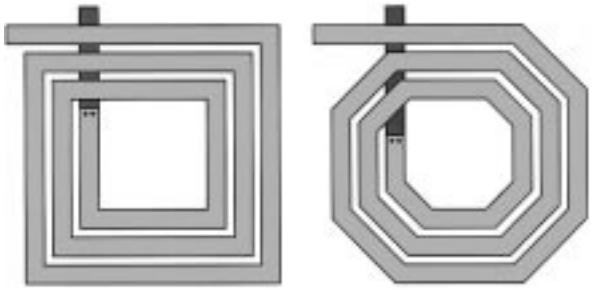
This paper presents a VCO design which uses integrated planar inductors in the resonance *LC*-tank, so no external elements are necessary. Moreover, a standard CMOS technology has been used with only two metal layers and a heavily doped substrate. The combination of these two aspects makes this a worst-case technology for designing VCO's, since only two metal layers means the spiral inductor will have a large series resistance compared to three- or four-level technologies, and the induced currents in the heavily doped substrate are an important source of extra losses.

The possibilities for and problems associated with silicon integrated inductors are discussed in Section II. To accurately quantify the losses present in spiral inductors, a finite-element simulation strategy is used. The results obtained are analyzed in Section III. The oscillator circuit design is discussed in Section IV. Finally, Sections V and VI give the measured performance and some conclusions.

II. Silicon Integrated Inductors

The key to the design of a low-phase-noise oscillator is a high-quality inductor [13]. Unlike capacitors, inductors are not readily available in a standard CMOS technology. As a result, some design tricks have to be used, which usually limit the performance of the inductor.

Active inductors use some active elements to transform the impedance of a capacitor to an inductive impedance. High-frequency operation is possible [14], and the fact that the inductance can be tuned is very advantageous in the design of a VCO. However, the noise generated by the active elements



(a) (b)

Fig. 2. Spiral inductor layout: (a) square and (b) octagonal.

requires the use of an excessive amount of power to achieve low-noise specs [13].

Recently, the feasibility of oscillators based on the inductance of a bondwire has been proven. The very low series resistance of gold bondwires allows the achievement of the unmatched phase noise performance of -115 dBc/Hz at 200 kHz offset from the 1.8-GHz carrier [10]. Bondwires are readily available in any IC technology, and can therefore be regarded as being a standard CMOS technology feature. However, because manufacturers cannot guarantee issues such as yield or repeatability of the bonding process, the semiconductor industry is still hesitant to use this technique.

The only option left is to lay out a rectangular spiral metal trace on the silicon substrate, using one or more of the standard metal interconnection levels available, as shown in Fig. 2(a). The basics for the inductance calculation of these planar inductors were developed by Greenhouse in 1974 [15]. If the technology allows 45° routing, an octagonal shape can be used [Fig. 2(b)]. Of course, a lot of parasitic effects limit the possible applications of spiral coils.

The quality factor of the inductor will be limited by the series resistance of the metal traces. Typical values in a simple process are 15 Ω for a 10-nH inductor [16]. GaAs circuits, which incorporate a lot of planar inductors, have the advantage of gold interconnects to achieve low series resistance. In silicon, most designers use very wide metal turns and several routing levels in a multilayer process to obtain a low series resistance [17], [18]. However, we will show in the next section that due to high-frequency magnetic field effects (such as the well-known skin effect), this is not necessarily the best solution.

One of the most recognized parasitics is the capacitance to the substrate. Together with the wanted inductance, this gives an *LC* resonance frequency above which the coil can no longer be used as an inductor. A typical value for the self-resonance frequency is 2.5 GHz for a 10-nH inductor [16]. This puts a limit on the maximal inductance value achievable at a certain frequency, as larger inductors require a larger area and thus also a larger capacitance and a smaller self-resonance frequency. Special processing technologies exist that create an air-gap underneath the inductor, or have very thick oxide under their top metal routing level [19]. The resulting smaller parasitic capacitance allows higher operating frequencies.

More recently, another solution for the self-resonance problem has been developed. By using selective etching techniques, the silicon substrate can be removed in a post-processing step from underneath the inductor, either by etching from the top of the wafer [20], [21], or from the back of the wafer [17]. This removes the capacitance to the substrate, and shifts the self-resonance frequency of a 100-nH inductor from 0.8 GHz to 3 GHz [20]. But more important, this technique also eliminates the resistive losses in the substrate. However, this requires extra nonstandard processing steps, and as a result, the industry is very hesitant to adopt those techniques.

The resistive losses in the substrate are indeed the most important limitation in using planar inductors in a standard CMOS process. Most bipolar or BiCMOS technologies use a lowly doped substrate, resulting in a substrate resistivity in the order of 10 Ωcm. Most submicron CMOS technologies however use epiwafers. They consist of a lowly doped epilayer, in which the transistors are situated on top of a heavily doped substrate. The resistivity in the substrate is in the order of 0.01 Ωcm. The reason for this low resistance is to diminish the effects of hot-electron induced substrate currents, prevent digital circuits from disturbing sensitive analog circuits, etc. A large drawback of these heavily doped substrates is the fact that now currents in the substrate, which are generated by the magnetic field of the inductor, are free to flow, as will be shown by the finite-element simulations in Section III-B. This severely increases the losses and reduces the inductance value.

III. Finite-Element Simulations

The goal of this design is to prove the feasibility of planar inductors for the design of standard CMOS VCO's. The technology used has only two metal layers and a heavily doped substrate. Post-processing is not accepted by industry, and etching the substrate away underneath the inductor cannot be regarded as being a standard CMOS technology. To make a completely monolithic standard CMOS VCO, the effect of the conductive substrate must be included in the design.

From the discussion in the previous section, we can conclude that spiral inductors suffer from three parasitic effects. First, parasitic capacitance to the substrate causes the inductor to self-resonate at a certain frequency. Second, the high-frequency series resistance will differ from the calculated one due to skin effect and other magnetic field effects. Third, the losses in the heavily doped substrate cause a large degradation in the overall quality factor and reduce the inductance value.

In order to better understand these effects, an efficient simulation strategy has been used. Simulation is necessary because the problem is much too complex to be solved analytically. The only way to fully simulate all the effects is a full three-dimensional (3-D) finite-element simulation. That is, however, very time-consuming. We want to gain some insight in the severity of the several parasitic effects as a function of coil geometry by simulating many different coils. This should lead to some general design guidelines for planar inductors. Therefore, simulation must be done as fast as possible. Planar two-dimensional (2-D) or so-called 2.5-D simulators work very fast and can operate on complex coil geometries. But these are not sufficient for the problem, because they do not account completely for the substrate effects.

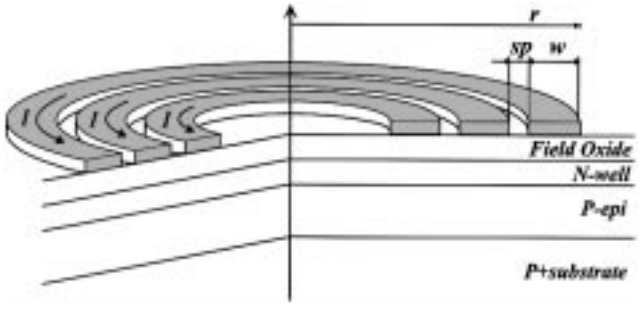


Fig. 3. Cross section of a circular inductor.

We have chosen to simulate circular inductors instead of square coils. Circular inductors offer the advantage of being symmetrical around the vertical axis, and the problem therefore only has a 2-D complexity. Two-dimensional simulation can be done very fast. The simulated structure is shown in Fig. 3. The coil has n metal turns, an outer radius r, conductor width w, and spacing sp between the conductors. The substrate consists of a heavily doped bulk material, a lowly doped epilayer, and an n-well (or p-well) layer. On top of this is the field oxide. A current of a certain frequency is forced through the coil, and the resulting magnetic field and all resistive losses are calculated. This simulation was done with the commercially available program MagNet [22] and takes approximately 10 to 15 min per inductor. This gives us a very fast way to calculate the inductance and the equivalent series resistance of several coil geometries. We can make a distinction between losses in the metal conductors and losses in the silicon. That way, we can gain insight in the several parasitic effects in the metal conductors and in the substrate. The conclusions drawn from these simulations are now discussed.

A. Metal Losses

At low frequencies, the series resistance of the metal conductor traces can easily be calculated as the product of the sheet resistance and the number of squares of the metal trace. At high frequencies, however, the skin effect and other magnetic field effects will cause a nonuniform current distribution in the inductor. This will have a (sometimes serious) influence on the losses in the metal conductor at high frequencies.

The best known of these effects is the skin effect. It can be analyzed analytically for a straight metal conductor with circular cross section. Instead of using the full area for current flow, the current is pushed to the outside of the conductor at high frequencies. This is shown schematically in Fig. 4. A skin depth δ is defined as being the equivalent thickness of a hollow conductor that has the same high-frequency resistance

$$\delta = \sqrt{\frac{2}{\mu \cdot \sigma \cdot \omega}} \tag{1}$$

with μ the magnetic permeability of the material, σ the resistivity, and ω the frequency of interest. In the planar inductor, this effect can no longer be calculated analytically, but it is clearly seen in the finite-element simulations.

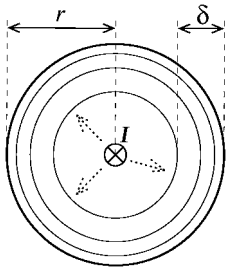


Fig. 4. Skin effect in a straight conductor with circular cross section.

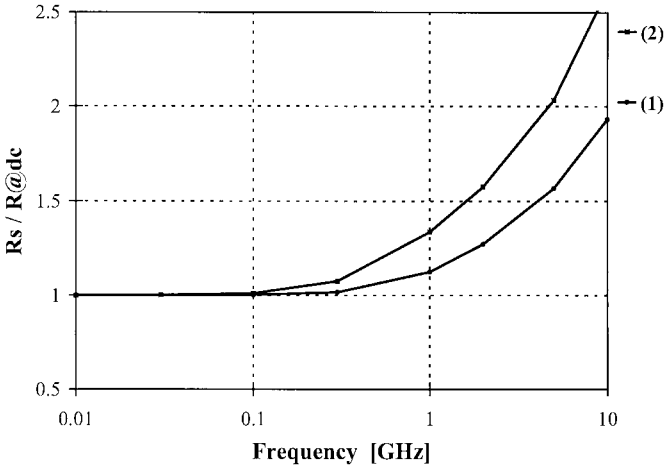


Fig. 5. Influence of the skin effect on planar inductors.

As an example, two inductor geometries are simulated, one with parameters $n = 2$, $r = 116$ μm, $w = 15$ μm, $sp = 2$ μm, and one with parameters $n = 2$, $r = 151$ μm, $w = 30$ μm, $sp = 2$ μm. So the second inductor has metal turns which are twice as wide as the first one. The radius has been adjusted in order to achieve approximately the same inductance value. The wide metal turns should allow a low series resistance and hence low phase noise in the oscillator. Due to the larger radius r, the resistor ratio is not as large as two, but equals 1.67. Since the phase noise of an *LC*-oscillator is proportional to the equivalent series resistance of the *LC*-tank [13], a $10 \cdot \log(1.67) = 2.2$ dB better phase noise performance is possible with the second coil. Fig. 5 shows the variation of the metal series resistance as a function of frequency. The ratio $Rs/R@dc$ is drawn, i.e., the ratio between the effective series resistance at a certain frequency and the resistance at dc. At 2 GHz, the series resistance of the second inductor (2) is already 60% higher than the value at dc, while the first one (1) only suffers a 30% increase. Therefore, the difference in resistance between the two inductors is now only a factor 1.35, or 1.3 dB. The inductance value remains roughly unchanged for both. At even higher frequencies, the resistance increase is enormous.

This proves that inductors using very wide metal turns are not the way to go in designing low-phase-noise oscillators. Due to the larger required coil radius when using wide turns to maintain the inductance value, the phase noise does not decrease linearly with conductor width. This is even enhanced

TABLE I
INDIVIDUAL SERIES RESISTANCE PER METAL TRACE

Freq.	L	R_{Al}	Resistance per metal trace [Ω]								
[GHz]	[nH]	[Ω]	R1	R2	R3	R4	R5	R6	R7	R8	R9
0.01	6.84	5.39	1.031	0.923	0.815	0.707	0.599	0.490	0.382	0.273	0.163
0.03	6.84	5.39	1.031	0.923	0.815	0.707	0.599	0.490	0.382	0.273	0.163
0.10	6.84	5.40	1.032	0.923	0.815	0.708	0.600	0.492	0.384	0.275	0.166
0.30	6.84	5.50	1.038	0.924	0.818	0.716	0.611	0.508	0.403	0.297	0.188
1.00	6.80	6.61	1.095	0.928	0.849	0.790	0.734	0.673	0.605	0.524	0.415
2.00	6.68	9.44	1.213	0.942	0.933	0.989	1.057	1.111	1.132	1.115	0.947
5.00	6.39	18.36	1.466	1.027	1.229	1.685	2.158	2.594	2.821	2.987	2.396
10.00	6.18	30.19	1.750	1.195	1.676	2.705	3.680	4.663	5.006	5.432	4.080

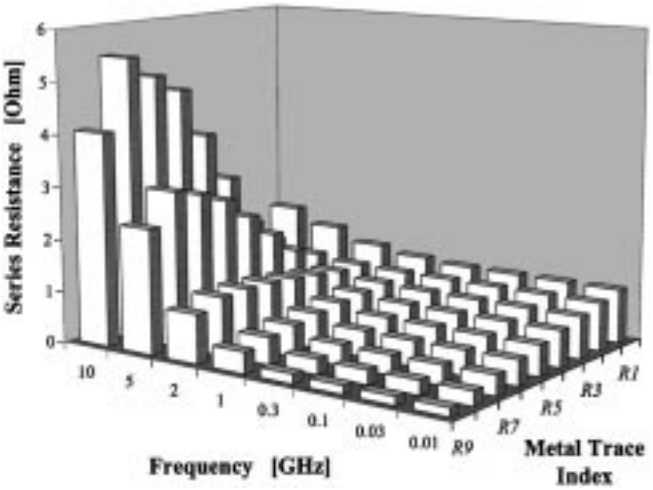


Fig. 6. Individual series resistance per metal trace.

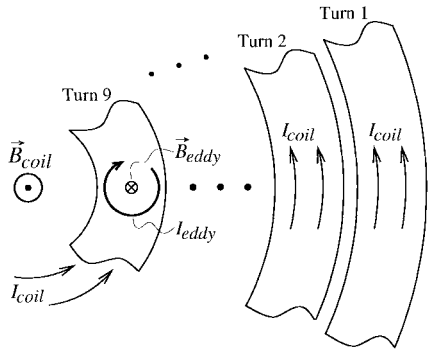


Fig. 7. Generation of eddy currents in planar inductors.

by the skin effect which seriously deteriorates the series resistance of wide conductors at high frequencies.

If we look at the individual resistance of each metal turn, we notice another, even more important, effect. Normally, we should expect a high resistance at the outer turns, because they are the longest, which then gradually decreases for the inner turns. However, an unexpected dependence results from the finite-element simulations. An inductor with parameters $n = 9$, $r = 100$ μm, $w = 9$ μm, and $sp = 1$ μm was simulated at several frequencies. Table I gives, as a function of frequency, the inductance value L, the total metal series resistance R_{Al}, and the individual resistance $R1 \cdots R9$ of each turn. $R1$ is the resistance of the outer turn, $R9$ the innermost one. Fig. 6 gives a 3-D graphical representation of the data in Table I. This data shows that at high frequencies, the largest contribution to the series resistance does not come from the longer outer turns, but from the inner turns! $R1$ increases from 1.03 Ω at low frequencies to 1.21 Ω at 2 GHz, or by 18%. The increase in $R9$ is from 0.16 Ω to 0.95 Ω, or 480%! This enormous difference cannot be explained by the skin effect in a single metal trace alone, since both traces are of equal width and they should suffer to the same amount from the nonuniform current distribution.

The cause for this phenomenon can be found in the generation of eddy currents in the inner conductors, as shown in Fig. 7. A part of the right half of the circular inductor is shown schematically, from the outer turn 1 to the inner turn 9. The inductor carries a current I_{coil}, which flows in the direction as indicated in the outer turns in the figure. This current of course has an associated magnetic field B_{coil}, which has a maximum intensity in the center of the coil. The magnetic field is oriented perpendicular to the page, in the direction coming out of the page (indicated by the symbol $\odot$).

When the spiral inductor is filled with turns up to the center of the coil, a large part of the magnetic field does not pass through the center of the coil but goes through those inner turns. Due to the time-varying nature of the coil current, the generated magnetic field B_{coil} also varies with time. According to the law of Faraday–Lenz, an electrical field is magnetically induced in the inner turns that will generate circular eddy currents I_{eddy} as indicated in Fig. 7. The direction of these eddy currents is such that they oppose the original change in magnetic field. So the magnetic field B_{eddy} resulting from the eddy currents has a direction flowing into the page (indicated by the symbol $\otimes$). The magnitude of the induced electrical field is proportional to the derivative of $B(t)$ to time, so the effect is only noticed at high frequencies. As the total magnetic field ($= B_{\text{coil}} + B_{\text{eddy}}$) will be smaller, the inductance value will decrease at high frequencies, as noticed in Table I.

These eddy currents again cause a nonuniform current flow in the inner coil turns. On the inner side of the inner turn, coil current I_{coil} and eddy current I_{eddy} flow in the same direction, so the current density is larger than average. At the outer side, both currents cancel and the current density is smaller

than average. As a result, the current in the inner turns is pushed to the inside of the conductor. This can clearly be seen when analyzing the results of the finite-element simulation. In extreme conditions, the magnitude of the eddy currents is even larger than the coil current, making the current density on the outside of the inner turn negative, i.e., current is flowing in the "wrong" direction.

One might be able to prevent these eddy currents to flow by making longitudinal stripes in the inner conductors, or perhaps by making the inner turns less wide than the outer ones. However, the effects of such countermeasures are questionable, since they will result in a higher dc resistance of the inner turns. These turns already have a low contribution to the inductance because of the small area they enclose, so even without the eddy currents they cause a (slight) deterioration of the overall quality factor. So it is best if the inner turns are completely omitted, i.e., one should leave a hole in the middle of the spiral coil.

To conclude the discussion on the losses in the metal conductors of a planar inductor, we can safely say that the interactions of skin effect and eddy currents seem far too complex to be analyzed analytically, so the only possible solution to predict the high-frequency metal series resistance is finite-element simulation. As a general rule, it can be stated that conductor width should be limited because of the skin effect, but most important, a "hollow" coil should be used. The inner turns already have a low contribution to the inductance, because of the small area they enclose, and they suffer from an incredible increase in series resistance due to eddy currents at high frequencies. In order to prevent deterioration of the overall quality factor of the inductor, they must be left out of the coil.

B. Substrate Losses

As stated earlier, a major drawback of most submicron CMOS technologies is the use of epiwafers which have a heavily doped substrate. In these substrates, currents induced by the magnetic field of the inductor are free to flow, which is the cause for extra resistive losses and a decrease in inductance value.

This is show in Fig. 8. This figure schematically shows a vertical cross section of the inductor, including the underlying substrate. At the projected instance of time, the inductor current I flows into the page on the right (symbol $\otimes$) and out of the page on the left (symbol $\odot$). As for the eddy currents in the inner conductors, here the law of Faraday–Lenz implies that an electrical field is magnetically induced in an imaginary coil in the substrate underneath the inductor. Therefore, a current I_{subs} will flow in the substrate. The direction of this induced current is such that it opposes the original change in magnetic field. So it flows in a direction opposite to the current in the inductor, as indicated in the figure.

In a substrate with a high resistivity, the induced electrical field only causes a small amount of current I_{subs} to flow, and the effect of the substrate currents can be neglected [16]. The quality factor of the inductor is than completely determined by the losses in the metal conductors. Finite-element simulations

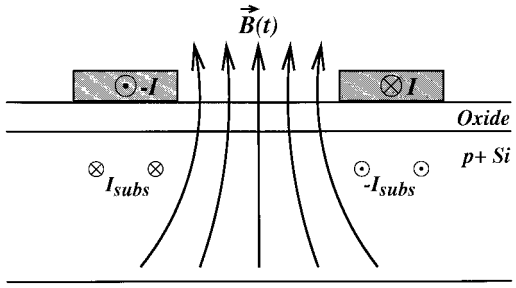


Fig. 8. Generation of substrate currents on planar inductors.

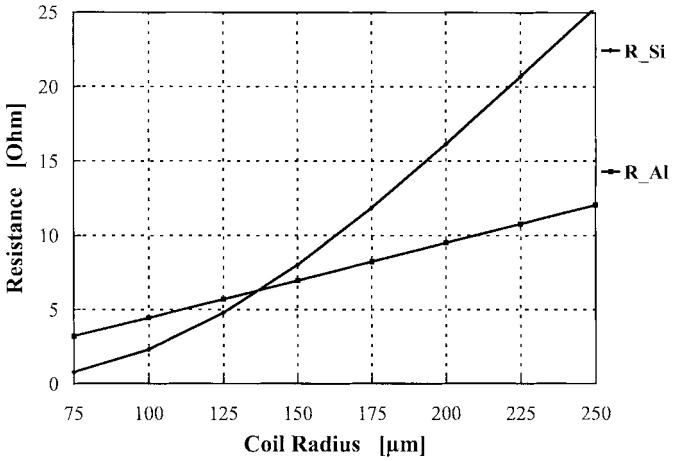


Fig. 9. Resistive losses in the metal traces and in the substrate for planar inductors on heavily doped substrates.

of coils in such a process indicate that values larger than ten can be achieved.

In our case, the losses in the heavily doped substrate prevent the realization of such high quality factors. This is demonstrated in Fig. 9. A coil with four turns, having a width $w = 9\ \mu$m and spacing $sp = 1\ \mu$m, is simulated at a frequency of 2 GHz for different radii r. Fig. 9 shows the metal series resistance R_{Al} and the silicon series resistance R_{Si}. This is an equivalent series resistance which models the losses of the induced substrate currents. As the length of the metal trace becomes longer, R_{Al} increases gradually. The silicon losses show a completely different curve. For small coils, the metal losses dominate, so the quality factor will be determined by R_{Al}. For the largest coil, the metal resistance is 12.1 Ω, whereas the silicon resistance is increased to a value as large as 20.7 Ω. Without the silicon losses, the quality factor would be $2\pi \cdot 2$ GHz $\cdot 13.7$ nH $/12.1\Omega = 14$. This is decreased to only five due to the substrate currents. At lower frequencies, the effect is less severe since the changes in the magnetic field are slower.

The inductance value L also suffers from the substrate currents. Since these currents flow in the opposite direction from the current in the coil, the total magnetic field magnitude will be smaller. Since the inductance value can be defined as the ratio between total magnetic flux and coil current, the inductance of the coil will be reduced. For the largest coil with radius $r = 250\ \mu$m, the substrate currents decrease the value of L with approximately 10%.

Again, analytically analyzing this effect seems impossible. Therefore, the only way to date to make a safe design is the use of finite-element simulation. A general guideline is to limit the area of the coil. As can be seen from the simulation data of Fig. 9, the effect is far less severe for coils with a small radius r. This can be explained by the fact that for small coils, the magnetic field penetrates less deep into the substrate and therefore has less effect. Changing the distance from the substrate, as can be done for an inductor using the third or fourth metal level, does not effect this, since the change in oxide thickness will always be negligible compared to the depth of magnetic field penetration into the substrate.

IV. Oscillator Design

In this section, the design of a low-phase-noise VCO using planar inductors will be discussed. The center frequency is chosen to be around 1.8 GHz, and a compromise between noise, power consumption, and tuning range is made.

A. Hollow Coil Design

From the discussion in the previous paragraph, we can remember three general design guidelines.

1) *Limit the width of the metal conductors*: due to the skin effect, the center of a wide conductor will not by used for current flow. So very wide metal conductors are not efficient.
2) *Do not fill the inductor up to the center*: due to the generation of eddy currents at high frequencies, the innermost turns of the coil suffer from an enormous increase in resistance, while their contribution to the inductance value is minimal. The overall quality factor is deteriorated. So it is necessary to use a *hollow coil*.
3) *Limit the area occupied by the coil*: at high frequencies, the magnetic field generated by the inductor induces currents in the substrate which cause extra resistive losses and a decrease in inductance value. The magnetic field of small coils penetrates less deep into the substrate, and the effect is less severe. So very large coils are not efficient.

For the design of the oscillator coil, several considerations must be made. Of course, the losses of the coil must be as low as possible for low noise and low power. One could use a tiny coil for this, or one with only one turn, since this will certainly have small resistance. But the power required for a stable oscillation is proportional to $R_{\text{eff}} \cdot (\omega_0 C)^2$, where R_{eff} is the total equivalent series resistance of the *LC*-tank, ω_0 is the oscillation frequency, and C is the required capacitance value [13]. So using a too small inductance value will require a large capacitance to set the desired frequency, and hence a large power consumption will result. But the inductance value cannot be made very high either. Then the required capacitance value will be almost achieved with the parasitics of the coil and the amplifying transistors alone. This leaves no room for an extra tunable junction capacitance, so the tuning range will be small.

Due to the efficient finite-element simulation strategy of circular coil, we were able to evaluate a lot of possible coils.

TABLE II
Optimal Coil Parameters

Radius	r	85 μm
Width	w	8.5 μm
Spacing	sp	1.5 μm
No. of Turns	n	4
Substrate Resistivity	ρ_{subs}	0.01 Ωcm
Field Oxide Thickness	t_{ox}	0.7 μm
Metal1 Resistance	$R_{\square,M1}$	50 $m\Omega/\square$
Metal2 Resistance	$R_{\square,M2}$	35 $m\Omega/\square$
Inductance	L	3.2 nH
Metal Losses	R_{Al}	4.60 Ω
Silicon Losses	R_{Si}	1.75 Ω
Quality Factor	Q	5.7

This allows us to gain insight in the different tradeoffs between coil radius r, conductor width w, and number of turns n. For the relatively small inductance values that are aimed at, fringing capacitance between the several conductor traces is negligible. So the conductor spacing sp should be chosen minimal. Both metal levels are used in parallel, except for the connection to the inner turn, which is done in Metal1. The parameters of the final optimal geometry for our problem are given in Table II. With an inductance value of 3.2 nH, a quality factor as large as 5.7 is achieved. These values are not the exact values given by the finite-element simulator, but were adjusted manually to account for the extra inductance and resistance caused by the connection leads. A more exact way than doing this manually would be to perform a 2-D planar simulation to investigate the effect of these connection leads. In a silicon layout, the circular coil can be adequately approximated by an octagonal shape. The size of this octagon is chosen such that the average radius is 85 μm.

B. Amplifier Design

The oscillator circuit schematic is shown in Fig. 10. Two of the optimized hollow coils are used in series in a differential configuration. Two NMOS transistors $M1$ and $M2$ are coupled in positive feedback to provide a negative resistance. This schematic allows for a very low power supply voltage. The minimum power supply is $V_{DSat,M3} + V_{GS,M1}$.

With an inductance value of 3.2 nH, the total capacitance on each node must be 2.4 pF to obtain an oscillation frequency of 1.8 GHz. The *LC*-tank's effective resistance will be, including the parasitic resistances of the capacitors, approximately 15 Ω. So the required negative conductance provided by the transistors must be $15\ \Omega \times (2\pi \times 1.8\ \text{GHz} \times 1.2\ \text{pF})^2 = 3$ ms. Using a safety factor of two, each of the amplifying transistors must have a transconductance g_m of 12 ms.

The capacitor of the *LC*-tank is formed by the inductor's parasitic capacitance to the substrate, the drain-bulk, gate-drain and gate-source capacitances of the NMOS transistors, and a tunable p+/n-well junction capacitor. In order to achieve a large tuning range, this last contribution must be as large as possible.

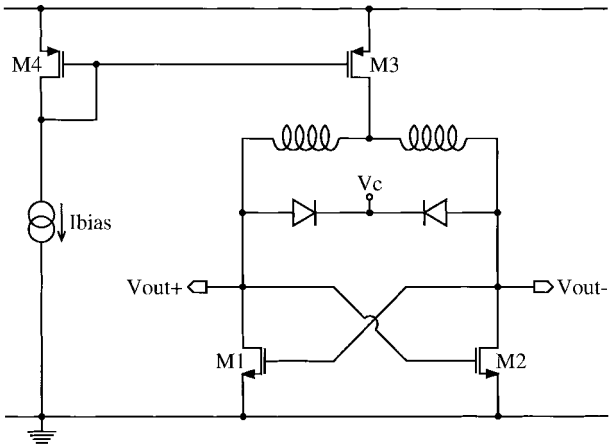


Fig. 10. Oscillator circuit schematic.

The parasitic capacitance of the coil is only 0.2 pF because of the small dimensions used. This leaves 2.2 pF to be divided between the transistors' parasitics and the tuning capacitor. For a minimum gate length transistor (i.e., 0.7 μm), the sum of drain-bulk, gate-drain, and gate-source capacitance in this technology approximately equals 3 fF per μm gate length. Very small values of $V_{GS} - V_T$ for $M1$ and $M2$ would yield a large transconductance-to-current ratio and hence a small power consumption. However, in that case, the transistor sizes and hence its parasitic capacitance becomes too large and the tuning range will be small. In this design, a $V_{GS} - V_T$ value of 0.3 V has been chosen. This yields a width of 400 μm for transistors $M1$ and $M2$ and a total current drain of 4 mA. With the power supply of 1.5 V, this results in only 6 mW total power consumption. With an oscillation amplitude of approximately 1.1 $V_{\text{peak,diff}}$, the expected phase noise can be calculated to be [13]

$$\mathcal{L}\{\Delta\omega\} = \frac{kT \cdot R_{\text{eff}} \cdot [1+A] \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2}{P_{\text{signal}}} \tag{2}$$

where R_{eff} is the total equivalent series resistance of the *LC*-tank (15 Ω), A is the excess noise factor of the amplifier (which equals two in this design), ω_0 is the oscillation frequency, $\Delta\omega$ is the frequency offset from the carrier, and P_{signal} is the power of the carrier signal. This results in a phase noise at 600 kHz offset of

$$\begin{aligned}\mathcal{L}\{600\text{ kHz}\} &= \frac{kT \cdot 15\Omega \cdot [1+2] \cdot \left(\frac{1.8\text{ GHz}}{600\text{ kHz}}\right)^2}{\frac{1.1V^2}{2}} \\ &= 2.75 \cdot 10^{-12} \\ &= -115.6\text{ dBc/Hz}. \end{aligned} \tag{3}$$

The 1-pF tunable junction capacitor is made as a p+ active area in an n-well. Its capacitance can be tuned with the control voltage V_C, which controls the bias voltage of the n-well. Since this n-well is a common-mode node, its parasitic capacitance to the substrate is not important. Of course, the layout of this junction capacitor is very important. Care must be taken to limit the series resistance, and to keep the symmetry which guarantees the common-mode nature of the n-well.

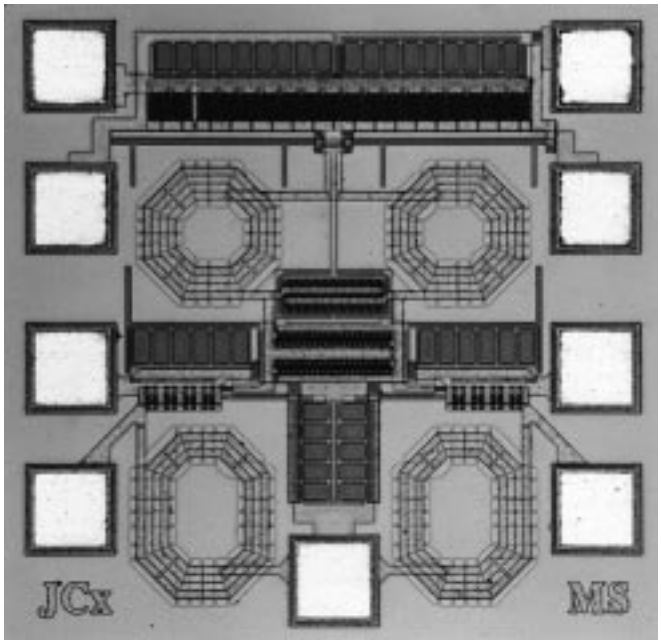


Fig. 11. IC microphotograph.

V. Measurement Results

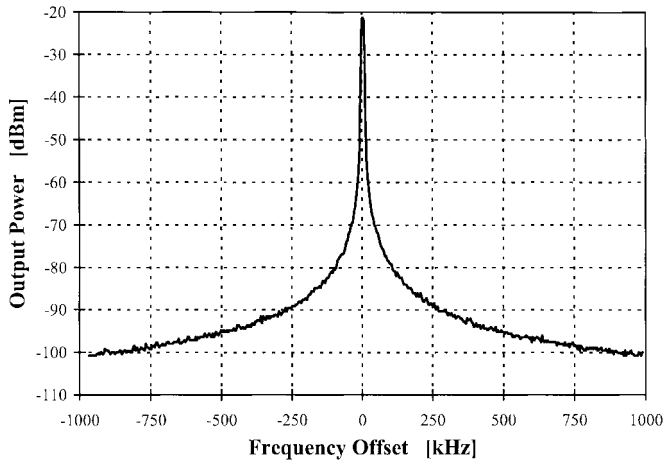
A microphotograph of the VCO is shown in Fig. 11. The die measures 750 × 750 μm^2. The two oscillator coils are situated on the top. The other coils are used as loads for the measurement output buffers. These output buffers are simple common-source transistors with an inductive load to compensate for the bondpad parasitics. The tunable capacitors and the amplifying transistors are placed in the middle of the die.

The free-running oscillation frequency is 1.81 GHz, which is only 4% off from the predicted value of 1.88 GHz. As said earlier, performing an analysis of the effects of the coil connection leads with a planar 2-D simulator might have resulted in an even better prediction of the center frequency. The oscillator operates from a 1.5-V power supply and consumes only 4 mA. The measured output spectrum is shown in Fig. 12(a). The center frequency is 1.81 GHz and the resolution bandwidth is 10 kHz. A logarithmic plot of the phase noise is given in Fig. 12(b). The resulting phase noise is −116 dBc/Hz at 600 kHz offset, which agrees very well with the theoretical value. For offset frequencies large than 100 kHz, the phase noise decreases with a slope of 20 dB/dec. This shows that $1/f$ noise only becomes important below 100 kHz offset.

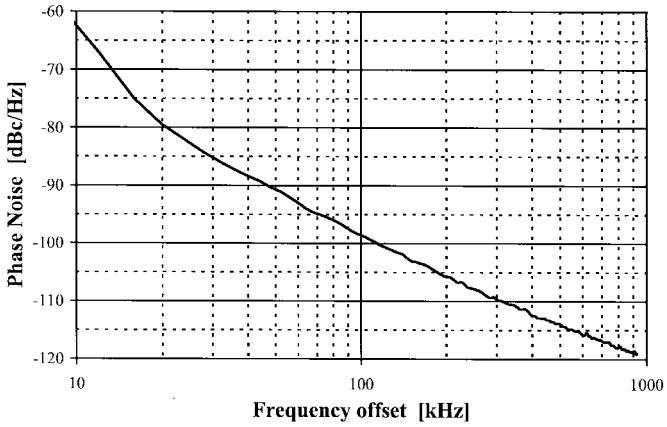
The frequency tuning with control voltage V_C is shown in Fig. 13. The voltage can be put as low as 0.5 V, to a point where the p+/n-well junction becomes slightly forward biased. At that time, the phase noise is approximately 3 dB worse than the result shown in Fig. 12. Two facts explain this. First, the total capacitance of the *LC*-tank becomes larger, in order to lower the oscillation frequency. This increases the transconductance required to maintain oscillation. Since there is no amplitude control implemented in this VCO, the negative resistance implemented by the transistors $M1$ and $M2$ remains the same. This causes a 1-dB decrease in oscillation amplitude

TABLE III
COMPARISON OF SEVERAL PLANAR-INDUCTOR OSCILLATORS

Design	Technology	Freq.	Power	Tuning Range	Phase noise $[dBc/Hz]$	
	[-]	[GHz]	[mW]	[%]	reported	equivalent
Ref. [23]	10GHz Bip	1.8	70	10	-88 @ $100kHz$	-104
Ref. [17]	1-μm CMOS	1.0	16	0	-95 @ $100kHz$	-105
Ref. [18]	12GHz BiCMOS	2.4	54	0	-92 @ $100kHz$	-110
Ref. [24]	25GHz Bip	0.9	10	N.A.	-101 @ $100kHz$	-110
Ref. [21]	1-μm CMOS	0.9	10..40	14	-85 @ $100kHz$	-95
Ref. [19]	0.5-μm BiCMOS	4.0	12	9	-106 @ $1MHz$	-109
This work	0.7-μm CMOS	1.8	6	14		-116



(a)



(b)

Fig. 12. (a) Oscillator output spectrum and (b) phase noise logarithmic plot.

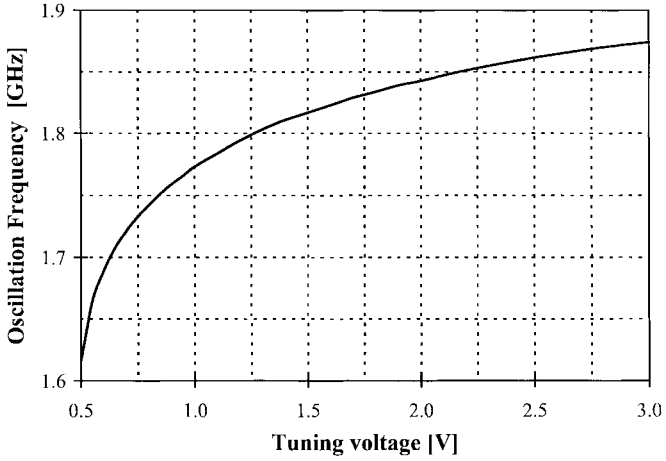


Fig. 13. VCO tuning characteristic.

and thus in phase noise. The other 2 dB loss is probably caused by increasing losses in the almost-forward-biased junction capacitors.

Table III gives a comparison of some recently published oscillators using planar inductors in their *LC*-tank. The frequency, power, tuning range, and phase noise are listed. For the phase noise, two numbers are given. In the first column, the phase noise at a certain offset from the actual frequency as reported in the reference is given. To compare these numbers, the last column gives the value of the phase noise, recalculated to an equivalent offset frequency of 600 kHz from a 1.8-GHz carrier, assuming a dependence of 20 dB per decade on offset frequency. Although some of the designs use exotic technology steps such as substrate etching or very thick conductors on a very thick oxide, the presented design achieves an improvement of 6 dB in phase noise over all other designs, while consuming minimal power. Actually, the only monolithic oscillator which outperforms this design in phase noise is the bondwire oscillator presented earlier [10]. This improvement must be contributed to the thorough analysis of the planar inductor with finite-element simulations.

VI. CONCLUSIONS

A low-phase-noise integrated VCO with "hollow" planar inductors is reported. The parasitics associated with planar inductors on conductive substrates, such as skin and other magnetic field effects and substrate losses, are analyzed qualitatively and quantitatively using a very efficient finite-element simulation strategy. The optimized coil uses four turns, has a radius $r = 85$ μm and conductor width $w = 8.5$ μm. The quality factor equals 5.7.

This coil has been used in a 1.8-GHz VCO that achieves the very low phase noise of -116 dBc/Hz at 600 kHz offset. Compared to other designs, a 6-dB improvement has been realized. Furthermore, this has been achieved in a standard double-metal CMOS technology with a heavily doped substrate without any

extra processing steps, such as substrate etching, being used. The VCO consumes 4 mA from a 1.5-V power supply. The tuning range is as large as 14%.

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