A 1.8-V $\Delta\Sigma$ Modulator Interface for an Electret Microphone With On-Chip Reference

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***Abstract*—The design of a delta–sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) for direct voltage readout of an electret microphone is presented. The ADC is integrated on the same chip with a bandgap voltage reference and is designed to be packaged together with an electret microphone. Having a power consumption of 1.7 mW from a supply voltage of 1.8 V, the circuit is well suited for use in mobile applications. The single-loop, single-bit, fourth-order $\Delta\Sigma$ ADC operates at 64 times oversampling for a signal bandwidth of 11 kHz. The measured dynamic range is 80 dB and the peak signal-to-(noise+distortion) ratio is 62 dB. The harmonic distortion is minimized by using an integrator with an instrumentation amplifier-like input which directly integrates the 125-mV peak single-ended voltage generated by the microphone. A combined continuous-time/switched-capacitor design is used to minimize power consumption.**

***Index Terms*—Analog-to-digital conversion, CMOS analog IC, continuous time, delta–sigma modulator, electret microphone, high input impedance, low-voltage bandgap reference, single-ended input, switched capacitor.**

I. Introduction

HIGH-PERFORMANCE CMOS processes are currently evolving toward increased switching speeds and transistor densities. Even if this evolution is driven by the needs of digital circuits, the performance versus cost ratio of analog circuits is also increasing [1], [2], though at a slower rate. In systems-on-chip, a large digital section can perform high-complexity data processing at high speeds while the analog circuits provide high-performance data conversion, in many cases without the need for pre-/post-conditioning of analog signals.

Integration of the analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) on the same chip with the digital signal processor is usually desired to reduce the overall system cost. However, there are cases where distributing the ADCs outside the main chip set can *improve* performance and *reduce* system costs. This is generally the case with specially packaged sensors [3].

The audio input device most used in telephony these days, the electret microphone, is such a specially packaged sensor. Fig. 1(a) shows the structure of an electret microphone. It consists of a variable capacitor, with one fixed plate and one flexible plate which bends under the pressure of sound. The fixed plate is covered with an electret layer which has a built-in charge resulting in an electric field of 200–300 V. Thus the microphone works as a high-impedance voltage generator, as shown in Fig. 1(b) by its electrical model. The microphone's output voltage V_{EM} depends on its geometry and the materials used [4]. The silicon chip IC placed inside the microphone package contains an FET which is used as a high input-impedance amplifier.

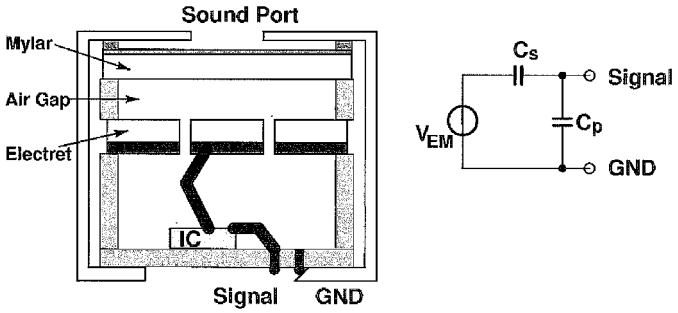

Fig. 1. Electret microphone model.

A schematic of the A/D conversion chain presently used in mobile phones is shown in Fig. 2(a). The JFET packaged along with the microphone M is used as a voltage-to-current converter. The signal is ac coupled to the *Codec* chip by a large-valued capacitor C. The cost of the system can be reduced by integrating R along with the JFET and designing new *Codec* chips that can be connected directly to the JFET drain [5]. However, two other disadvantages of this system remain. At approximately 60-dB dynamic range and 1% total harmonic distortion, the performance is limited by the JFET's noise and nonlinearity, even when this is biased at a relatively high drain current. The analog signal at the JFET drain is also sensitive to externally generated electrical noise.

In this paper, a different approach to analog-to-digital conversion of electret microphone signals is presented. The concept is illustrated in Fig. 2(b). The JFET is replaced by a chip containing an ADC and a voltage reference. The ADC is connected directly to the microphone, without making use of an amplifier or filter for signal conditioning. The voltage reference is placed on the same chip, so no sensitive analog connections are taken outside the metal package. The only needed external connections, besides ground and supply, are the digital *Clock* input and 1-bit *Data* output.

The next section gives a high-level description of the designed one-chip system. Section III covers the design aspects of the $\Delta\Sigma$ modulator, both at the behavioral level and at circuit level. In Section IV, the design of the on-chip low-voltage bandgap reference is explained. Conversion nonlinearity is analyzed in Section V. Section VI presents experimental results and the conclusions are drawn in Section VII.

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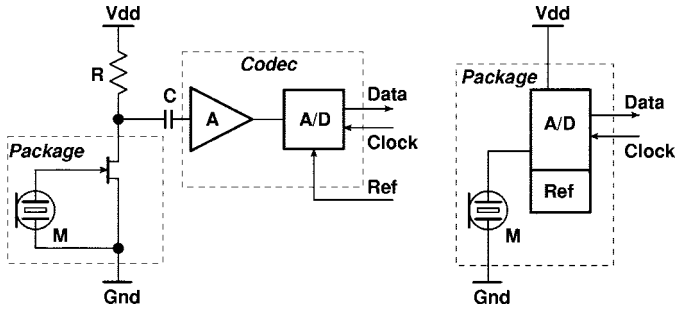

Fig. 2. (a) Conventional and (b) new approach for A/D conversion of an electret microphone signal.

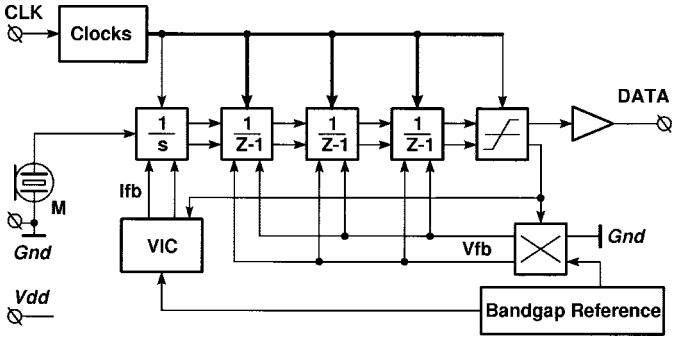

Fig. 3. System-level schematic of the digital microphone chip.

II. System Design

The small number of available pins and the need for a high conversion resolution at audio frequencies makes the choice of a $\Delta\Sigma$ modulator the most suitable one for this application. The design challenges at system level consist of connecting the $\Delta\Sigma$ modulator directly to the microphone and to the on-chip voltage reference without making use of high-power amplifiers or buffers.

A system-level schematic of the chip is shown in Fig. 3. A fourth-order, single-loop $\Delta\Sigma$ modulator performs the function of A/D conversion. Only one bit of data is delivered at the output on each clock cycle, therefore a single-bit quantizer is used. A large oversampling ratio (OSR) in conjunction with higher order noise shaping make it possible to attain a high conversion resolution.

The $\Delta\Sigma$ modulator is connected to one plate of the microphone M with the single-ended input of the first integrator. As one plate of the microphone is structurally connected to ground, there is no possibility to connect it to the microphone differentially. However, for good performance at low supply voltages, the rest of the modulator is designed with differential circuitry. Single-ended-to-differential conversion takes place at the level of the first integrator.

The first integrator is a continuous-time (CT) circuit with a high input impedance. While all switched-capacitor (SC) circuits need a driver in front of the integrator to load the sampling capacitors which perform the voltage-to-charge conversion [6], CT integrators can be designed with a high input impedance [5]. Their additional advantage is a lower noise bandwidth than an SC counterpart. The higher order integrators, free from special constraints, are designed as SC integrators which perform well when biased at a low supply voltage. The quantizer inside the $\Delta\Sigma$ loop is a differential comparator (1-bit quantizer).

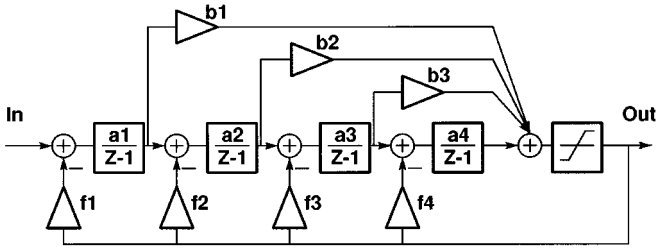

Fig. 4. Modulator topology.

The on-chip bandgap reference supplies a voltage which is converted to a differential current by the VIC circuit. This approach does not load the bandgap reference dynamically, therefore allowing for lower power consumption in the voltage reference buffer. The buffer only has to drive the scaled-down capacitors of the higher order integrators.

All the clock phases required by the SC circuits are derived on-chip from a master clock line supplied externally.

III. $\Delta\Sigma$ ADC Design

A. ADC Requirements

The $\Delta\Sigma$ modulator connected to the microphone requires a high impedance input to isolate the electret material from the rest of the circuit. This single-ended input connects capacitively to the V_{EM} signal source (Fig. 1). The voltage generated by the microphone has a peak amplitude of 125 mV when the device is loaded by a 2-pF capacitor and a large value resistor (around 100 MΩ). The signal has no dc offset, therefore the input of the $\Delta\Sigma$ modulator requires a voltage input range which extends below ground. Because of the small input amplitude, a conversion gain has to be designed in the converter so full-scale codes are reached with a large reference voltage. A low ripple of the conversion gain inside the signal bandwidth is preferred.

The required dynamic range of 84 dB exceeds the dynamic range achievable by the JFET-based solution. The converted signal bandwidth is 11 kHz, so the microphone can be used for both telephony and multimedia applications.

B. $\Delta\Sigma$ Modulator Topology

The architecture of the $\Delta\Sigma$ modulator is shown in Fig. 4. This architecture allows for good control of the noise transfer function (NTF) *and* of the signal transfer function (STF) by using both the feedback coefficients $f_1 \cdots f_4$ and the feedforward coefficients $b_1 \cdots b_3$. No feedforward coefficient is connected at the input of the converter, leaving only the first integrator to load the electret microphone.

The first three integrator gains $a_1 \cdots a_3$ can be chosen arbitrarily and all the other coefficients are then calculated to map the z-domain transfer functions NTF(z) and STF(z) to the physical structure. The coefficients are designed to bound the integrator outputs within 10% to 80% of the supply voltage when the modulator is not overloaded. Integrator clipping to supply rails is used to limit oscillations when the input is larger than

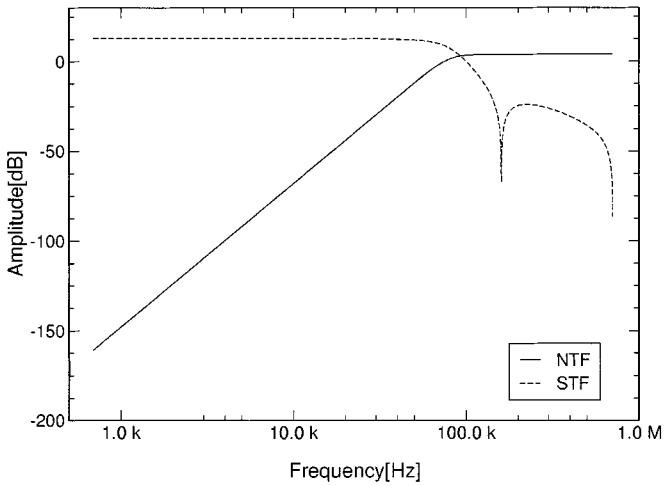

Fig. 5. Magnitude characteristics of STF and NTF.

the overloading level. A value of f_1 lower than unity sets the desired in-band conversion gain.

The modulator is designed to oversample the 11-kHz signal bandwidth at 64 times, with a clock frequency of 1.408 MHz. Under these conditions, the fourth-order single-bit ΔΣ attains a total in-band quantization noise power of −92 dB. As a result, the white noise having a projected in-band power of −84 dB will dominate the quantization noise and function as dither to prevent the idle tones at −115 dB to become audible. The reference voltage considered for all behavioral modeling is 1.5 V. The supply voltage is 1.8 V and all circuits and signals are considered fully differential.

The advantage of a high-complexity architecture is illustrated in Fig. 5. As opposed to simpler architectures [7], complete control of in-band STF magnitude ripple is achieved. The designed flatness of the STF magnitude is better than 0.1 dB from dc to 11 kHz. The pair of zeros in the STF characteristic also provides for high-frequency roll-off, which increases rejection of out-of-band input signals. This compensates for the complete absence of input-signal conditioning. The in-band STF gain is 12 dB, which translates the peak input signal of 125 mV (−21 dBR) to the output overloading level of the modulator of −9 dBR.

C. High Input Impedance Integrator

Conventional SC integrators [6] and CT integrators [8] do not need a high input impedance because, in most applications, a signal buffer or amplifier is already available in front of the ΔΣ modulator. To connect the modulator directly to the microphone, the custom integrator shown in Figs. 6 and 7 was designed.

The single-ended microphone signal Vin (Fig. 6) is connected to the gate of the pMOS transistor $M1$. The use of pMOS devices provides the required input range, which extends more than 200 mV below ground. The transistor pair $M1$, $M2$ repeats the voltage Vin onto the resistors Rs. The resulting current is integrated by the operational amplifier on the feedback capacitors Ci. The two-stage class-A output amplifier keeps its differential input voltage close to zero by balancing the drain currents of $M1$ and $M2$. In the single-ended-to-differential conversion which takes place, balancing of the circuit greatly reduces common-mode cross talk (CMCR) and nonlinear distortion.

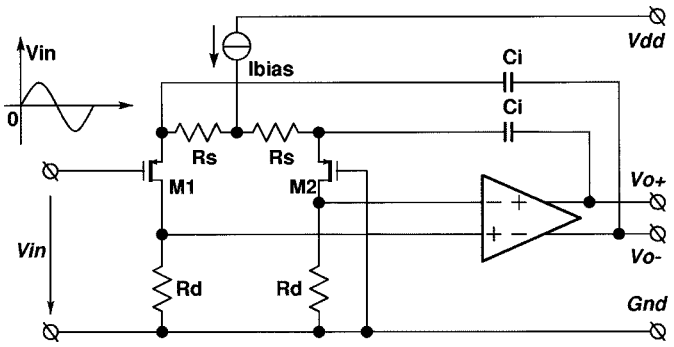

Fig. 6. Microphone signal integration by a single-ended input CT integrator.

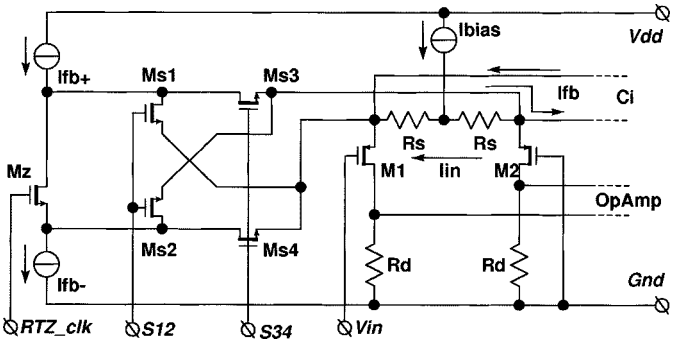

Fig. 7. One-bit ΔΣ feedback integration by a single-ended input CT integrator.

To keep the circuit balanced when the 1-bit decision is fed back from the loop quantizer, a differential feedback current is used as shown in Fig. 7. The two current sources, $Ifb+$ and $Ifb-$, are connected to the sources of the two MOS transistors according to the quantizer decision. The switches $Ms1 \cdots Ms4$ are activated by the digital signals $S12$ and $S34$, directing the differential feedback current Ifb to flow from the source of $M1$ to the source of $M2$ or vice versa. The feedback current is integrated by the operational amplifier on the two capacitors Ci in the same manner as the signal current. The functioning of the return-to-zero clock RTZ_clk will be explained in a following section. All three clocking signals are boosted by local charge-pump voltage doublers to 3.4 V.

With the signal Vin at the input and the ΔΣ feedback applied, the output of the integrator at an arbitrary clock index n is

$$V_{\text{out}}(n) = V_{\text{out}}(n-1) + \frac{V_{\text{in}}}{Rs}\frac{T_{\text{clk}}}{Ci} - Q(n-1)\frac{I_{fb}T_{\text{clk}}}{Ci} \quad (1)$$

with T_{clk} being the clock period and $Q(n-1)$ representing the previous comparator decision with values of $+1$ or -1. In the equation above, Ifb is considered to be integrated during the full clock period. The input signal can be approximated with a dc voltage due to high oversampling.

Switching current feedback has one main advantage for low-power applications: there is no need for a high-speed low-noise buffer for the reference voltage. This is because the only required current sources are static loads for the voltage reference. Fig. 8 shows the schematic of the voltage-to-cur-

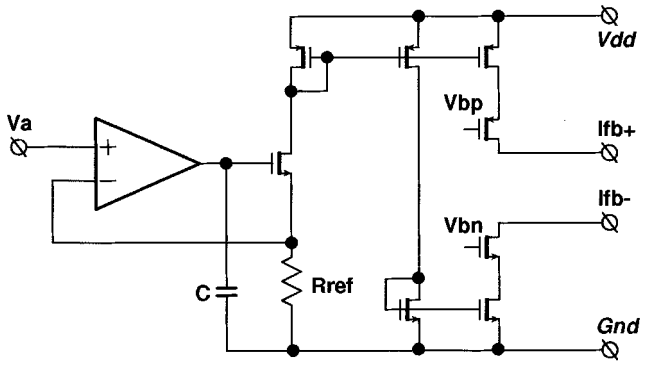

Fig. 8. V/I converter used to generate the feedback current for the first integrator.

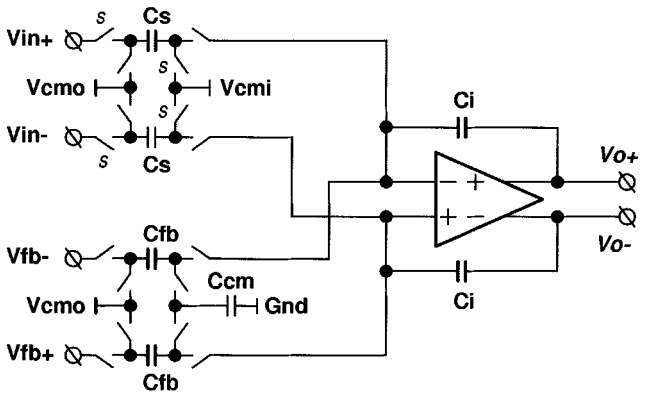

Fig. 9. Switched-capacitor noninverting integrator with $\Delta\Sigma$ feedback path.

rent converter used to derive the feedback currents from the reference voltage Va. The operational amplifier repeats the voltage Va on the resistor $Rref$, sustaining the resulting current through the nMOS transistor connected in the loop. The noise bandwidth of the V/I converter is reduced by the capacitive load of the one-stage amplifier. Variation of $Rref$ over temperature does not degrade the $\Delta\Sigma$ performance as long as $Rref$ is matched with the resistors Rs (Fig. 6). The matching ensures a constant signal/feedback gain ratio.

The feedback current sources are cascoded to increase their output impedance, so the supplied current is not dependent on the microphone voltage signal when an Ifb source is connected to the source of $M1$ (Fig. 7).

The main noise contributors are the drain resistors Rd, whose value is limited by the upper margin of the operational amplifier input range, and by the lower margin of the drain-to-source voltage needed to operate the MOS transistors away from the linear region. The other noise sources are the Rs resistors, whose values can only be decreased at the expense of increasing the size of the Ci capacitors, and the MOS transistors $M1$ and $M2$, which are operated at drain currents of 7.5 μA to allow the use of larger- value Rd resistors. Approximately 90% of the noise power is generated by the mentioned devices.

D. Switched-Capacitor Integrators

The higher order integrators are fully differential SC circuits, following the topology shown in Fig. 9. They consist of a signal integration path built with the sampling capacitors Cs and a $\Delta\Sigma$ feedback integration path, represented by Cfb capacitors. All integrators deliver their outputs to the adder in front of the quantizer to implement the $b_1 \cdots b_3$ coefficients (Fig. 4).

The SC integrators are better suited for low-voltage operation than CT circuits. One advantage is the decoupling of the input signal common-mode and operational amplifier common-mode input. As shown in Fig. 9, during the sampling phase, the switches marked s are closed and the input signal common-mode voltage is $Vcmi$. During the opposite clock phase, when the switches marked s are open and the other four switches are closed, the common-mode voltage $Vcmo$ is used to correctly bias the input stage of the operational amplifier. The $Vcmi$ and $Vcmo$ voltages are independently set, so $Vcmi$ is tied to the middle of the supply voltage to take advantage of the rail-to-rail output capability of the previous integrator, while $Vcmo$ has a low value falling inside the common-mode input range of the pMOS-input amplifier.

Another advantage of SC circuits is the good control of ratios of capacitors. For a CT circuit, a path gain is dependent on the RC or g_mC product, which has a typical 3-σ spread of 30%. In the case of SC circuits, however, the gain is given by an Cs/Ci ratio with a spread of less than 1%. In a $\Delta\Sigma$ modulator, the better control of each path gain means that the output range of the integrators in nonoverloaded condition can be extended closer to the supply rails without decreasing the yield. The larger the output range, the smaller the capacitive load of the operational amplifier, hence the lower the power consumption.

The MOS capacitor Ccm is charged to the common-mode value of the differential feedback voltage $Vfb+ - Vfb-$, eliminating the need for an additional buffer circuit.

All the nonoverlapping clock phases are generated on-chip. The switching signals for all the SC circuits are boosted by a single set of charge-pump voltage doublers. The second integrator contains a two-stage rail-to-rail output amplifier which attains higher output range compared to the folded-cascode amplifiers used inside the third and fourth integrators.

E. Adder and Comparator

The adder in front of the quantizer (Fig. 4) is designed as an SC integrator (Fig. 9) which resets its Ci integrating capacitors on each *sampling* clock phase. It samples the outputs of the integrators on each *integrating* phase to deliver the non-delayed sum to the quantizer.

The quantizer is a differential-input dynamic comparator which preloads on each integrating phase, making a decision at the beginning of the sampling phase. The decision is latched at the end of the sampling phase by a digital RS latch to maintain a constant output until the next decision is made.

F. Feedback Timing

The use of both CT and SC integrators in the same $\Delta\Sigma$ modulator requires two different types of $\Delta\Sigma$ feedback to be supplied. As shown in Fig. 10 and explained in the previous sections, the CT first integrator has a differential reference current $Iref$ which is supplied by the V/I converter (Fig. 8) and is switched according to the $S12$ and $S34$ digital signals. The feedback for the SC integrators is supplied as a differential voltage V_{fb}.

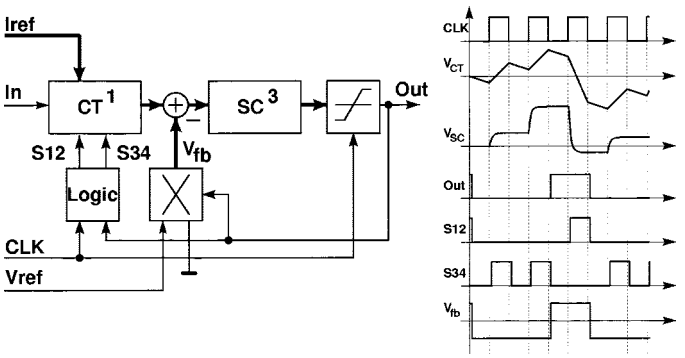

Fig. 10. Timing of ΔΣ feedback signals.

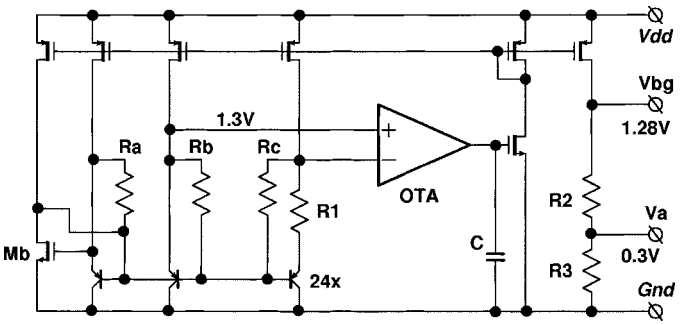

Fig. 11. Low-voltage bandgap reference.

Considering the master clock to be divided into sampling ($CLK = 0$) and integrating ($CLK = 1$) phases, the comparator makes its decision at the end of the integrating phase, as shown in Fig. 10, waveform *Out*. The decision is used to generate the feedback signals $S12$, $S34$, and V_{fb}. For the $S12$ and $S34$ digital signals, the sampling phase is used as return-to-zero control to reduce intersymbol interference at the level of the first integrator [5]. As shown by the waveform V_{CT}, the current feedback is only integrated during the integrating phase. During the sampling phase, only the input signal is integrated while both $S12$ and $S34$ are off and RTZ_clk (Fig. 7) is switched on to connect the $Ifb+$ and $Ifb-$ sources, thus keeping them out of saturation.

The SC integrators do not require a certain shape of feedback pulse, so their feedback is supplied during the sampling phase, as shown by the V_{fb} waveform. The waveform labeled V_{SC} in Fig. 10 is the output of the second integrator and is supplied for easier identification of sampling and integrating phases.

IV. Low–Voltage Bandgap Reference

A low-voltage low-power bandgap reference generator is integrated on-chip. The circuit in Fig. 11 generates two voltages of bandgap quality, Vbg of 1.28 V, which is buffered and used to supply the feedback for the SC integrators (a total capacitive load of 2 pF, in-band noise power of −60 dB), and Va of 0.3 V, which is used to bias the V/I converter to generate feedback currents for the CT integrator (Fig. 8). The low voltage value is needed to correctly bias the pMOS input stage of the operational amplifier used in the V/I converter.

Because a base–emitter voltage is larger than the common-mode input range of a pMOS differential pair, an nMOS input stage is used in the OTA and is biased by lifting the base-collector voltage of the substrate PNPs so their emitter voltage is equal to the V_{gs} of Mb.

The OTA is loaded with a MOS capacitor C to decrease its noise bandwidth. All resistors used are n-well resistors with large values, so a low current consumption is achieved. This does not affect the bandgap performance, as the output voltages only depend on the ratio of resistors [9].

V. Linearity Analysis

High linearity can be achieved in single-bit ΔΣ modulators due to the inherent linearity of the 1-bit DAC [10]. The linearity limit in such modulators is the linearity of the integrators, and especially of the first integrator for high OSR values.

The high input impedance integrator used in this design makes use of a capacitive feedback connection to the sources of the MOS transistors $M1$, $M2$ (Fig. 6) which causes all the signal current to flow directly into the capacitors without passing through the input transistors. This improves the linearity compared to that of an open-loop MOS pair [5] as it keeps the input stage balanced. With a differential input signal in the order of 100 mV, the integration linearity can reach 100 dB (better than 16 bit) without requiring high current levels (large transconductance) for the input transistors.

With this topology, the linearity performance is limited by the single-ended-to-differential conversion. Imbalance of the input stage allows the common-mode component of the input signal to be converted to a differential output. The resulting common-mode to differential cross talk is

$$\frac{1}{H} = \frac{\Delta\mu}{\mu}\,\frac{2R_s g_{ds}}{1+g_m R_s} \tag{2}$$

where $\Delta\mu/\mu$ is the relative imbalance of the voltage gain for the MOS transistors

$$\mu = \frac{g_m}{g_{ds}}. \tag{3}$$

These equations assume that the integrator is placed in a feedback loop which helps to keep the output voltage stable. This is a good approximation of a high-oversampling ΔΣ feedback.

Two mechanisms put the circuit out of balance. The first one is caused by the finite operational amplifier gain, which produces a difference in the drain currents of $M1$, $M2$

$$\Delta I_D = \frac{V_{O+} - V_{O-}}{A_{DC} R_d}. \tag{4}$$

The second one is caused by the low voltage gain of the MOS input transistors. Due to their finite output impedance, the imbalance in their drain-source voltages

$$\begin{aligned} V_{DS1} &= V_{in} + V_{SG1} - R_d I_{D1} \\ V_{DS2} &= V_{SG2} - R_d I_{D2} \end{aligned} \tag{5}$$

induces a difference in the gate-source voltages. The complete drain current equation of a pMOS transistor in strong inversion

$$I_D = \beta(V_{SG} + V_{TH})^2(1+\lambda V_{SD}) \tag{6}$$

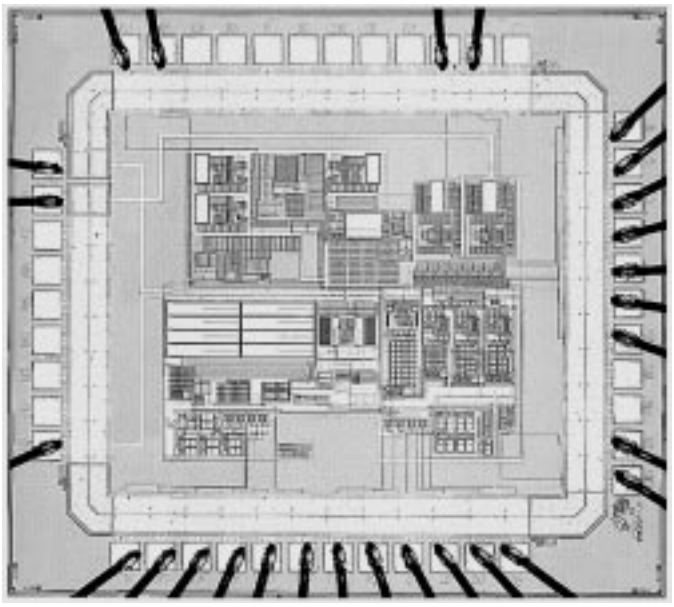

Fig. 12. Chip micrograph.

must be used to calculate the two V_{SG} values numerically considering the values of V_{SD} and the equality of the two drain currents. With all the voltages calculated, the expressions of g_m and g_{ds} can be derived and used to calculate (2). An equivalent distorted input signal can be written

$$V_{\text{in}}^{\text{DIST}} = V_{\text{in}} \left(1 + \frac{1}{2H}\right). \tag{7}$$

The distortion is generated by the proportionality of $1/H$ to the input signal, in a first-order approximation. For high-accuracy simulations, both effects must be taken into account. In this design, the second effect was found to dominate due to the high voltage gain of the amplifier and low output impedance of the MOS transistors. Therefore, the input MOS transistors are operated between moderate and strong inversion to optimize both their voltage gain and source-to-drain voltage. No cascoding of the input transistors is possible because the input range has to extend below ground.

VI. Experimental Results

The chip has been realized in a 0.5-μm CMOS process with a high-linearity capacitor option. A micro-photograph of the layout is shown in Fig. 12. The $\Delta\Sigma$ modulator occupies 0.8 mm^2, most of the area being taken by the first integrator capacitors with a total value of 80 pF. The on-chip bandgap reference takes another 0.4 mm^2. The layout of the bandgap reference has not been optimized for area. Test circuitry is integrated on-chip to allow control of clock lines and observation of integrator outputs. The prototype can be operated in test mode or as a stand-alone acquisition system, in which case only five pins are used. An on-chip 5-nA current source is used to dc-bias the input.

All measurements reported here have been taken with the chip biased at 1.8 V and clocked at 1.404 MHz. A single-ended signal generator with 18-bit linearity and noise performance has been attached to the input of the $\Delta\Sigma$ modulator. The small-amplitude single-ended signal requires special care concerning the shielding of signal cables and PCB traces.

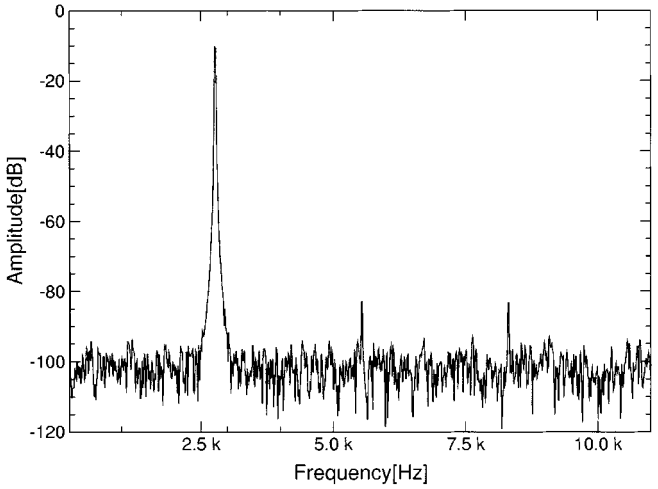

Fig. 13. Measured FFT of output bit stream with an input signal of -24 dBR (rms).

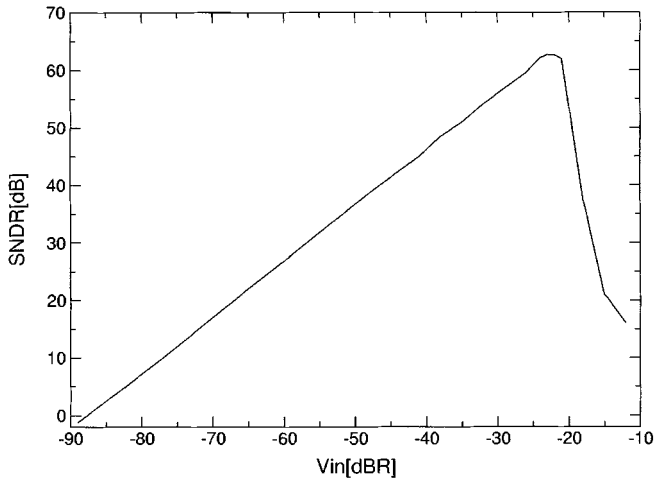

Fig. 14. Measured SNDR versus input signal level for a chip using internal clocks and references.

Fig. 13 shows the measured output spectrum when a 2.75-kHz, zero dc offset sinusoid is applied at the input. The amplitude of the input signal is 125 mV (-24 dBR rms with respect to the design reference of 1.5 V). The spectrum has a frequency resolution (FFT bin) of 14 Hz. With the -21 dBR input amplitude, a -10 dBR output is reached. The second harmonic distortion is 73 dB below the main spectral component, as the theoretical model predicted. The third harmonic distortion is generated by nonlinearity of the first integrator's operational amplifier gain, which in turn is caused by its large output voltage swing.

The variation of signal-to-(noise+distortion) (SNDR) with input signal amplitude has been measured. The curve is shown in Fig. 14 for an input signal ranging from -90 dBR up to -12 dBR. Due to the conversion gain, the upper limit translates as a 0-dB output signal, which is used to test the loop overloading condition. SNDR shows good linearity up to an input signal amplitude of -23 dBR rms (overloading level). There is

TABLE I
PERFORMANCE SUMMARY

Supply Voltage	1.8V
$\Delta\Sigma$ Supply Current	600μA
Reference Supply Current	350μA
Total Power Consumption	1.7mW
Signal Bandwidth	11kHz
OSR	64
Maximum Input Signal	125mV peak
Dynamic Range	80dB
Peak SNDR	62dB
Technology	0.5 μm CMOS 2P2M
Total Die Area	1.2 mm^2

a flat region caused by harmonic distortion and, at large input levels, the SNDR sharply drops due to loop overloading. The loop overloads but does not become unstable as the integrator outputs are clipped to supply rails. The peak SNDR value is 62 dB (10 bit) and the measured dynamic range on the 11-kHz signal bandwidth is 80 dB (13 bit). Thermal noise dominates the in-band quantization noise. The measured performance and characteristics have been summarized in Table I.

VII. CONCLUSION

A 1.8-V $\Delta\Sigma$ modulator which can be packaged with an electret microphone has been designed and measured. The modulator contains a high input-impedance CT integrator that is connected directly to the microphone, without using an amplifier for signal conditioning. The other integrators are all SC circuits which offer good performance in low-voltage applications. Switching-current feedback is used for the first integrator to minimize the dynamic load of the on-chip bandgap reference. The peak input signal is 125 mV (-21 dBR). This value is converted to the full-scale output of -9 dBR. The converter shows an in-band STF flatness of 0.1 dB and sharp roll-off at frequencies above 50 kHz so aliasing of input signal is prevented.

The chip consumes 1.7 mW to attain 80-dB dynamic range on a signal bandwidth of 11 kHz. The effective number of bits is 10, limited by nonlinear distortion in the first integrator. All the support circuits, complete with bandgap reference and clock phases generation, are integrated on-chip. The circuit can be placed inside the microphone package, where only four wires are being needed to connect it to a digital chip set: incoming clock, output data, supply, and ground.

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