12.4 A 1.9μW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC

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Future systems powered by energy scavenging, e.g., wireless sensor nodes, demand μW-range ADCs with no static bias currents in order to have a power dissipation proportional to the sample rate. An ADC that meets these requirements by using a charge-redistribution DAC, a dynamic 2-stage comparator, and a delay-line-based controller is realized in CMOS.

Figure 12.4.1 shows a DAC based on charge redistribution, with a binary-weighted capacitor array [1]. The left side of every capacitor can be switched between a low reference voltage, V_{ref-}, and a high reference voltage, V_{ref+}, using a simple digital inverter. If the left side of capacitor C_{MSB} is switched from low to high, the step on output V_{DAC} is $\Delta V_{DAC} = (V_{ref+} - V_{ref-})*C_{MSB}/C_{tot}$, where C_{tot} is the total capacitance at the output node. The effect of the charge-redistribution is reversible: if the left side of C_{MSB} is switched from high to low, the output returns to its original value. This does not contribute any noise to the output voltage as there is no sampling involved. The switch at the output of the DAC can be used to reset the DAC voltage to V_{ref-} to prevent DC drift due to leakage. This reset gives a thermal-noise voltage of kT/C_{tot}.

The matching of metal-plate capacitors in a modern CMOS process is very good. For a 10b converter with a total DAC capacitance C_{tot}=600fF; the matching is better than 0.5 LSB. For this DAC, mismatch is dominant over thermal noise if the output-voltage range is more than ~0.2V. The inverter charging or discharging C_{MSB} of 300fF only sees the equivalent capacitor C_{eq} of 150fF. If $V_{ref+} - V_{ref-}$ is 1V it takes only 150 fJ to switch C_{eq} from V_{ref-} to V_{ref+} and back to V_{ref-}. Thus, the theoretical energy per conversion in the DAC can be less than a few hundred fJ. This energy can even be lower if the charging and discharging of C_{eq} is done in multiple steps. This is shown in Fig. 12.4.2 where the voltage over C_{eq} is charged from 0 to V in 3 steps of V/3. The dissipated energy is $1/6C_{eq}V^2$. which is 3× less than the $½C_{eq}V^2$ of a one-step charge. In theory, charging with n equidistant voltage steps always decreases the power by a factor of n. In practice control overhead is added and there is only a net saving for "small" values of n with "large" values of C_{eq}. Switches are implemented as small NMOS or PMOS devices driven by logic. The intermediate voltage levels come from big capacitors C_{BIG1} and C_{BIG2} and automatically converge to appropriate values due to repetitive DAC operation. This implementation is allowed, because the accuracy of the intermediate steps does not affect the accuracy of the DAC. Only intermediate levels are used for the 3 MSBs, while the supply voltage is used directly for all other reference voltages.

The charge-redistribution DAC can be used in a simple way to make a SAR ADC, as shown in Fig. 12.4.3. First, the DAC is reset to a state where the MSB is high and all other bits are low. Next, V_{in} is sampled onto output V_{DAC}. In a single-ended ADC, V_{DAC} is compared to V_{half}. In this differential implementation, the two halves are compared to each other. The comparator decides if the MSB should remain high or set low during the remainder of the conversion. Next, MSB-1 is set to high and the procedure is repeated, until N comparisons have been done for N bits. The DAC setting is now a digital representation of the analog input voltage.

In this ADC, V_{in} is sampled through one switch onto the DAC output. In [1], a similar ADC principle is used, but with a more complicated sampling scheme: during the sampling phase the DAC output is connected to a reference voltage while V_{in} is connected through N switches to the other sides of the N capacitors of the DAC. Therefore, it is necessary to set the MSB in between the sampling phase and the first comparison. In the ADC discussed here, this has already been done, saving energy and time.

The 10b differential ADC uses bootstrapped NMOS devices to sample the differential input voltage onto 2 identical charge-redistribution DACs. These 2 DACs are the inputs of the comparator. An advantage of differential operation is that the reference voltage V_{ref} only needs to be accurate during the sample phase. During the actual conversion, supply noise that is common mode to both DACs hardly influences the ADC accuracy. For some further energy reduction the DACs are not completely binary weighted, but use a split capacitor bank [2].

Requirements on the comparator are: no DC quiescent current and a low input equivalent noise. Figure 12.4.4 shows the comparator that is inspired from a dynamic comparator optimized for high speed [3]. Nodes FN and FP are precharged "high" while SN and SP are precharged "low". A rising clock edge stops the precharging state and soon biases MN_{tail} in triode. For maximum voltage gain, this transistor is dimensioned such that the first differential pair operates in subthreshold. The signal and noise are integrated on FN and FP, resulting in an SNR that increases while the common-mode voltage decreases. When the common-mode voltage on FN and FP reaches a threshold below V_{DD}, the input transistors in the second stage turn on and the signal is amplified onto SN and SP. When SN and SP reach a certain common mode, the second stage starts to regenerate. The overall voltage gain prior to regeneration is high, because of the double-gain stage and the dominant subthreshold operation. As a result, the relative noise contribution of the regeneration stage is less than in a single-stage comparator.

The T/H signal is derived from an external sample clock. An internal delay-line is used to generate all further control signals of the SAR algorithm. The delay-line is implemented with inverters with alternately a large length of the NMOST and PMOST. After the conversion, a ready signal is generated and the power consumption stops. According to simulation the delay-line and control signals use about 44% of the power, the comparator about 31%, the DAC, the register and the on-chip digital output about 21%, and the T/H switches about 4%.

A testchip is fabricated in a 65nm CMOS process. Measurement results are shown in Figures 12.4.5 and 12.4.6. The power consumption of 1.9μW at 1MS/s and 1V supply closely matches simulation results. The best SNDR is measured with an input amplitude slightly over half the input range. Increasing the amplitude improves the SNR to 59dB, but the THD also increases resulting in a decreased SNDR. This increase in THD is caused by the (underestimated) non-linear parasitic capacitor that is part of C_{tot}. This results in a DNL of 0.5LSB and an INL of 2.2LSB. With a supply voltage of 1.3V and a 20% duty cycle of the sample clock, the maximum sample frequency is 4.9MS/s with an accuracy of about 8 ENOB. Using the FOM definition in [4], a FOM of 4.4fJ/conversion-step is measured, which is 15× better than the 65fJ/conversion-step of [4].

Acknowledgements:
The authors thank NXP Research for chip fabrication and valuable assistance with chip finishing and measurements.

References:
[1] J. McCreary and P. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques," *IEEE J. Solid-State Circuits*, vol. 10, no. 6, pp. 371-379, Dec. 1975.
[2] B. Ginsburg and A. Chandrakasan, "An Energy-Efficient Charge Recycling Approach for a SAR Converter with Capacitive DAC," *Proc. IEEE ISCAS*, vol. 1, pp. 184–187, May 2005.
[3] D. Schinkel, E. Mensink, E. Klumperink, et al., "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *ISSCC Dig. Tech. Papers*, pp. 314-315, Feb. 2007.
[4] J. Craninckx and G. van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 246-247, Feb. 2007.

 978-1-4244-2010-0/08/$25.00

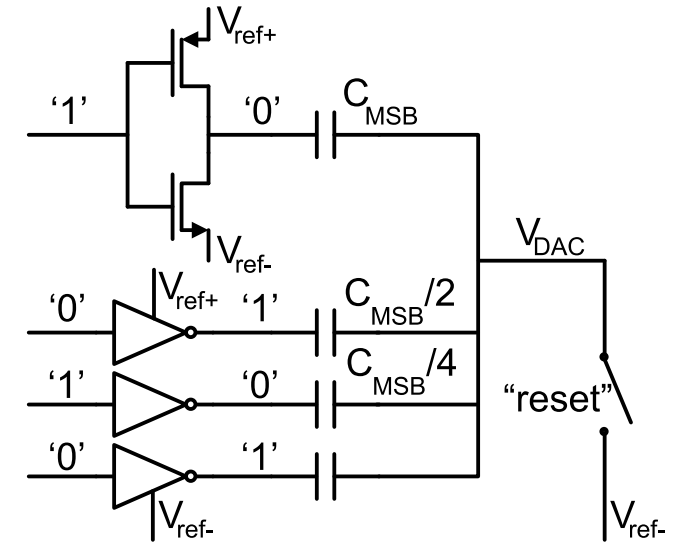


Figure 12.4.1: Charge-redistribution DAC.

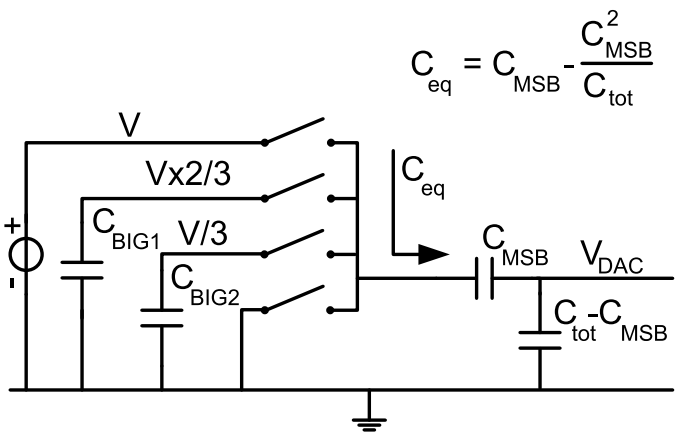


Figure 12.4.2: Efficiency improvement for charge-redistribution DAC.

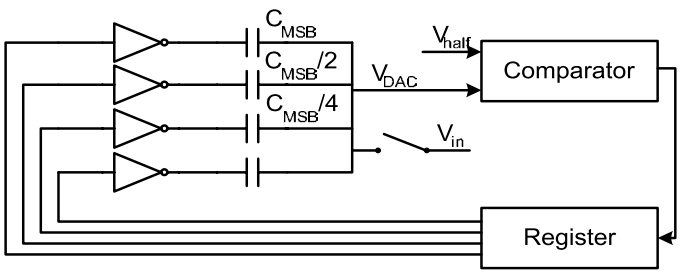


Figure 12.4.3: Single-ended SAR ADC based on charge-redistribution DAC.

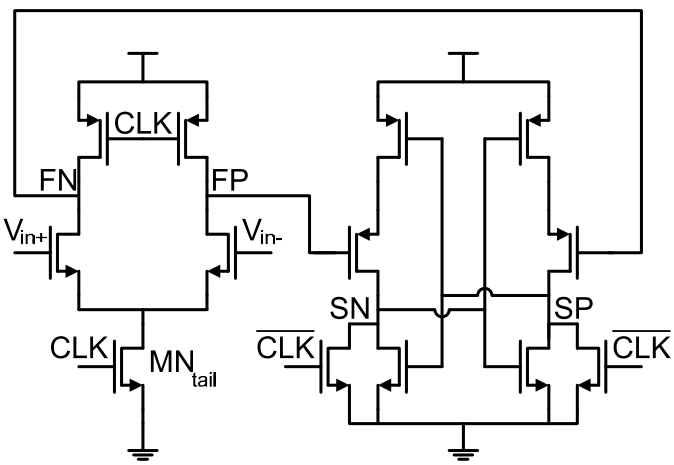


Figure 12.4.4: Energy efficient two-stage comparator.

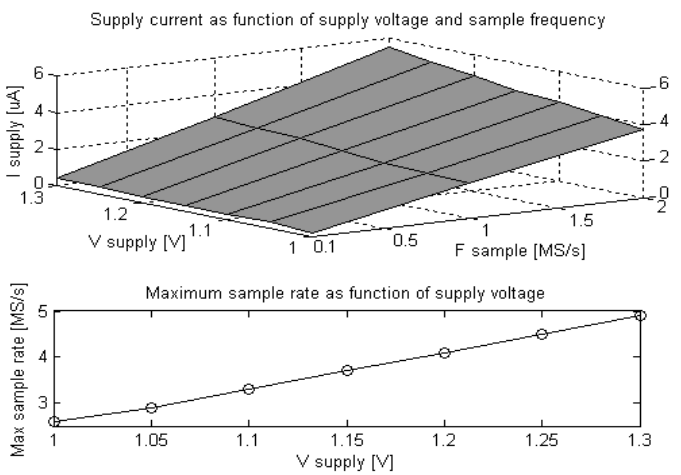
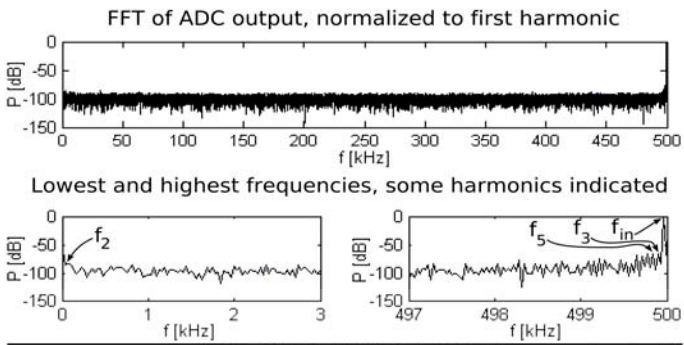


Figure 12.4.5: Measured relations between supply voltage, samplerate and supply current.



	SNR [dB]	THD[dB]	FOM [fJ/conversion-step]
Average (over 12)	55.6	-61.1	4.42
Standard deviation	0.58	1.95	0.24

Figure 12.4.6: Measurement results: f_{in}= 499968.75Hz, f_{sample}=1MS/s, V_{supply}=1V

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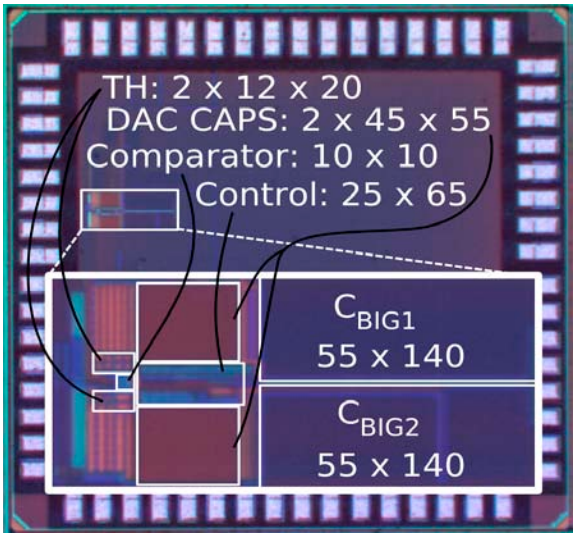

Figure 12.4.7: Die micrograph of the 65nm CMOS testchip, dimensions in μm².

 978-1-4244-2010-0/08/$25.00