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A 1 GS/s, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT-ΔΣ ADC with 1.5 Cycle Quantizer Delay and Improved STF

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Abstract A 1 GS/s Continuous-time Delta-Sigma modulator (CT-$\Delta\Sigma$M) with 31 MHz bandwidth, 76.3 dB dynamic range and 72.5 dB peak-SNDR is reported in a 0.13 μm CMOS technology. The design employs an excess loop delay (ELD) of more than one clock cycle for achieving higher sampling rate. The ELD is compensated using a fast-loop formed around the last integrator by using a sample-and-hold. Further, the effect of this ELD compensation scheme on the signal transfer function (STF) of a feedforward CT-$\Delta\Sigma$ architecture has been analyzed and reported. In this work, an improved STF is achieved by using a combination of feed-forward, feedback and feed-in paths and power consumption is reduced by eliminating the adder opamp. This CT-$\Delta\Sigma$M has a conversion bandwidth of 31 MHz and consumes 34 mW from the 1.2V power supply. The relevant design trade-offs have been investigated and presented along with simulation results.

Keywords Analog-digital (A/D) conversion · continuous-time (CT) · delta-sigma ($\triangle\Sigma$) · excess loop delay (ELD) · feedforward · signal transfer function (STF)

1 Introduction

Rapid evolution of wireless broadband communication systems has necessitated development of power-efficient analog-to-digital data converters (ADCs) with ever increasing conversion bandwidth (BW). Continuous-time delta-sigma (CT-$\Delta\Sigma$) ADCs have recently been explored for wideband data conversion while providing sufficiently high dynamic range (DR) for wireless applications and unique features that greatly reduce the challenges of deploying such ADCs in high-speed, high-performance systems. CT-$\Delta\Sigma$ ADCs are particularly of interest in broadband wireless communication systems due to their following unique features:

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- An inherently power-efficient continuous-time $\Delta\Sigma$ ADC architecture eliminates the power hungry gain-stages which are predominantly required for input-sampled ADCs such as the pipeline ADC. Besides, CT-$\Delta\Sigma$ ADCs are tolerant of the non-linearities associated with the input-sampling process as the sampling takes place inside the feedback loop and the associated errors are noise-shaped [1,2].
- The CT loop-filter in the $\triangle\Sigma$ feedback loop provides inherent alias filtering before sampling occurs in the quantizer. This greatly relaxes the requirement of an additional anti-alias filter (AAF) resulting in higher on-chip integration and overall saving in power consumption [1,2].
- Continuous-time $\triangle\Sigma$ operation results in relaxed unity-gain bandwidth requirements for the integrator stages in comparison with the traditional discrete-time (DT) $\Delta\Sigma$ ADCs. This results in significant power savings compared to the DT-$\Delta\Sigma$ ADCs for the same sampling-rate, and enables much higher sampling rates in a given technology when compared to the latter.
- A purely resistive input impedance offered by the CT-$\Delta\Sigma$ alleviates the requirement of a buffer usually employed to drive an input-sampled ADCs. Further, a CT loop-filter leads to reduced switching in the ADC resulting in quieter supply and ground rails[1,2].

The confluence of above desired features and relaxed opamp gain-bandwidth and nonlinearity requirements, CT-$\Delta\Sigma$ ADCs have been successfully implemented in smaller CMOS technologies (65 nm and 45 nm) resulting in GHz sampling rates [3, 4,5,6]. The CT-$\Delta\Sigma$ loop-filter lends to easier implementation at low supply voltages and thus CT-$\Delta\Sigma$ ADCs can easily be ported into scaled CMOS technologies while leveraging the speed and power improvements in the digital decimation stages.

Modern wireless network standards require ADCs with conversion bandwidth up to 160 MHz and resolution of 10-14 bits. Rapid development of these systems can be sustained by leveraging the higher conversion bandwidth and dynamic range from CT-$\Delta\Sigma$ ADCs while maintaining power efficiency. To achieve a wider conversion bandwidth, the designers are limited by the lower oversampling ratio (OSR) for the maximum achievable clock rate in a given process technology. Moreover, trading the OSR for higher BW restricts the highest achievable dynamic range. In order to compensate for the signal-to-quantization noise (SQNR) degradation due to lower OSR, higher resolution, i.e. multi-bit quantizers are often used [1,2]. Several CT-$\triangle\Sigma$ modulators achieving 10-12 bits resolution with a signal bandwidth ranging from 5-20 MHz have been recently reported [3,6,7,8,9].

There are several advantages of using a multi-bit quantizer, which include a lower quantization noise floor and higher dynamic range, and relaxed slew-rate requirements in the loop-filter opamps. A lower LSB size allows a higher out-of-band gain (OBG) which allows aggressive noise shaping with higher maximum stable amplitude (MSA) . On the other hand, increasing the resolution above 4-bits results in an exponential increase in circuit complexity, as increase in 1-bit in the quantizer requires a doubling of the number of comparators. Also, in a given technology, the maximum achievable sampling frequency, $f_{s,max}$ is primarily constrained by the tolerable excess loop delay (ELD) in the CT-$\triangle\Sigma$ loop. ELD is largely contributed by the finite regeneration time of the comparator latches in the quantizer and the delay from the DAC mismatch shaping logic in the feedback DAC, while the excess delay from the opamps also contributes to the ELD [10,11]. Figure 1 shows the general block diagram of the traditional single-loop CT-$\triangle\Sigma$ modulator. In this figure, $L(s)$ is

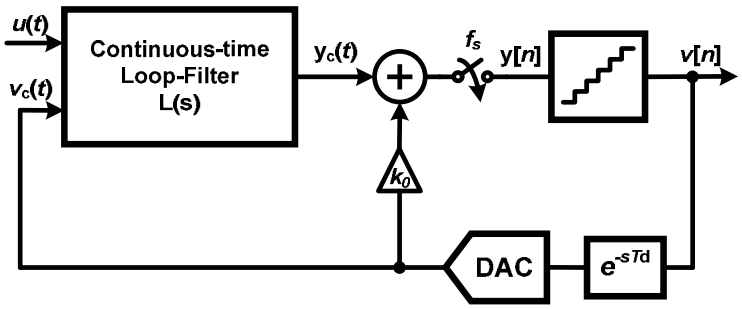

Fig. 1 General block diagram of a CT-$\triangle\Sigma$ modulator.

the continuous-time loop filter, implemented either using cascaded integrators with distributed feedforward or feedback summation architecture, whose output is sampled and quantized at frequency, f_s, or equivalent time period T_s. k_0 is the gain of the direct path introduced to compensate for an ELD of less than one clock cycle.

To design a power-efficient CT-$\triangle\Sigma$ ADC, the feedforward architecture is preferred, as it results in power savings in the loop-filter and requires only a single feedback DAC. In a feedforward loop-filter, after dynamic range scaling is performed, the unity-gain bandwidth (ω_{un}) requirements of the integrators are progressively reduced from the input stage to the last integrator stage [1]. Since the first integrator stage already necessitates a power hungry opamp from noise and linearity considerations, the latter opamps can be designed with progressively lower unity-gain bandwidths. This results in overall power savings in the loop-filter when compared to the feedback architecture. However, feedforward modulators exhibit out-of-band peaking in the signal transfer function (STF) magnitude response. This is one of main drawback in using them in wireless application where any strong out-of-band blocker can get amplified by the peaking of the STF and thus reducing the dynamic range of the ADC or risking instability by saturating the quantizer. Few feedforward CT-$\triangle\Sigma$ modulators have been reported in past with a low-pass STF, without any out of band peaking at the cost of increased circuit complexity [12,13].

In our earlier work, in order to achieve a higher conversion bandwidth (BW), a quantizer with an excess loop delay (ELD) of one-and-a-half clock cycles ($1.5\,T_s$) was used, which enabled higher sampling rate ($f_s = 1\,GHz$) for a fixed oversampling ratio ($OSR = \frac{f_s}{2 \cdot BW}$) [14]. To compensate for the loop instability caused by an ELD of 1.5, a sample-and-hold (S/H) based excess-loop-delay (ELD) compensation presented in [11,15], was employed. Despite of the over two-fold increase in the sampling rate, this architecture suffers from aggravated STF peaking which is undesirable in several wireless applications. Further, the authors have proposed a CT-$\triangle\Sigma$ architecture employing a two-step quantizer to realize higher dynamic range at low OSR (i.e. higher BW) [16]. The proposed technique and design discussion can be directly applied to such hybrid CT $\triangle\Sigma$-pipelined ADC architectures to achieve a low-peaking STF response. In this work, the impact of this ELD compensation on out-of-band peaking in STF of the feedforward CT-$\triangle\Sigma$ modulator is analyzed in detail. Further, a detailed description of the earlier proposed CT-$\triangle\Sigma$ architecture in [14] is provided along with a systematic design method to achieve lower STF peaking. The simulation results validate that the proposed power-efficient architecture results in a reduced out-of-band peaking STF, making it suitable for next-generation broadband

wireless applications such as IEEE 802.11ac which require up to 160 MHz conversion bandwidth [17,18].

The architecture and implementation details of the CT-$\triangle\Sigma$ADC form the discussion of rest of the paper. Section 2 illustrates design of the required CT-$\triangle\Sigma$ noise transfer function (NTF), the impact of ELD greater than one the STF and the systematic design procedure for the proposed ADC. Section 3demonstrates circuit level implementation of the design blocks. Section 4 presents the simulation results of the proposed modulator. Finally, section 5 draws conclusions about the work.

2 System-Level Design of the Modulator

As previously discussed, the quantizer can be clocked over two times higher sampling rate by absorbing the excess loop-delay (ELD) greater than a clock cycle in the feedback$\triangle\Sigma$ loop [11]. Fig. 2 shows the modified CT-$\triangle\Sigma$ modulator block diagram, incorporating an ELD compensation technique of more than one clock cycle [11]. Here, the ELD compensation is achieved by using an additional feedback path around

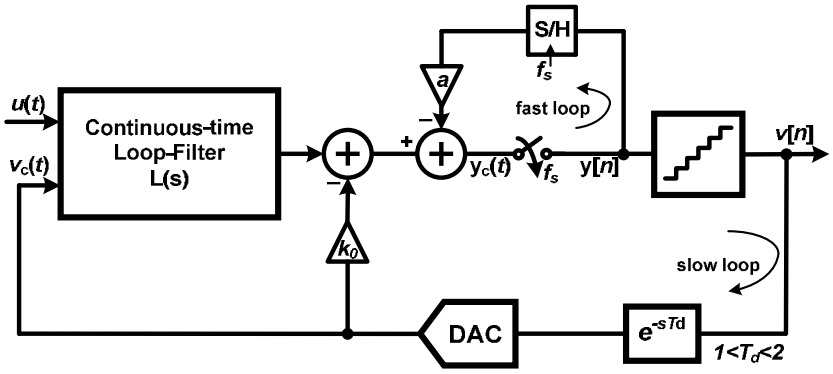

Fig. 2 General block diagram of a CT-$\triangle\Sigma$ modulator with an S/H [11].

the sampler using a sample-and-hold (S/H) with a gain *'a'*. The purpose of this fast-loop is to restore the second sample of the open-loop response, $l[n]$. Due to this additional loop formed by the S/H, an extra zero appears in the resulting noise-transfer function (NTF) of the modulator. Therefore, the resulting noise-transfer function, $NTF_{new}(z)$, is of the form[11]

$$NTF_{new}(z) = (1 + az^{-1}).NTF(z) \tag{1}$$

where $NTF(z)$ is the originally desired NTF without the S/H based short-loop. Even though the ability to tolerate ELD in the range of 1 to 1.5, increases the achievable sampling rate (f_s) by a factor of two, there are few drawbacks with this technique. The resultant larger out-of-band gain (OBG) of the NTF_{new}, with increased in-band noise floor, results in larger 'wiggling' of the quantizer output sequence, $v[n]$. As a consequence, the signal variation at the input of the quantizer ($y_c(t)$) is increased by large extent and thus overloading the quantizer more often, which significantly reduces the maximum stable amplitude (MSA), and degrades the achievable dynamic

range of the modulator. Fig. 2 shows the comparison between the resultant OBG (OBG_{new}) with $1 < ELD < 2$ with the desired OBG (OBG_{orig}). Here, the increased OBG due to the additional zero in $NTF_{new}(z)$ degrades the SQNR performance of CT-$\triangle\Sigma$ by an order of the modulator. Therefore, in order to compensate it, an extra order in the loop filer is required to achieve the same SQNR and DR performance in a modulator, where the ELD is compensated for less than one clock cycle. In this work, a maximum NTF OBG of approximately $OBG_{orig} = 7\,dB$ is selected such that the resulting equivalent $OBG_{new} = 12\,dB$ can be tolerated. Since a multi-bit quantizer is employed in the design, the resulting overload due to OBG_{new} slightly reduces the MSA and dynamic range.

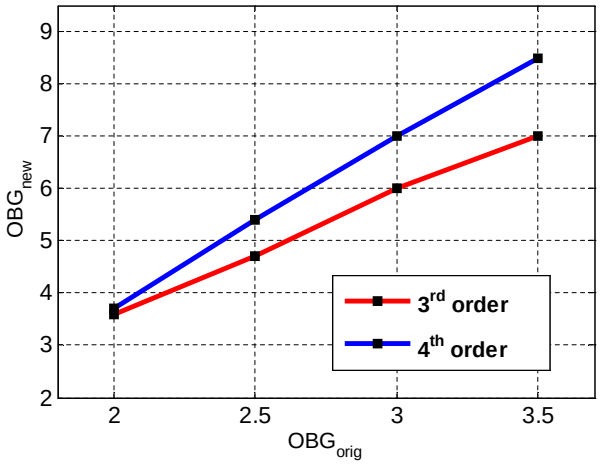

Fig. 3 Plot showing the increased out-of-band gain (OBG_{new}), compared to the original OBG_{orig} with $ELD = 1.5$ technique for $3^{rd}-$ and 4^{th}-order CT-$\triangle\Sigma$ modulators.

2.1 STF Response of CT-$\triangle\Sigma$M Compensated for $ELD > 1$

In a CT-$\Delta\Sigma$M, the input signal is pre-filtered by the loop filter before its sampled by the quantizer. Thus, the modulator provides an inherent anti-alias filtering [1]. However, in the case of ELD compensation greater than one clock cycle, we have another loop around the sampler. Fig. 4 illustrates the equivalent linear model used to derive the signal transfer function, $STF(j\omega)$, of the CT-$\Delta\Sigma$M compensated for $ELD > 1$. The resulting STF is given by the expression[14]

$$STF_{new}(j\omega) = FF_{new}(j\omega).\frac{1}{1 + az^{-1} + k_0 z^{-2} + L_1(z)}|_{z=e^{j\omega T_s}} = FF_{new}(j\omega) \cdot NTF(e^{j\omega T_s}) \tag{2}$$

where $FF_{new}(j\omega)$ is the pre-filter transfer function, and $L_1(z)$ is the open-loop response of the CT-$\triangle\Sigma$M compensated for $ELD > 1$. The general form of the pre-filter ($FF(j\omega)$) for a feedforward modulator is given by [12,13]

$$FF(j\omega) = \frac{\gamma_N s^N + \gamma_{N-1} s^{N-1} + \ldots \gamma_1 s + \gamma_0}{s^N + \alpha_{N-1} s^{N-1} + \ldots \alpha_1 s + \alpha_0} \tag{3}$$

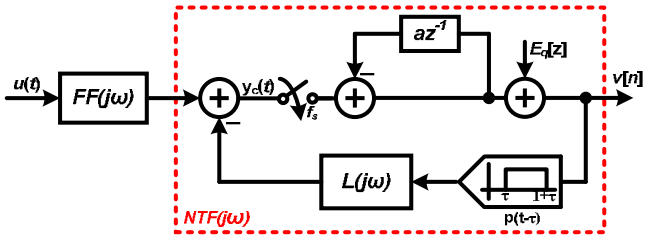

Fig. 4 Linear model used in the derivation of $STF_{new}(j\omega)$.

where N is the order of the loop-filter. The key for avoiding the peaking in the STF and achieving a monotonic roll-off is an *all-pole* $FF(s)$ which requires $\gamma_N = \gamma_{N-1} = \gamma_1 = 0$. Also, the value of γ_0 can be linked to the DC gain of the STF. Fig. 5 shows the STF's of a 4^{th}order CT-$\triangle\Sigma$M with OSR = 16, designed for ELD = 0.5 and 1.5 respectively. The figure clearly illustrates that the out-of-band peaking in the

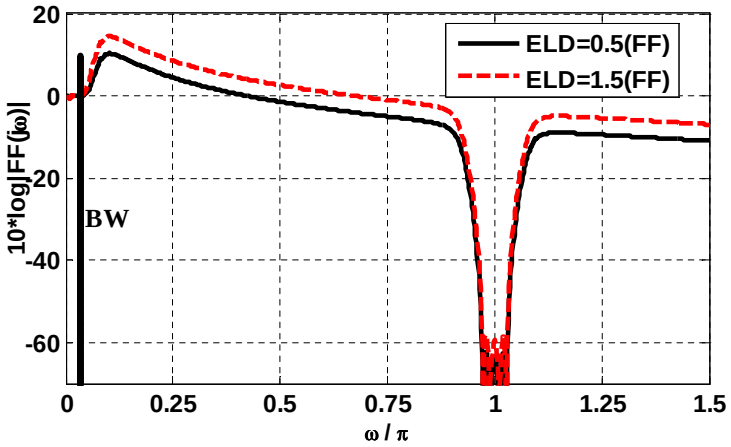

Fig. 5 Comparison of $|STF(j\omega)|$ and $|STF_{new}(j\omega)|$.

CT-$\triangle\Sigma$M compensated for $ELD = 1.5$ is increased by at least $6\,dB$, (i.e) almost doubled, when compared to the design with ELD = 0.5. Further, any decrease in the OSR of the modulator results in significant increase in STF peaking. For low-OSR designs (OSR < 16), the aggravated peaking appears closer to signal band edge of the modulator. This peaking translates into degradation in the dynamic range (DR) of the modulator due to the increased signal content in $y_c(t)$ which overloads the quantizer. Also, an amplified blocker in this frequency range will significantly degrade the modulator DR and can induce instability for large input signal swing.

In order to understand the increased peaking in STF, consider the pole-zero plots for $FF(j\omega)$ and $FF_{new}(j\omega)$ shown in the Fig. 6. In literature, for an n^{th}-order loop-filter, the coefficients $K = [k_0\, k_1\, k_2 \ldots k_n]$ are typically obtained by least-square fitting the impulse response ($l[n] = [0\ l_1\ l_2\ l_3 \ldots]$) of discrete-time loop filter, $L(z) = 1 - NTF^{-1}(z)$, to the continuous-time loop-filter,$L_c(s)$, using the impulse in-

variance transformation (IIT) for the selected feedback DAC pulse shape [2,19]. Now,

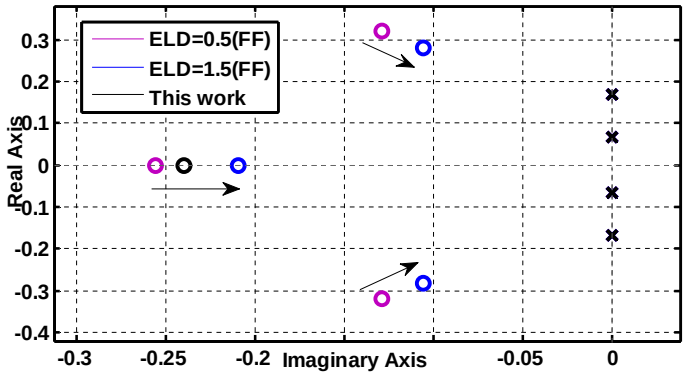

Fig. 6 Pole-zero plot of $FF(j\omega)$ and $FF_{new}(j\omega)$ for CT-$\triangle\Sigma$M compensated for ELD = 0.5 and 1.5.

since the fast-loop using the S/H restores the second sample (l_1) of the open-loop response, the remaining samples ($l_{new}[n] = [0\ l_2\ l_3 \ldots]$) are restored by appropriately choosing loop-filter coefficients $K = [k_0\, k_1\, k_2 \ldots k_n]$ by least-squares fitting. Due to the increase in magnitude of samples in $l_{new}[n]$, when compared to $l[n]$, the loop-filter co-efficients K have to be large enough to fit the $l_{new}[n]$ to the continuous-time loop-filter response,$L_c(s)$. Also, table 1 shows the loop-filter coefficients of a fourth-order NTF with NRZ DAC pulse with ELD = 0.5 and 1.5 in a feedforward architecture.

Table 1 Coefficients of a forth order $NTF(z)$ for ELD < 1, $= 1.5$ for the feedforward architecture

ELD	k_0	k_1	k_2	k_3	k_4	a
0.5	0.5895	1.3493	0.7200	0.2378	0.0388	0
1.5	0.9532	2.1209	0.8933	0.2250	0.0145	1.3418

The increase in the values of K correspondingly increases the magnitude of the co-efficients $\gamma_N, \gamma_{N-1} \ldots \gamma_1$ of $FF(j\omega)$, which results in pushing the zeros of $FF_{new}(j\omega)$ closer to the $j\omega$- axis. This results in aggravated peaking in the STF. Despite of the fact that higher BW is achieved through this ELD compensation method, the resultant peaking in the STF considerably affects the AAF performance of the CT-$\triangle\Sigma$M (see Fig. 5). Also, Fig. 7 shows the Bode plot comparison of $FF(j\omega)$ and $FF_{new}(j\omega)$.

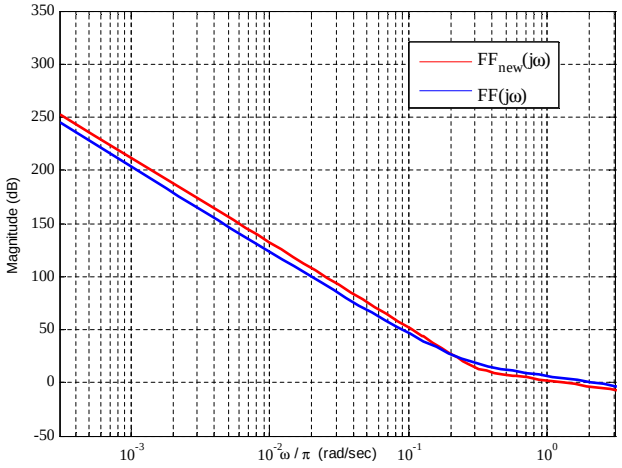

Fig. 7 Pole-zero plot of $FF(j\omega)$ and $FF_{new}(j\omega)$ for CT-$\triangle\Sigma$M compensated for ELD = 0.5 and 1.5.

2.2 CT-$\triangle\Sigma$ Modulator Architecture and Design Procedure for Reduced STF-Peaking

To mitigate the out-of-band STF peaking in a feedforward CT-$\triangle\Sigma$M , additional feed-in coefficients can be introduced [12]. Fig. 8 shows the proposed CT-$\Delta\Sigma$M architecture with reduce STF peaking and thus improved anti-alias filtering performance. The modulator employs a 4-bit quantizer, with a sample rate of $1\,GHz$ in a $0.13\mu m$ CMOS technology and an OSR of 16 to achieve a signal bandwidth of $30\,MHz$. A 4^{th}-order NTF is chosen to compensate for the SQNR reduction due to the additional NTF-zero in $NTF_{new}(z)$ and achieve at least 13-bit ENOB performance. A combination of feedforward (k_1,k_2,k_3), feedback (k_4) and feed-in (b_2) coefficients with NRZ feedback DACs (to implement the feedback and the k_0 paths) are used in this design. This hybrid architecture eliminates an additional summing opamp before the quantizer. Here, the quantizer delay is $1.5\,T_s$ to enable the 1 GHz-sampling rate in the selected technology. This delay is compensated by a fast-path using the sample and hold and a slow-path using a feedback DAC (k_0). The NTF out-of-band gain (OBG_{orig}) is set to 2 (or $6\,dB$) which corresponds to an OBG_{new} of $13\,dB$ in the resulting $NTF_{new}(z)$ as shown in Fig. 9.

The systematic design procedure for the hybrid architecture is as follows: First, a desired 4^{th}-order inverse-Chebyshev $NTF(z)$, given in equation-4, is chosen for the target SQNR.

$$NTF(z) = \frac{\left(z^2 - 1.996z + 1\right)\left(z^2 - 1.971z + 1\right)}{\left(z^2 - 1.2z + 0.3746\right)\left(z^2 - 1.425z + 0.6564\right)} \tag{4}$$

Then, by using the *impL*1 command in the Schreier's Toolbox [2], the value of second sample '**a**' is found. Fig. 10 shows the discrete-time equivalent impulse response, $l[n]$, of the loop filter $L(s)$ for the chosen $NTF(z)$. Also, fig. 9 shows the comparison

of the desired $NTF(z)$ with $NTF_{new}(z)$ achieved through the design. Then, after removing the second sample and advancing the remaining samples (i.e. $[0\ l_2\ l_3 \ldots]$), the equivalent IIR transfer function ($L_1(z)$) is found by using the *prony* fitting function in MATLAB. Using the resultant transfer function and the DAC pulse shape, $L(s)$ is computed, which is given by the equation-5.

$$L(s) = \frac{\left(0.9532s^4 + 2.1209s^3 + 0.9249s^2 + 0.2857s + 0.0402\right)}{(s^2 + 0.03305s^2 + 0.0001274)} \tag{5}$$

For the 4^{th}- order feedforward and feedback hybrid topology shown in the fig.8 the state space (ABCD) matrices of the modulator are

$$A = \begin{bmatrix} 0 & -g_1\omega_1 & 0 & 0 \\ \omega_2 & 0 & 0 & 0 \\ 0 & \omega_3 & 0 & -g_2\omega_3 \\ k_1\omega_4 & k_2\omega_4 & k_3\omega_4 & 0 \end{bmatrix} \quad B = \begin{bmatrix} -\omega_1 & \omega_1 \\ 0 & b_2\omega_2 \\ 0 & 0 \\ -k_4\omega_4 & 0 \end{bmatrix}$$
$$C = \begin{bmatrix} 0\ 0\ 0\ 1 \end{bmatrix} \qquad D = \begin{bmatrix} k_0\ 0 \end{bmatrix}$$

The resultant parametric transfer functions $L(s)$ and $FF(s)$ are given by

$$L(s) = \frac{-\left(X_4s^4 + X_3s^3 + X_2s^2 + X_1s + X_0\right)}{(s^2 + Z_1)(s^2 + Z_2)}$$
$$FF(s) = \frac{\left(Y_2s^2 + Y_1s + Y_0\right)}{(s^2 + Z_1)(s^2 + Z_2)}$$

where the parametric equivalents of X_i and Y_j coefficients and their set of equations are shown in table-2. Here, the goal is to eliminate one of the zero's of $FF(s)$ or by nulling out the s^2- term, i.e. $Y_2 = 0$. Also, in order to nullify the Y_1 term, an additional feed-in b_1 co-efficient will need to be introduced into the loop-filter. However, this will significantly increase the signal content at $y_c(t)$ and consequently alter the value of 'a' and thus further reducing the MSA and degrading the dynamic range. Thus, in this design only a single feed-in coefficient (b_1) is employed to achieve reduced STF-peaking.

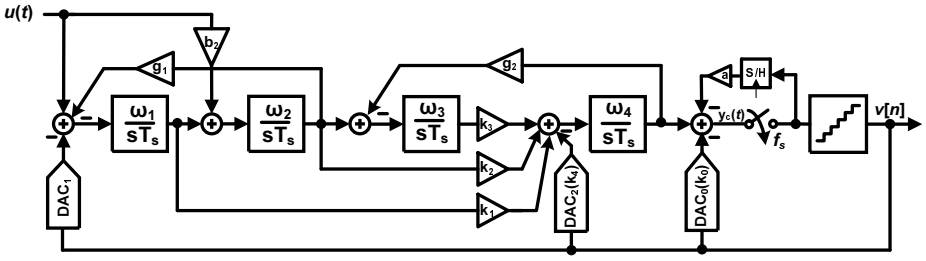

Fig. 8 Proposed CT-$\Delta\Sigma$ modulator architecture with reduced STF peaking.

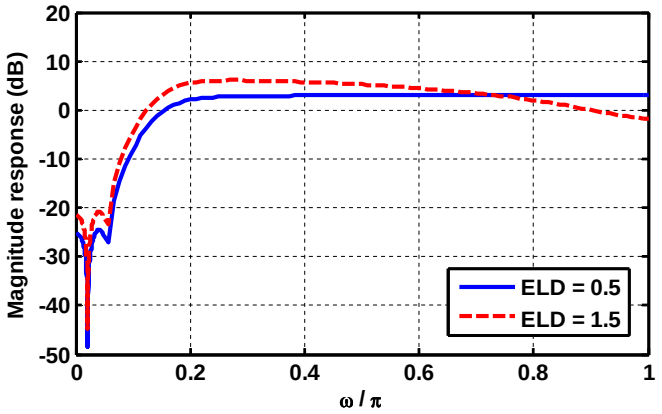

Fig. 9 Comparison of $NTF(e^{j\omega})$ and $NTF_{new}(e^{j\omega})$.

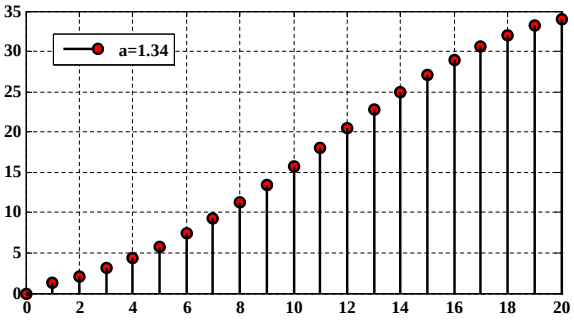

Fig. 10 Discrete-time equivalent impulse response of the loop filter $L(s)$ for the chosen $NTF(z)$

Table 2 $L(s)$ and $FF(s)$ coefficients for the hybrid loop-filter topology

Term	Parametric Equivalent	Parametric Equi. Value	State-Space Variables	Value
X_4	k_0	0.9532	k_0	0.9533
X_3	k_4	2.1209	k_1	0.8932
X_2	$g_1k_0 + k_1 + g_2k_0k_3$	0.9248	k_2	0.2249
X_1	$k_2 + g_1k_4$	0.2857	k_4	0.0401
X_0	$k_3 + g_1g_2k_0k_3$	0.0402	ω_4	2.1210
Z_1	$g_1 + g_2k_3$	0.03305	g_1	0.0286
Z_2	$g_1g_2k_3$	0.0001274	g_2	0.1123
Y_2	$k_1 + b_2k_2$	$\gamma_2 = 0$	b_2	-3.9715
Y_1	$k_2 + b_2k_3 - b_2g_1k_1$	–	–	–
Y_0	k_3	–	–	–

3 Circuit Implementation

3.1 Loop Filter

Fig. 11 shows an active-RC implementation of the proposed CT-$\Delta\Sigma$M architecture seen in Fig. 8. In order to optimize power consumption in the design, the last inte-

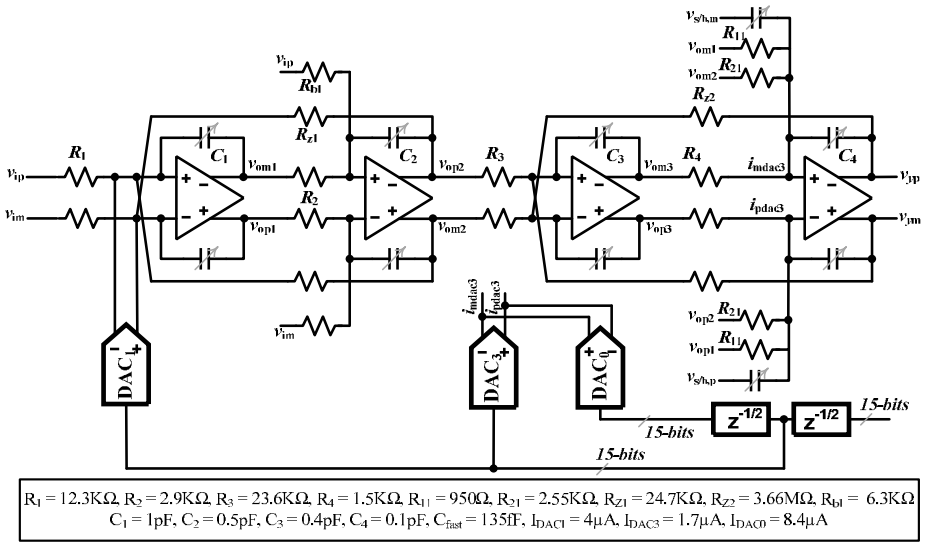

Fig. 11 CT-$\Delta\Sigma$ modulator loop filter.

grator is also used as an adder, along with analog differentiation of the k_0 feedback path using an NRZ DAC, similar to [7,20]. Feedback paths $g_1$and $g_2$are implemented using R_{z1} and R_{z2} resistors. The input, v_{in} is added to the input of second integrator using resistor R_{b2} to implement the feed-in co-efficient b_2. The integrating capacitor is implemented as programmable bank using four control bits to tune for the RC time-constant variation with process. Adding a direct feed-in path from the modulator input $u(t)$ to the quantizer input $y_c(t)$ helps reduce the signal content at $y_c(t)$ [21], but results in a degraded STF, and is thus avoided in this design. A simple source-follower based pseudo-differential sample-and-hold is used to implement the fast path as in [11]. The S/H-based fast-loop output is added to $y_c(t)$ using capacitive addition as shown in Fig. 11.

3.2 Operational Amplifier

Figs. 12& 13 show the schematic of the feed-forward compensated opamps used in the CT-$\triangle\Sigma$ modulator. Low-V_t devices are used for the input diff-pairs in all the opamps to achieve a wider input range. The opamp topology shown in Fig. 12 is used for the first three active-RC stages, with a gradual reduction in bias currents from the first to third stage. The first opamp sets the overall input-referred noise and nonlinearity for the modulator and thus consumes largest amount of power. These opamps employ a telescopic first stage with PMOS diff-pair followed by a class-A output stage. Since g_{m3} shares the bias current with g_{m2}, the topology results in lower power dissipation. To ensure that the opamp common mode output voltage is held at V_{cm}, separate CT common mode feedback (CMFB) loops are used in both of the op-amp stages. The output of first stage (v_{o1p} and v_{o1m}) is averages through $30K\Omega$ resistors and fed to the input transistors and compares it to V_{b4} to tune the output common-mode voltage (V_{CMFB1}). The 100fF capacitors bypass the active

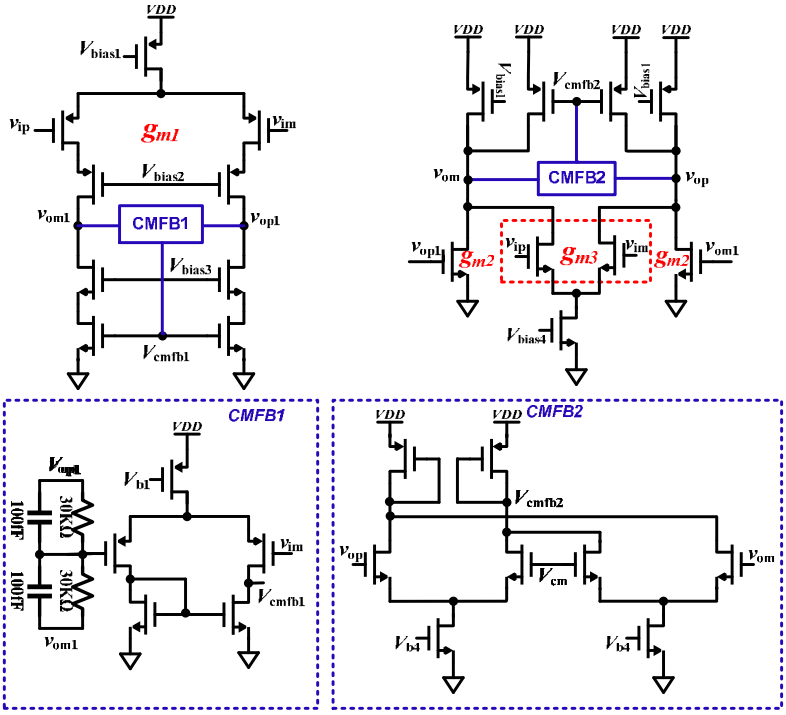

Fig. 12 Two-stage feed-forward compensated opamp with CMFB circuit used in first three integrators.

common-mode detector for high frequencies and help stabilize the loop. Similarly, the CMFB2 circuit shown in the Fig. 12 uses a differential averaging and tune the PMOS current to keep the output node (v_{op} and v_{om}) at V_{CM}. The total current drawn by the first opamp, including the CMFB circuitry, is $3.4\,mA$ from the $1.2\,V$ supply. The performance requirements on the opamps used for the last integrator are high. To achieve high gain/speed opamp, a gain-boosted folded-cascade first stage is used as shown in Fig. 13. To provide sufficient current at the loop-filter output ($y_c(t)$), a class-AB second stage is employed. The total current consumed by this opamp is $6.1\,mA$. Since feed-forward compensated opamps exhibit higher slew-rate performance [22], their usage in the loop-filter leads to significant improvement in the overall modulator linearity.

3.3 Quantizer

A 4-bit Flash sub-ADC, shown in fig. 14, is used to implement the quantizer. The quantizer consists of 15 differential comparators and has a full-scale input range of $1.6\,V_{pp}$ resulting in a step size of $V_{LSB} = 100mV$. The quantizer is designed to meet the specification at the maximum sampling frequency of 1 GHz with the total maximum regeneration delay and the latch delay of 1.2 ns in the slow-slow simulation corner. The comparators used in the quantizer are designed to provide sufficient regenerative gain to mitigate the effects of metastability at the high sampling rate.

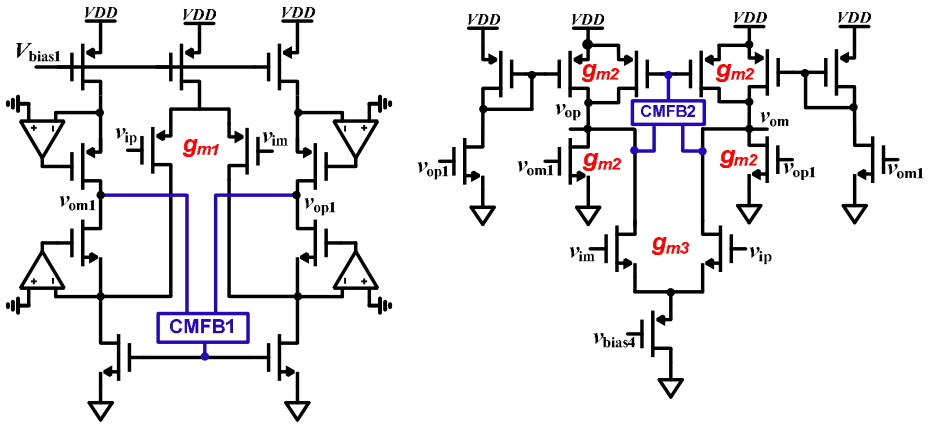

Fig. 13 Two-stage feed-forward compensated opamp with CMFB circuit used in the fourth integrator (implicit adder) and the S/H.

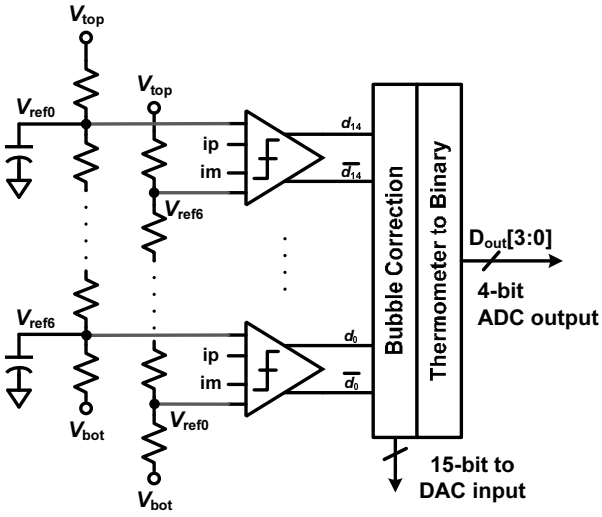

Fig. 14 The 4-bit quantizer used in the CT-$\triangle\Sigma$ modulator.

This presents a trade-off between the performance and the static power consumption in the comparators. Fig. 15 shows the high-speed comparator used in the modulator, similar to [7] with additional current-mode logic (CML) latch stages. Here, the first stage uses a differential difference amplifier for reference subtraction. The amplifier is loaded with cross-coupled PMOS latches to provide initial regeneration followed by a clocked latch. The second stage latch provides a large regenerative gain and resolves the outputs to full logic levels. The latch is disconnected from the input to avoid kickback noise and a reset phase is used to remove the memory in the latches. A cascade of three latches sufficiently resolves the analog difference into logic levels. The timing of the latches is shown in the fig. 15. A trimming current DAC is employed

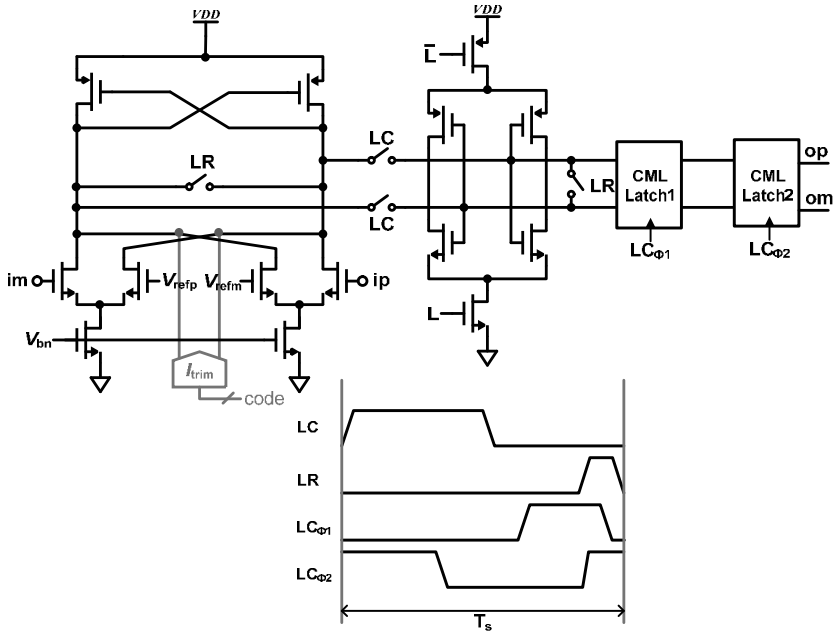

Fig. 15 Comparator circuit used in the quantizer with timing diagrams[7].

for the comparators to compensate for the mismatch in the diff-pairs and the tail current sources as in[7].

3.4 DAC

As seen in the schematic in Fig. 8, three current-steering DACs are employed in the modulator with bias currents of ($I_{DAC0} = 4\mu A$, $I_{DAC1} = 1.8\mu A$ and $I_{DAC2} = 8.7\mu A$) respectively. The feedback loop can tolerate mismatch errors in the inner DACs (DAC_0 and DAC_3) as the errors are noise-shaped by the loop. However, any nonlinearity in the feedback DAC at the modulator input (DAC_1) will directly be observed at the output. Traditionally data weighted averaging (DWA) technique has been employed to noise shape the mismatch errors in the DAC elements[2]. However, DWA will introduce a 4-bit barrel shifter in the feedback loop and contribute at least 400ps excess delay. In the selected process, it was observed that at sampling rates greater than around 600 MHz, DWA-based DAC mismatch noise-shaping techniques become infeasible. Thus, to minimize any additional delay in the feedback loop, a calibrated DAC shown with redundancy is employed[21]. Fig. 16 shows the feedback DAC used in the modulator along with a unit current steering cell with calibration circuitry. The DAC unit cell uses fixed current references for supplying 80% of the total unit current and a tunable current reference is used to provide 20% tunability in the DAC current. A unit DAC cell employs a redundant cell to enable online calibration. While in operation, one of the DAC pairs are selected sequentially and calibrated against reference current cells ($I_{ref,p}$ and $I_{ref,m}$) using an analog calibration loop as shown in Fig 16 [21].

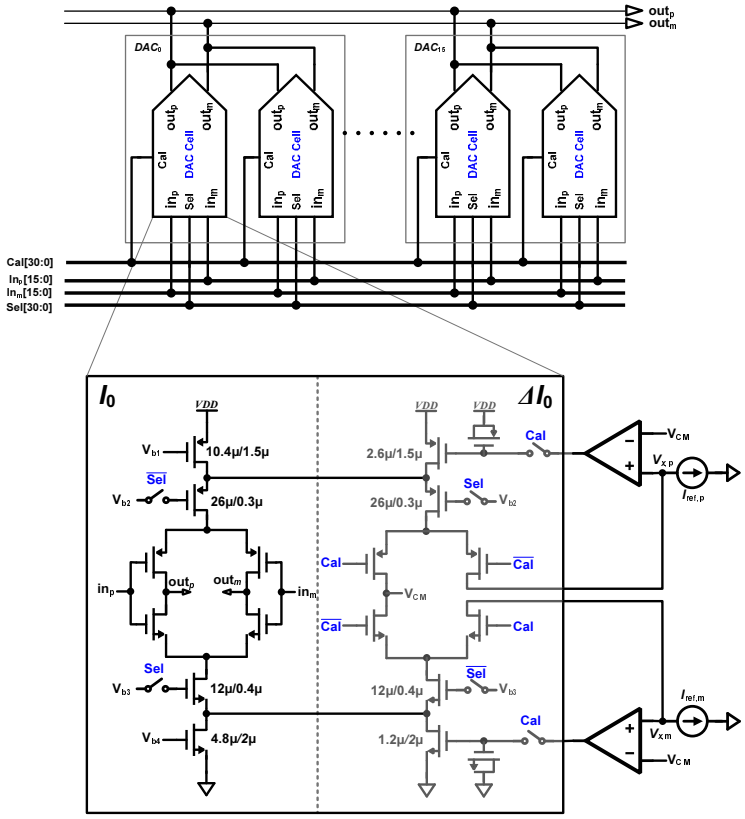

Fig. 16 The calibrated current steering DAC architecture [21].

Following concerns are carefully taken into account to achieve better dynamic performance from the unit DAC cell: (i) imperfect synchronization of the control signals at the switches, (ii) source-coupled node variation of the current-source transistors, and (iii) coupling of the control signals through the switches to the output. A high crossover DAC driver is employed to reduce the glitching energy in the DAC cells.

4 Simulation results

The 4^{th}-order CT-$\triangle\Sigma$ ADC has been implemented in the $0.13\,\mu m$ IBM CMOS process. Transistor-level simulations of the CT-$\triangle\Sigma$ modulator were performed using Spectre and the results were post-processed using MATLAB. Fig. 17 shows the simulated STFs of feedforward ($ELD = 0.5$) and the proposed modulator architecture ($ELD = 1.5$). It can be observed that the STF out-of-band peaking is substantially reduced by 24 dB. 18 shows the PSD of the modulator output for a $15.5\,MHz$ input tone with $-2.5\,dBFS$ amplitude, and the simulated SNR/SNDR and DR respectively. A $8K$-point FFT with Hann window is used for spectral estimation. The peak simulated SNR of the modulator is $72.5\,dB$ and the DR is $76.3\,dB$. The CT-$\triangle\Sigma$

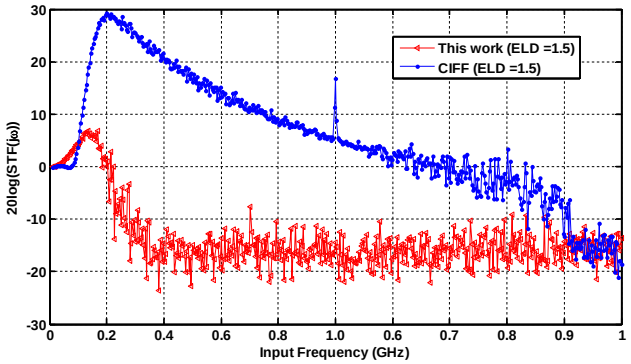

Fig. 17 Simulated STF response for the conventional feedforward and the proposed modulator with ELD=1.5.

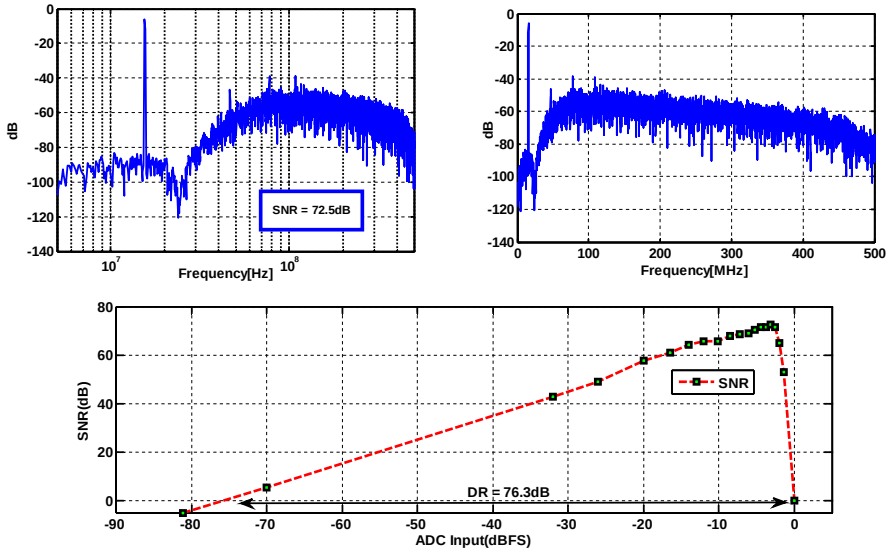

Fig. 18 Simulated performance of the proposed CT-$\triangle\Sigma$M at 1GS/s and $BW = 31\,MHz$ ($OSR = 16$).

modulator dissipates around $34\,mW$ power from a 1.2V supply and achieves a figure of merit ($FoM = \frac{P_d}{2^{ENOB}\cdot 2\cdot BW}$) of $0.189\,pJ/level$.

5 Conclusion

A 1GS/s CT-$\triangle\Sigma$M, using a quantizer with 1.5 clock cycle delay, is designed in $0.13\mu m$ CMOS technology to achieve 31 MHz conversion bandwidth. The total power consumption of the modulator is $34\,mW$. Also, the effect of 1.5 clock-cycle excess loop-delay compensation on the STF of feedforward architecture has been analyzed. A design method to improve the STF performance of the modulator is presented

Table 3 Performance Summary

	This work	[7]	[6]	[22]
Process	0.13 μm	0.13 μm	0.13 μm	0.18 μm
Supply Voltage	1.2 V	1.2 V	1.5 V	1.8 V
Sampling rate (MHz)	1000	640	900	300
BW (MHz)	31	20	20	15
Power Dissp. (mW)	34	20	87	20.7
DR(dB)	76.3	80	80	70
SNR_{max}(dB)	72.5	76	81.2	67.2
$SNDR_{max}$(dB)	72.5	74	78.1	63.2
STF peaking (dB)	9dB	-	-	-
FoM (pJ/conv.)	0.189	0.122	0.330	0.37

which results in 24dB reduction in out-of-band peaking. The transistor-level simulation results of the proposed CT-$\triangle\Sigma$M exhibit a peak SNR of 72.5dB, a dynamic range of 76.3dB with a MSA of $-2.5dBFS$.

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