

A 10.7-MHz CMOS SC Radio IF Filter Using Orthogonal Hardware Modulation

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Abstract—FM radio receivers require an IF filter for channel selection, customarily set at an IF center frequency of 10.7 MHz. Up until now, the limitations of integrated radio selectivity filters in terms of power dissipation, dynamic range, and cost are such that it is still required to use an external ceramic 10.7-MHz bandpass filter. This paper demonstrates a CMOS switched-capacitor IF filter that can be integrated with most of the rest of the FM receiver, eliminating external components and printed circuit board area. This is made possible through a combination of two techniques: orthogonal hardware modulation, and delta-charge redistribution. It exhibits a tightly controlled center frequency with a Q of 55 and also contains a programmable gain. The filter occupies an area of 0.7 mm² in a 0.6- μ m CMOS process with poly-poly capacitors. The new filter requires only 16 mW of power, and this is offset by elimination of the power needed in current designs to drive off-chip filters.

Index Terms—AGC, analog CMOS, bandpass filter, IF, N-path, orthogonal hardware modulation, radio, switched capacitor.

I. INTRODUCTION

THE MAIN AIM in the innovation of portable radio receivers is the ever-further integration of more and more functions on chip to drive down costs and power consumption. The use of CMOS technology is a big step in this direction, since it offers the possibility of integration of analog and digital processing on a single chip. One function that has remained external up until now is the IF selectivity filter, since it has not been possible to create a filter in IC technology that comes near the accuracy and low cost of a ceramic filter [1]. Many attempts have been made in the past in both BiCMOS and CMOS technologies, using both continuous-time (CT) and switched-capacitor (SC) techniques, but these do not meet the specifications of portable radio [2]–[4].

SC techniques are suitable for application in a CMOS-only technology, for instance, as part of discrete-time channel that includes digital signal processing. Applications include both recursive and linear-phase filters, A/Ds, and demodulators [6]–[9]. For high-frequency narrow-band filters, in particular, SC techniques offer a number of advantages. First, the external clock reference frequency can be used to tightly control the center frequency without a separate tuning control loop as

needed by CT filters. Second, simple amplifier structures can be used in which linearity (slewing) is not a major issue. Instead, the amplifiers must be optimized to have a good step response, with sufficient dc gain and bandwidth to ensure the SC circuit can settle to its end value within a single clock cycle. The allowance of some slewing in the step response means SC circuits are capable of dealing with large signal swings.

In this paper, a low-power sixth-order SC bandpass filter (BPF), with added selectable gain control, is presented for 10.7-MHz radio IF selectivity. It goes further than previous designs in the literature in achieving the required specifications of a portable FM radio receiver. The filter design is based on an N -path technique that, through a process of orthogonal hardware modulation, tolerates some path mismatch. All the required circuitry—including sample-and-holds and clocks—are placed on board the IC to get a complete picture of the performance of the filter.

The paper is divided into seven sections. In Section II, the IF BPF is placed in a system context and the adaptation of the traditional radio receiver to include SC filtering is examined. The BPF design procedure based on the N -path technique is presented in Section III. The design concepts of orthogonal hardware modulation and delta-charge redistribution are presented in this section. Section IV deals with the actual circuit implementation and layout of the realized filter. The measurement results are presented in Section V. Finally, in Section VI, a short summary is given of this work and its significance.

II. SYSTEM CONTEXT

Practically every FM receiver made today makes use of at least one 10.7-MHz ceramic BPF for channel selectivity. Some high-quality applications, such as car radio, even require four ceramic BPFs [10]. This BPF must distinguish the wanted FM band of 200 kHz from the broad-band IF signal after demodulation in the RF front-end. Although ceramic filters have the advantages of being cheap and reliable, they cost printed circuit board (PCB) area and require input and output pins. Although passive, they require input and output buffering and are susceptible to pick-up from the PCB. For car radio, as mentioned, the chain of four BPFs requires eight pins and buffers.

CMOS technology offers the possibility of integration of both receiver and digital processing circuitry on a single chip if an extremely accurate and high dynamic range CMOS IF filter is available. Since the RF gain control range is limited in CMOS designs, an IF filter that can provide some of this gain control is preferred. Fig. 1 shows a general simplified FM receiver chain, including the possible application of the SC filter. All radio receivers have a readily available crystal reference frequency, so the clock generation for the SC BPF is not a significant overhead.

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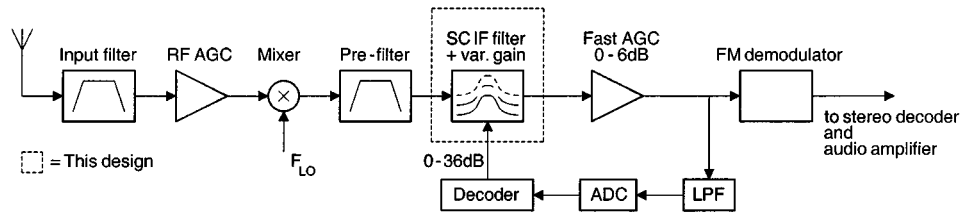
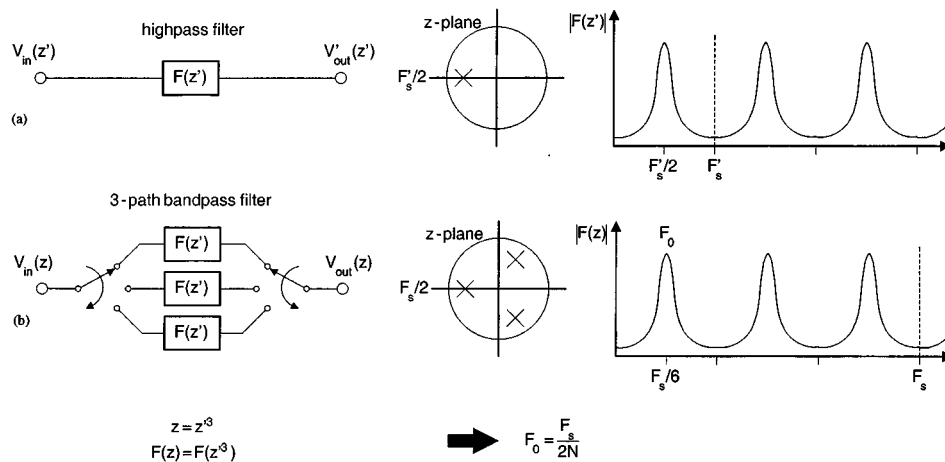


Fig. 1. SC IF filter for portable FM radio.

Fig. 2. Known solution for accurate F_o : the N -path technique. (a) first-order HPF, (b) third-order 3-path BPF.

Some prefiltering is needed, as explained in Section III, in order to attenuate those frequency components that can alias in to the filter band. The BPF contains a distributed coarse gain control with a range of 36 dB in steps of 6 dB. The fine gain control with a range of 6 dB (in steps of 0.2 dB) can be implemented in the subsequent digital hardware. The possibility of integrating the ceramic BPF function gives the designer extra flexibility—a center frequency of 10.7 MHz does not have to be chosen any longer, and another more convenient frequency could be chosen. Unlike a ceramic filter, an active BPF has no insertion loss (containing even a gain in this case), but it has a limited dynamic range. The integrated BPF should not contribute significantly to a reduction in performance of the fully integrated receiver compared to one in which an external ceramic filter is used.

The typical specifications of such a ceramic filter are 10.7 MHz \pm 30 kHz. The 3-dB bandwidth is 200 kHz. A group delay variation of $<1 \mu\text{s}$ within this bandwidth is acceptable for FM demodulation. An integrated version of this filter should, therefore, have a Q higher than 53. It was also estimated that, for portable radio applications, the intermodulation-free dynamic range should be greater than 70 dB. Since chip area and power dissipation are very important for low-cost portable radio applications, we set our goal at maximizing performance for a chip area of under 1 mm² in 0.6- μm CMOS and a dissipation of circa 15 mW.

III. BANDPASS FILTER DESIGN BASED ON N -PATH TECHNIQUE

The power of using analog sampled data (ASD) techniques is that highly accurate circuits can be realized based on relative

accuracy on-chip (through capacitor ratios in SC circuits), and on absolute accuracy off-chip (clock frequency). Moreover, the clock can be used to determine an accurate positioning of the filter characteristic in the frequency domain. Consider, for instance, the classic N -path technique [5]: through N -path hardware modulation of a filter function $F(z)$, the Nyquist bandwidth is increased N times and a new filter function $F(z^N)$ arises. In this way, it is possible to transform a sampled lowpass filter (with poles centered around dc), or a sampled high-pass filter (with poles centered around half its sample frequency), to a BPF. In Fig. 2, for example, the Nyquist bandwidth of the single-pole high-pass filter is expanded three times through hardware modulation, to create a third-order N -path filter with a bandpass response centered at $F_s/6$. An N -path BPF can be realized in which the center frequency F_o is directly determined by the sample clock frequency (with frequency F_s) through $F_s = F_o \times 2N$. An error in the coefficient value that determines the position of the pole only affects the bandwidth of the eventual BPF. Note that in classic N -path filters, the filter order is fixed by the number of parallel paths N .

A. Possible Problems with the N -path Technique

The two major problems in realizing the classic N -path filter using ASD techniques are pattern noise (modulation of dc) and in-band aliasing (modulation of the signal), both of which are due to expected component mismatch between the N paths. Path mismatch results in F_s/N subsampling. For N -path BPFs based on a lowpass prototype, upsampled dc components appear at $F_s/N, 2F_s/N$, etc., producing pattern noise within the passband. To avoid this, N -path BPFs based on a high-pass

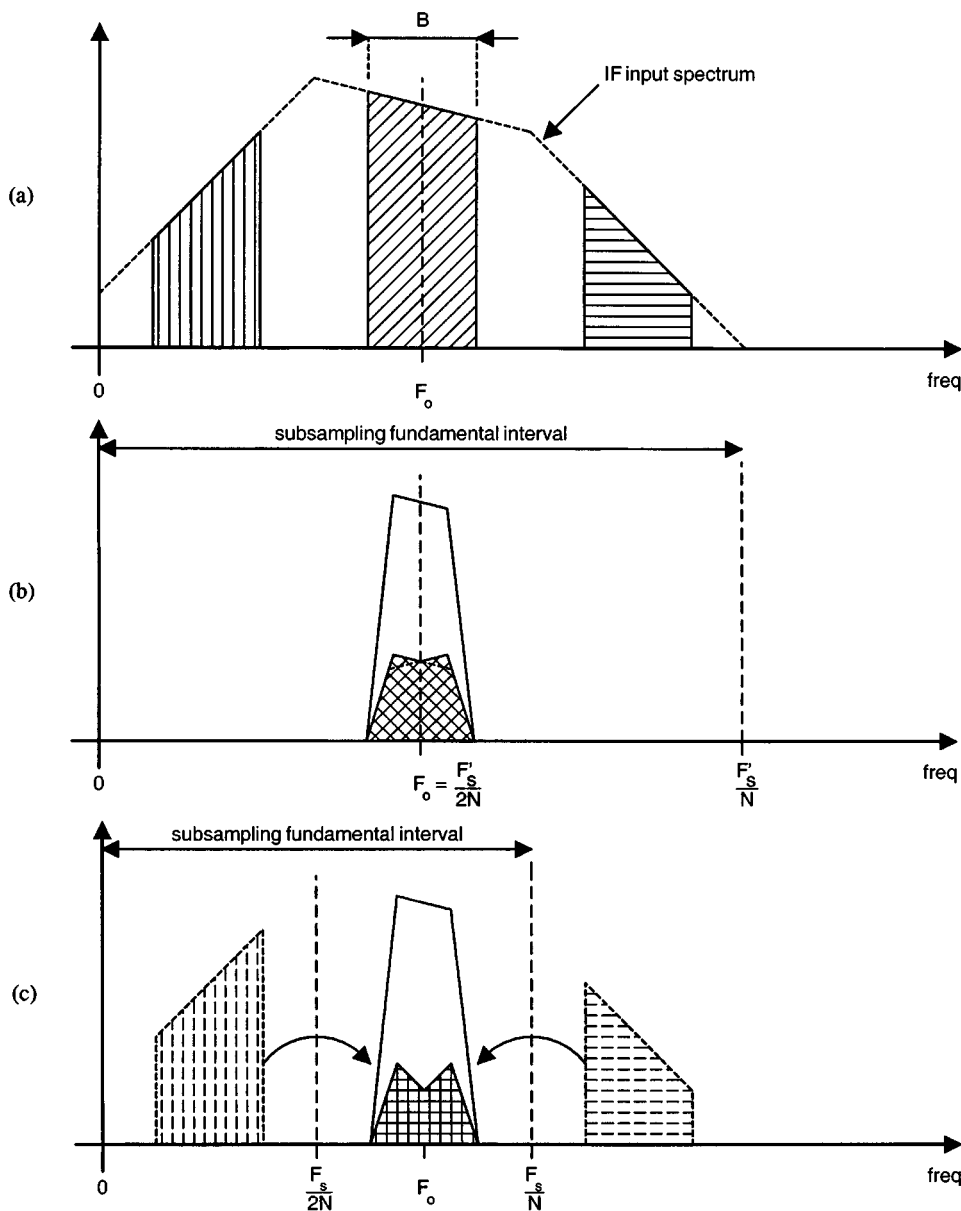


Fig. 3. Aliasing due to path mismatch in N -path filters. (a) Filter input spectrum, including band of interest B . (b) In-band aliasing in classic N -path filter ($N = n$). (c) Out-of band aliasing after decoupling number of paths N from filter order n ($N > n$).

filter prototype are preferred. However, these filters suffer from in-band aliasing due to path mismatch, since the edge of the subsampling Nyquist bandwidth (e.g., $F_s/6$ in Fig. 2) falls *within* the passband. This effect is visualized in Fig. 3(a) and (b). Consider an input signal spectrum, such as shown in Fig. 3(a), in which a small band of bandwidth B centered at F_o has to be filtered. When this spectrum is filtered by a classic three-path BPF based on a high-pass filter prototype ($F_s = 6F_o$), path mismatch causes frequency components at $F_o + \delta F$ to fold back in attenuated form to $F_o - \delta F$, and vice versa. For $\delta F < B/2$, in-band aliasing occurs. No pre- or post-filtering can alleviate this process. In theory, a symmetrical signal spectrum, such as in this FM radio application, would not be degraded by this symmetrical in-band aliasing. In practice, however, the center of the FM IF band is never located at exactly the BPF center frequency F_o due to inaccuracies in the RF mixing and/or inaccuracy in the

frequency arising from the clock frequency synthesizer. The FM signal becomes distorted due to the cross-modulation of Bessel components.

B. Improved N -path Technique using Orthogonal Hardware Modulation

The solution is to introduce a design method, using *orthogonal hardware modulation*, which ensures that the consequences of hardware imperfections (giving rise to path mismatch) can be treated independently of the signal processing. This is carried out in this design by introducing an extra degree of freedom, where the number of hardware paths N (*hardware modulation*) is decoupled from the *functional modulation* factor n , as introduced by the transformation $z \rightarrow z^n$.

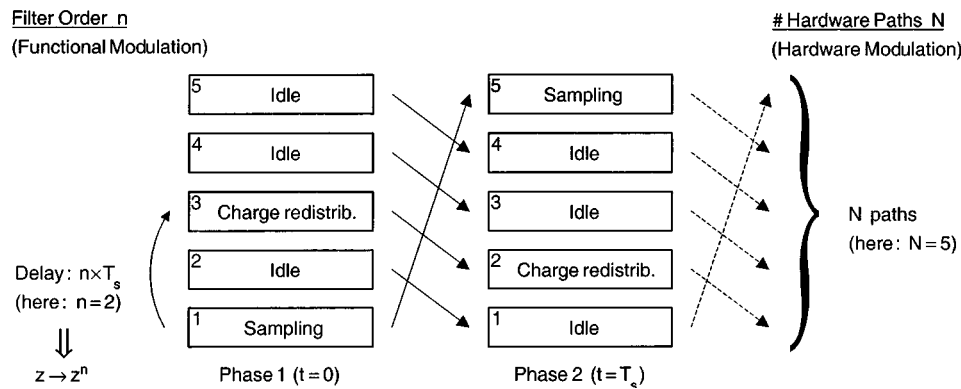


Fig. 4. Illustration of orthogonalization in an N -path filter.

This design method is shown conceptually in Fig. 4 for two consecutive sample clock phases of a single path of a five-path second-order filter. Five pieces of similar hardware (five-path) are set out vertically—these can be, for instance, five sets of switched capacitors, each with three separate functions, namely sampling, charge redistribution and idling. The function rotation of each piece of hardware is set out horizontally in time, from one sample instant to the next. The functional modulation n is determined by the delay between sampling and charge redistribution (here $n = 2$). Every period T_s , a new sample is taken and processed. For instance, at $t = 0$, hardware piece “1” samples the input; at $t = T_s$, “5” samples the input; at $t = 2 \times T_s$, “4” samples the input, etc. After $5T_s$, the whole process starts again. In this case, the hardware modulation is given by $N = 5$.

The basis cell per path is normally a simple first- or second-order filter. For instance, a first-order high-pass filter cell is modulated to an n th-order N -path filter, where n gives the number of resonance peaks contained in the Nyquist bandwidth of the N -path filter. Knowing F_o and n , the sampling frequency F_s is chosen as

$$F_s = F_o \times 2n. \quad (1)$$

Next, N is chosen such that in the event of path mismatch, 1) no sub-harmonics of the clock at integer multiples of F_s/N (which are caused by the unwanted upsampling of dc components) appear within the frequency band of interest, 2) no aliasing from inside the band can occur back into the band (due to the unwanted subsampling of the signal with F_s/N), and 3) those frequency components from outside the filter band that are capable of folding back into the band can be attenuated in advance with the simplest prefilter. Referring to Fig. 3(c), in order to satisfy points 1) and 2), N must be chosen such that any subsampling Nyquist edge frequency (per path) does not fall within the BPF passband, i.e.

$$i \times \frac{F_s}{2N} \notin \left[F_o - \frac{B}{2}, F_o + \frac{B}{2} \right], \quad i = 0, 1, 2, \dots \quad (2)$$

Furthermore, to satisfy point 3) for ease of prefiltering, N should be chosen such that F_o fits approximately half way inbetween two consecutive subsampling Nyquist edge frequencies, i.e.

$$N = \lceil 1.5 \times n \rceil. \quad (3)$$

For example, a second-order BPF (poles at $F_s/4$) should have $N = 3$; whereas, say, a fifth-order BPF (poles at $\pm F_s/10$, $3F_s/10$, $F_s/2$) should have $N = 7$. Note that for certain applications, the choice of N may be ultimately determined by the need to avoid certain critical out-of band frequencies from folding back in band; for a radio application, this could be a nearby channel which is known to be very strong with respect to the wanted channel.

C. Delta Charge Redistribution

Finally, a choice has to be made for circuit implementation. A standard circuit solution for SC filters is based on the charge transfer (QT) stage drawn in Fig. 5(a). Here C_s samples the input voltage on one clock phase and has its charge transferred to integrator capacitor C_i on the following clock phase via the virtual earth node of the amplifier. The amplifier in the QT stage has the dual function of providing 1) charge transport via its virtual earth node (*active* charge redistribution), and 2) buffering so as to allow the following stage to read the output voltage without affecting the charge on the capacitors. Finite amplifier dc gain and bandwidth cause incomplete charge redistribution due to incomplete charge transfer in one clock cycle. Two (damped) SC stages similar to this one shown in Fig. 5(a), placed in series within a closed loop, form the basis of the SC biquad filter, much in use even for high-frequency BPFs [6], [7], [9].

Instead of using the QT circuit, a more efficient circuit implementation has been chosen for the radio IF filter based on *delta-charge redistribution* (δ - QR), illustrated in Fig. 5(b). Here C_a is used to both sample the input voltage and damp the integrator capacitor C_b . There is *passive* redistribution of charge between C_a and C_b by connecting them in parallel, which is unaffected by amplifier errors. In fact, the principle purpose of the amplifier is buffering only. Only the parasitic capacitances must be charged up from one clock cycle to the next—hence the term *delta-charge redistribution*. The circuit technique of Fig. 5(b) allows N -path with orthogonal hardware modulation and delta-charge redistribution to be combined in one single stage, as will be seen in Section IV. It is also possible to include a gain control function by adding extra capacitors at the input which regulate the amount of signal charge transferred to C_a and C_b in parallel. There is only a single transfer of charge from input to output, enabling high settling accuracy.

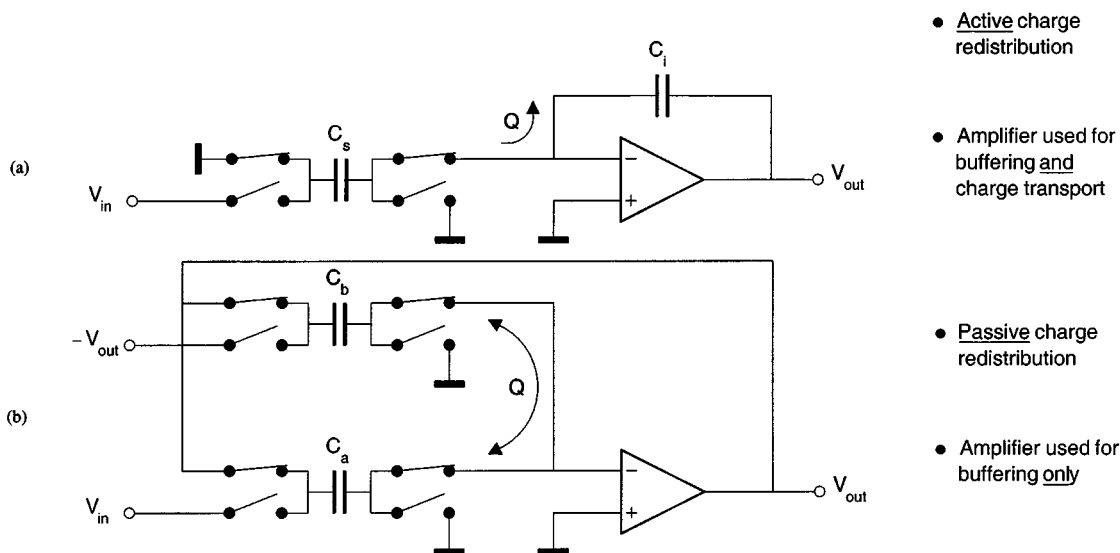


Fig. 5. QT circuit (a) compared to δ - QR circuit and (b) as basis for a SC resonator.

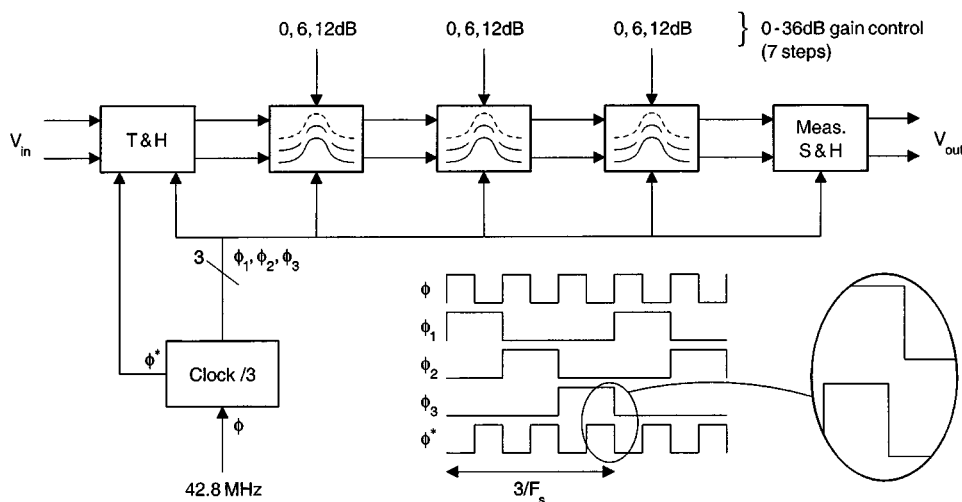


Fig. 6. Functional design of SC BPF.

IV. DESIGN OF RADIO IF FILTER CIRCUITRY

The block schematic of the SC IF filter, together with peripheral circuitry, is depicted in Fig. 6. A single second-order BPF with a Q -factor of 55 would have a bandwidth that is too sensitive to process variations, so instead the Q -factor has been spread over a cascade of three identical fully differential second-order BPF sections. Since F_o is principally dependent on the clock, N -path δ - QR BPF sections can be cascaded while still maintaining a very accurate center frequency for the overall filter. A cascade of standard SC biquad filters, on the other hand, would show too high a center frequency sensitivity. In general, for m cascaded second-order sections, the Q of each section is given by

$$Q_{\text{sect}} = Q_{\text{tot}} \times \sqrt{2^{1/m} - 1}. \quad (4)$$

For $m = 3$, Q_{sect} should be 28. Each BPF section provides a selectable gain of 0, 6, and 12 dB for use by the IF AGC. The filter is preceded by a track-and-hold (T&H) to allow for ac-

curate sampling of the wide-band continuous-time input signal. Finally, a sample-and-hold buffer (S&H) is added for measurement purposes. All stages are driven by an on-board three-phase clock.

A. SC Filter Design

A second-order ($n = 2$) N -path BPF requires $N = 3$, as discussed in Section III. With path mismatch, frequency components around $1/3 F_o$ and $5/3 F_o$ fold back in attenuated form around F_o . This can be reduced by a simple prefilter. With $n = 2$, the sample frequency of the radio IF BPF is $F_s = 4F_o = 42.8$ MHz, in which the two poles are placed at exactly $z = \pm j\beta$. The filter is realized based on delta-charge redistribution in order to create a low-sensitivity Q .

In Fig. 7, the circuit schematic of one three-path BPF section is depicted. It makes use of the δ - QR stage of Fig. 5(b), in which the amplifier is shared between the paths. Although the function of each path (sample, idle, and passive charge redistribution)—as determined by the state of the switches—rotates

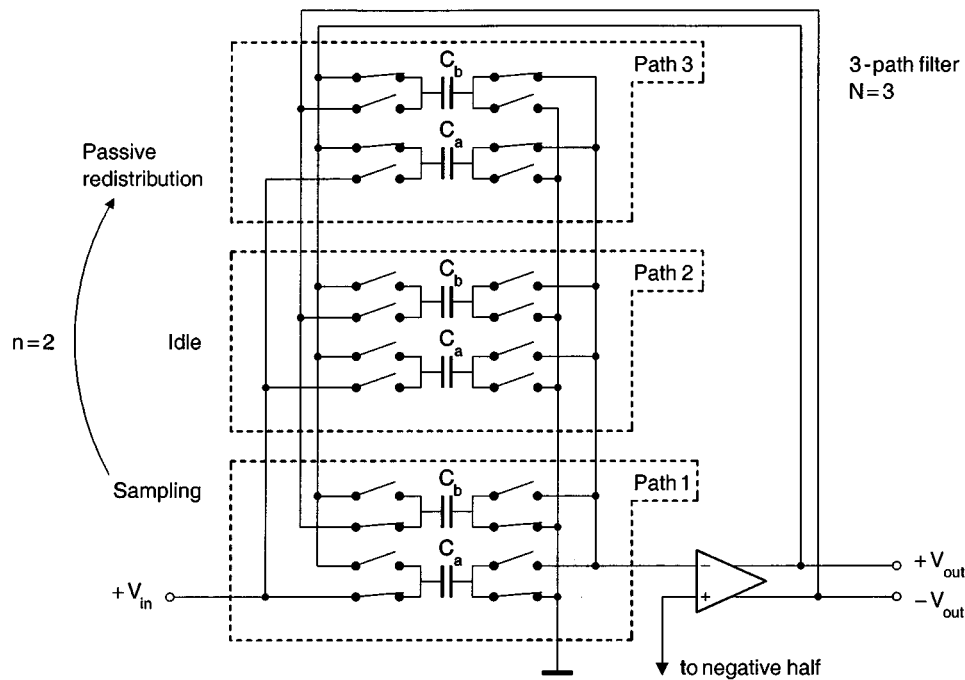


Fig. 7. SC filter circuit design.

from one sample period to the next, Fig. 7 only shows the situation for a specific sampling moment ($t = 0$). This can be compared to phase 1 of Fig. 4.

The input signal is sampled on C_a , while the negative output signal is sampled on C_b . After two sample clock periods (at $t = 2T_s$), the charges on both these capacitors are combined passively by switching both capacitors in parallel. The combined capacitors C_a , C_b are also placed in the feedback loop of an operational transconductance amplifier (OTA) in order to buffer the voltage on these capacitors for read out. The charge on the total capacitance $C_a + C_b$ becomes

$$(C_a + C_b) \times V_{\text{out}}[k] = C_a \times V_{\text{in}}[k-2] - C_b \times V_{\text{out}}[k-2]. \quad (5)$$

The voltage transfer function can be written in the z -domain as

$$\frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = (1 - \beta^2) \times \frac{z^{-2}}{1 + \beta^2 z^{-2}} \quad (6)$$

where

$$\beta^2 = \frac{C_b}{C_a + C_b}. \quad (7)$$

The pole displacement factor β , and hence the Q , is determined by a simple ratio of capacitors C_a , C_b . A Q of 28 per BPF section requires C_b to be 20 times larger than C_a . To make Q less sensitive to process variations, C_b is created from 20 parallel C_a capacitors, each with its own set of switches. A C_a of 140 fF is chosen based principally on kT/C noise considerations.

The BPF presented here is capable of providing a more accurate transfer function than previous N -path filters [5], or parallel switched biquads [6]. This increased accuracy is because 1) delta-charge redistribution is used in which the filter action occurs through the passive redistribution of charge, from which

filter transfer (6) arises, 2) only a single transfer of charge is needed between input and output, making F_o and Q less sensitive to settling inaccuracy, 3) the Q is determined by a simple ratio of capacitors C_a , C_b , making the Q less sensitive to capacitor spreads, and 4) BPF sections can be easily cascaded for increased selectivity while still maintaining low F_o and Q sensitivities.

B. Selectable Gain Control

The BPF section has a nominal 0 dB gain at F_o . It is possible to multiply up the filter gain without the need for an extra amplifier. Instead, one or more C_a capacitors sample the input signal and transfer their charge to output capacitor combination $C_a + C_b$, as shown in Fig. 8. In each BPF section, a gain of 0, 6, or 12 dB can be selected. For the total filter, this means a potential programmable gain of 0 to 36 dB in steps of 6 dB. In order to avoid noise and distortion variations with each gain setting, the impedance seen at the BPF OTA input is not allowed to vary with the gain setting. This is achieved by replacing those C_a capacitors that switch between the input signal and the OTA input with dummy C_a capacitors that switch between the reference voltage and the OTA input. Similarly, the impedance at the output of the stage preceding the filter section is kept constant by maintaining the switching of all the C_a capacitors, even if some of these capacitors are not used for the subsequent gain control.

C. Track-and-Hold

The T&H has been designed for low distortion and low noise. The circuit diagram is shown in Fig. 9. It is again a fully differential three-path construction. Only nMOS switches are used, with the input switches being designed extra large (15/0.6) to reduce sensitivity to channel resistance

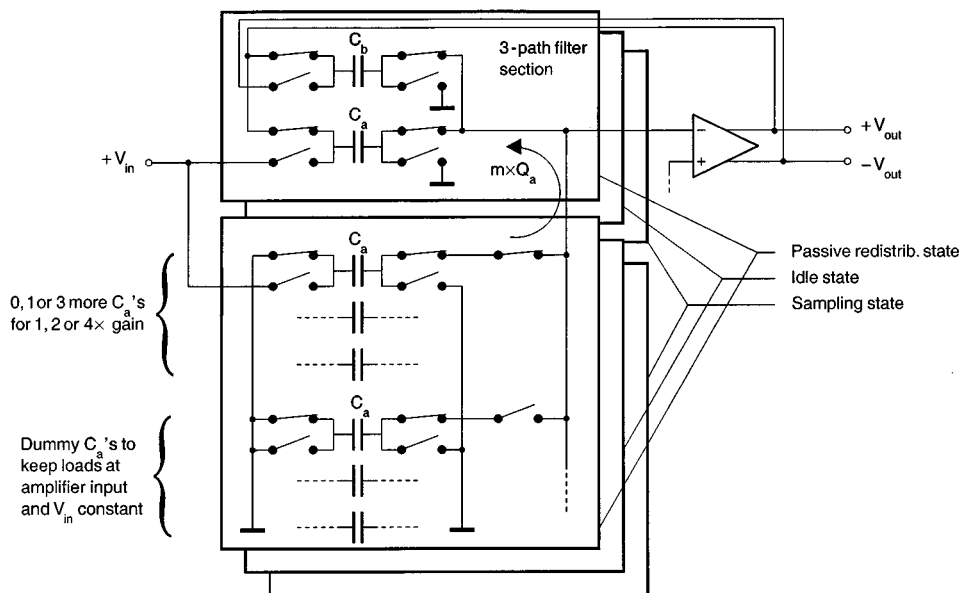


Fig. 8. Selective gain control for IF AGC.

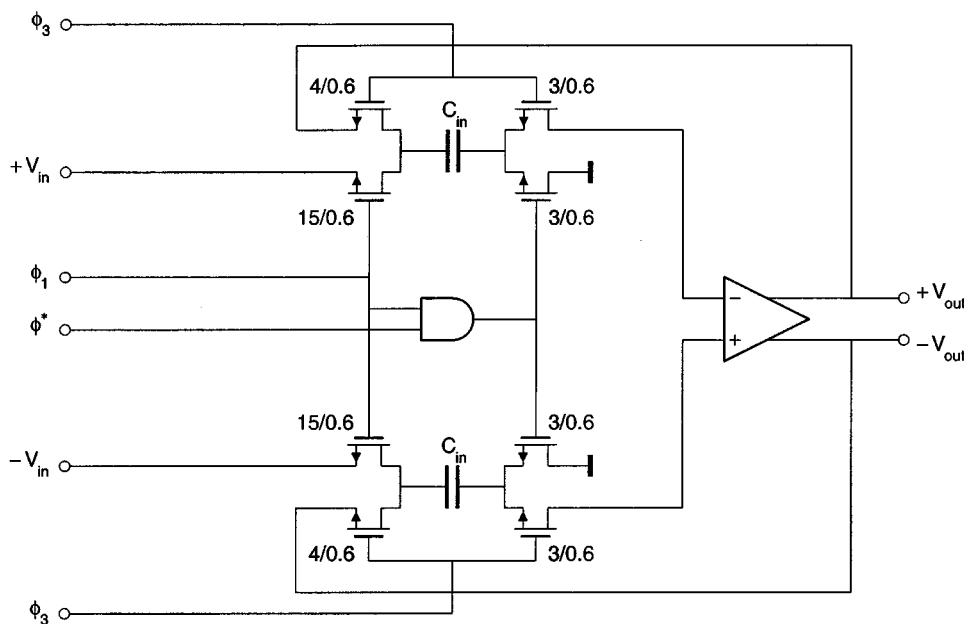


Fig. 9. Track-and-hold.

modulation. Each sampling branch has a small switch (3/0.6) connected to V_{ref} , the turn-off time of which is controlled by a single fast turn-off early clock (ϕ^*) switching at frequency F_s . In this way, clock feedthrough and nonuniform sampling are reduced significantly. In addition, the need for exact phase matching of clocks ϕ_{1-3} is avoided. The noise is kept low by choosing C_s to be 400 fF. Note that the measurement S&H is made in a similar way to the T&H, except that extra OTAs have been placed in parallel in order to drive the chip output capacitance. The S&H design has been optimized to guarantee a good linear settling response under nominal signal conditions. Some slewing cannot be avoided, particularly for large signals ($>0.5 V_{pp}$).

D. Amplifier

A single-stage dual-input telescopic OTA is used to realize all the amplifiers, as depicted in Fig. 10. The nMOS and pMOS input stages are connected together in this design and not separated out as previously [8]. This is because, in this design, with the use of a compact poly-poly capacitor option, the extra routing that would be needed to connect up the split capacitors and switches would take up too much area relative to the area taken up by each capacitor. The dc tail current nMOS transistor to V_{ss} is removed for two reasons. First, a single low V_{ref} of 1 V can be chosen for the input and output sides, meaning small nMOS-only switches can be used with reduced on-resistance modulation and reduced signal dependent clock

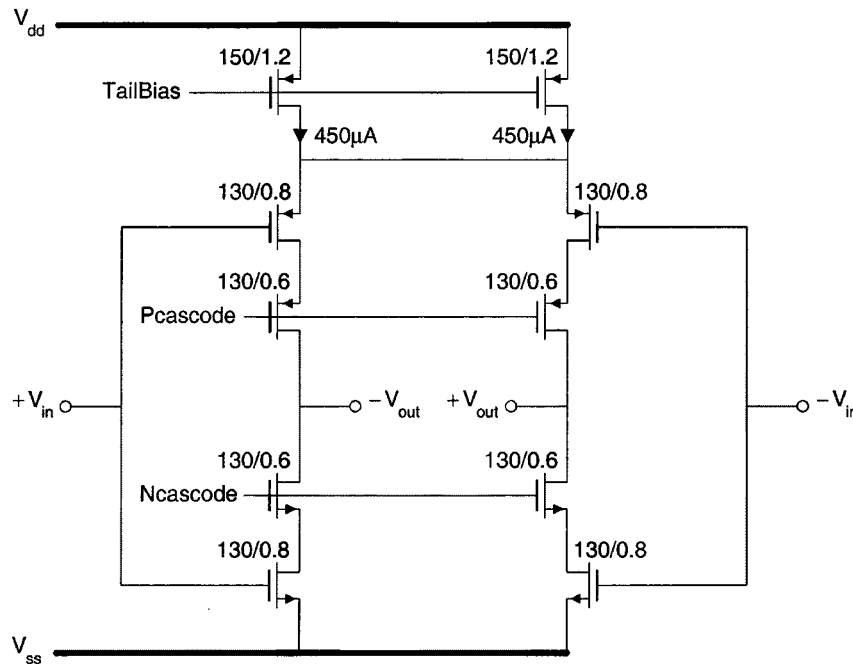


Fig. 10. Dual-input transconductance amplifier.

feedthrough. Second, no separate common-mode feedback (CMFB) circuitry is needed, since the NMOS differential stage has inherent CMFB control [11]. The advantages of this are that the OTA can settle very quickly without being affected by the response of an external CMFB circuit; the power is kept down, since the BPF does not have to drive the extra load capacitors needed to sense the output voltage for a CMFB control circuit, and the dissipation of such extra circuitry is avoided. The maximum output signal swing for proper operation of the OTA, assuming single pMOS and nMOS cascodes, is given by $\pm(V_{DD} - 3V_{DSSP} - 2V_{DSSN})$. The swing becomes severely limited, however, when equal input and output references are chosen. In this case, V_{ref} must be chosen as $V_{TN} + V_{DSSN}$, with V_{TN} and V_{DSSN} the nMOS threshold and saturation voltages, respectively. Now the output swing becomes just $\pm(V_{TN} - V_{DSSN})$, which in the case of the designed OTA is ± 0.6 V. This is adequate, however, for radio IF processing. Furthermore, with a supply of 3.3 V, it is still possible to create a cascoded single-stage amplifier with a dc gain of greater than 1000. Special attention must be paid to the biasing, though, to ensure that all transistors remain optimally biased into saturation (with a nominal V_{DSS} of just under 200 mV), even for varying supply, process, and temperature conditions. The OTA has been simulated to have an open-loop dc gain greater than 61 dB and a GBW greater than 125 MHz for a 3.5-pF differential load.

E. Clock

The clock generator circuitry, shown in Fig. 11, has been placed on-chip together with the SC filter. The reference clock is divided by three, producing three 120° phase-shifted clocks ϕ_{1-3} with 1:2 duty cycles. The early sampling clock ϕ^* always switches off earlier (by about 4 ns) than each of ϕ_{1-3} . The loading and routing of each of the clocks are the same

for good mutual matching. The total clock circuitry, including buffer drivers, consumes only 4.2 mW from a 3.3-V supply.

F. Layout

The SC radio IF filter is integrated using a $0.6\text{-}\mu\text{m}$ double-metal double-poly 5-V analog CMOS technology ($V_{TN0} = 0.75$ V) with high resistance substrate. A chip micrograph can be seen in Fig. 12. The area of the three BPFs, T&H, and clock, is 0.69 mm^2 . Strict matching of the three paths of each BPF section is maintained. The crossing of sensitive nodes (e.g., the OTA inputs) with clock signals is avoided. There are no overlaps between the OTA inputs and outputs, and the analog input signal is kept away from all other signal nodes to avoid crosstalk signal distortion. The clocks in metal-1 are transported over the chip much like coax cables, enclosed by poly and metal-2 layers. Current flow is kept within the cables and not allowed to return via the substrate. In this way, all signal nodes are kept clean of any clock interference.

V. MEASUREMENT RESULTS

All the measurements were carried out with a 3.3-V supply and 42.8-MHz clock. Measured for 25 samples of the same batch, the F_o is 10.6784 MHz (instead of 10.7 MHz) with a 3σ peak-to-peak variation of just $\pm 0.024\%$; the Q is $55.1 \pm 1.0\%$ (3σ). The small shift downwards in center frequency is caused by the limited dc gain of the OTA in combination with the extra input capacitance at its input terminals from all the switched gain control capacitors. The frequency transfers for gain settings of 0 to 36 dB in steps of 6 dB are shown in Fig. 13. The gain deviates no more than 1% from the target value, apart from a fixed attenuation of about 0.6 dB due to settling errors. A zoom-in on the F_o deviation for the 0-dB setting can be seen in Fig. 14. The

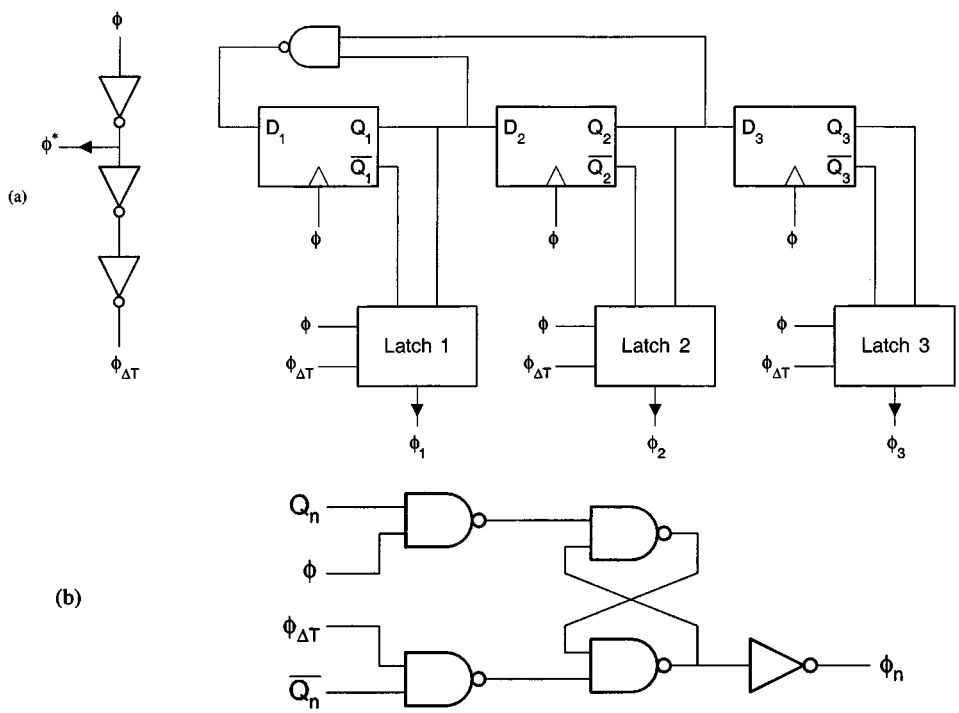


Fig. 11. (a) Clock circuitry. (b) With latch circuit.

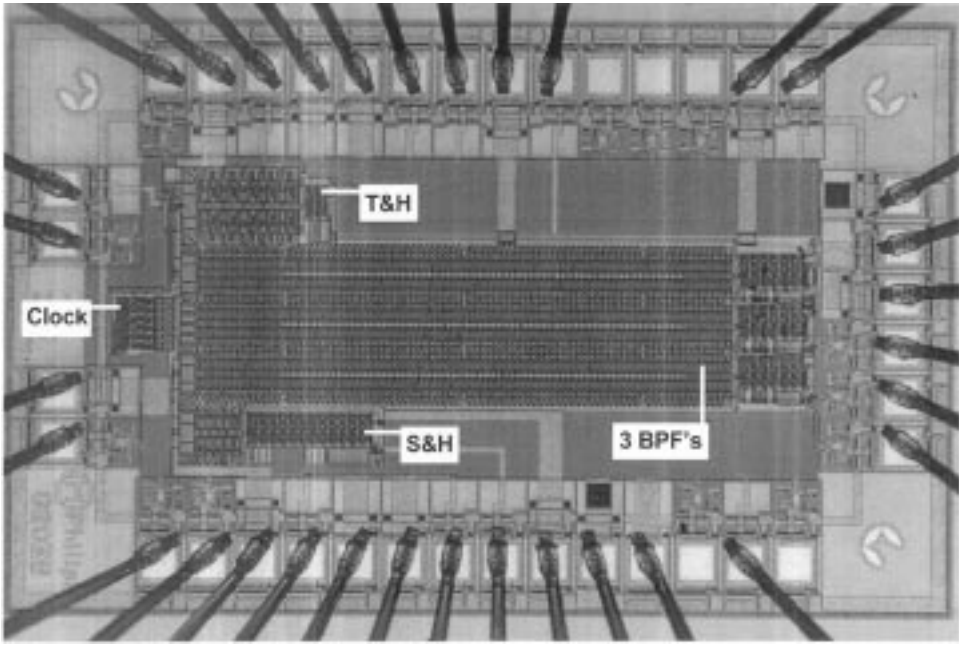


Fig. 12. Chip micrograph of 10.7-MHz SC IF filter.

measured group delay is shown in Fig. 15, where it can be ascertained that the in-band group delay variation is less than $0.5 \mu\text{s}$, meeting the requirements of portable FM radio applications.

In Fig. 16, a plot is given of the measured 1% third-order intermodulation distortion (IM3) for two 0.5-V p-p input signals at frequencies of $F_o \pm 7.5 \text{ kHz}$. The total noise measured at the output is $226 \mu\text{V}_{\text{RMS}}$, resulting in a dynamic range of 58 dB for 1% IM3. It was found that the measurement S&H made a significant contribution to the total distortion. Since the S&H is

not considered part of the application of the IF BPF, as noted in Section II, the dynamic range when corrected for this is greater than 61 dB.

An important item for N -path filters is the matching performance. As this filter is based on a three-path construction, any path mismatch causes $\frac{1}{3}F_s$, or $\frac{4}{3}F_o$, sub-sampling. Components at $\frac{1}{3}F_o$, $\frac{5}{3}F_o$, $\frac{7}{3}F_o$, etc., are mirrored in attenuated form to F_o . A measurement signal at $\frac{1}{3}F_o$ is not a good choice because the third harmonic of the signal generator appears di-

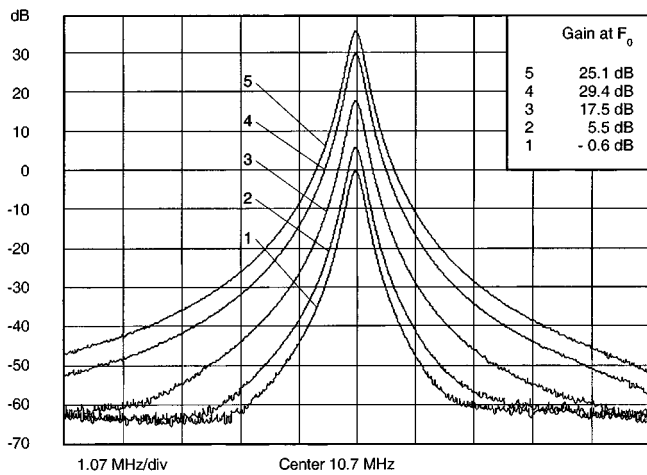


Fig. 13. Filter transfer plots for different gain settings.

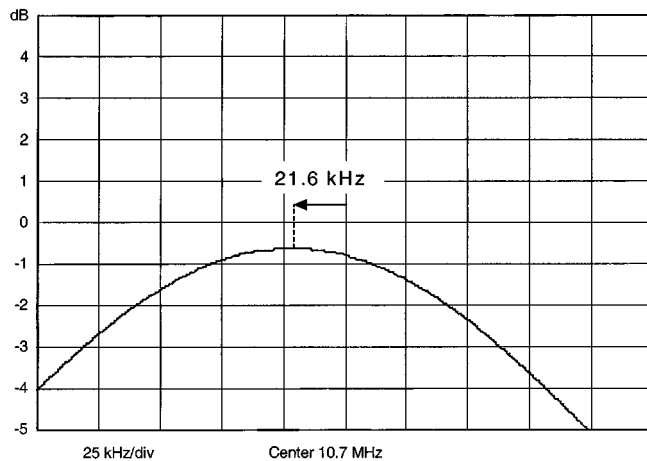
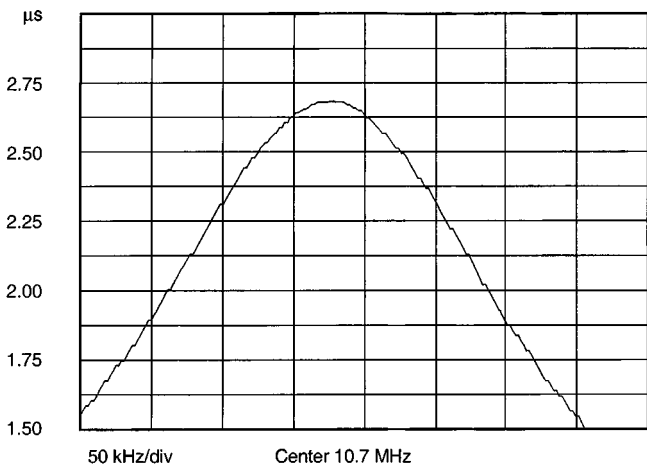
Fig. 14. Measured F_0 deviation from 10.7 MHz.

Fig. 15. Passband group delay characteristic.

rectly at F_0 . For this reason, the next possible frequency is used: $\sqrt[3]{3}F_0$. Fig. 17 shows the combined plot of the input at $\sqrt[3]{3}F_0$ (17.83 MHz) and the output at F_0 (10.7 MHz) for a single measurement. The signal level at F_0 is found to be less than 0.05% of the input level for all 25 samples measured. Another frequency component can be found at $\frac{1}{3}F_s$ (14.27 MHz) and is caused by

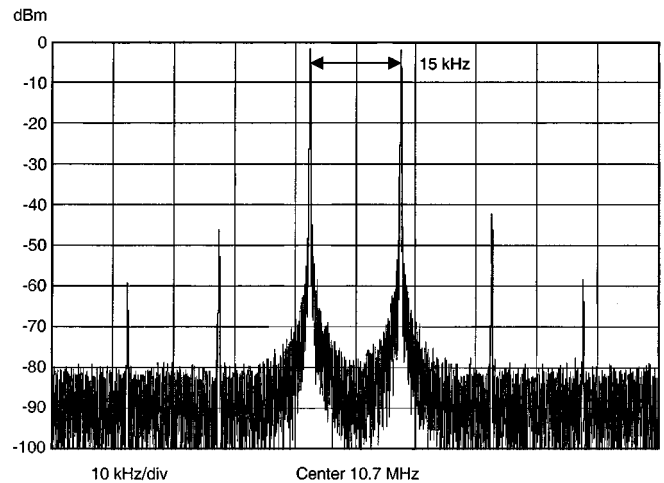
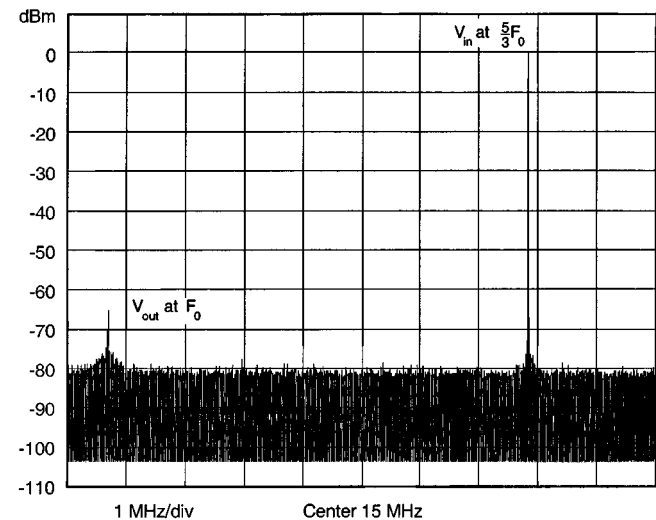


Fig. 16. Measured 1% IM3 for two signals of 0.5 V p-p (including the S&H distortion).

Fig. 17. Path mismatch measurement for F_0 of 10.7 MHz.

a slight timing mismatch between the three clock phases. However, the magnitude is very small ($400 \mu\text{V}_{\text{RMS}}$) and constant and will not be a problem for FM radio. The CMRR has been measured to be more than 55 dB and the PSRR to be more than 29 dB within the passband of the filter.

The total power consumption, including the T&H and clock circuitry, is 16.1 mW, corresponding to a power per pole of just 2.7 mW. All the measurement results are summarized in Table I together with a performance comparison with some previous designs. Note that for the portable radio application intended for this BPF, cost price (circuit area) and power consumption are important design constraints, as discussed in Section II. For these design constraints, the measured dynamic range of 61 dB does not meet the required dynamic range, set at a minimum of 70 dB. One way to improve the signal-to-noise ratio (S/N) for nominal signal levels (0 dB gain setting) is to remove the dummy capacitors at the BPF OTA input (Section IV-B)—this would give a 6 dB improvement in S/N. Furthermore, an increase in S/N can only come at the expense of increased die area and power. For instance, the S/N of the BPF can be increased by

TABLE I
MEASURED FILTER PERFORMANCE AND COMPARISON WITH PREVIOUS SOLUTIONS

	This design	Nagari [2]	Martinez [3]	Song [4]
Technology	0.6 μ m CMOS	1.2 μ m BiCMOS	1.5 μ m CMOS	2.25 μ m CMOS
Filter order	6 (SC)	2 (SC)	4 (CT)	6 (SC)
Center frequency F_0	10.7MHz	10.7MHz	10.7MHz	10.7MHz
F_0 deviation ΔF_0	- 0.2%	- 1%		- 3%
Max. measured F_0 variance	0.024% (3σ)	\pm 0.4%	\pm 1%	\pm 0.4%
Q factor	55	10	36	27
In-band group delay var. $\Delta\tau_g$	0.56 μ s			
Total output noise	226 μ V _{rms}	707 μ V _{rms}	225 μ V _{rms}	1.1mV _{rms}
Dynamic range (1% IM3)	61dB	58dB	68dB	34dB
Supply voltage	3.3V	3V	5V	10V
Power dissipation (w/o clock)	12mW	23mW	220mW	500mW

3 dB for every doubling of the value of the signal capacitors. The $g_{m,s}$ of the BPF OTAs must then also be doubled to maintain the same settling accuracy. This can be done by doubling the area of the input transistors of the OTAs and doubling their current consumption.

VI. SUMMARY

A low-power and very accurate sixth-order SC BPF has been proved feasible in CMOS for 10.7-MHz radio IF selectivity. Through the combination of the N -path technique, orthogonal hardware modulation, and SC delta-charge redistribution, it is possible to design a BPF that is more accurate than ceramic filters for radio applications. In addition, it is possible to combine a selectable gain with each BPF section, in which the total noise and distortion is independent of the gain setting. The high Q (55 at F_0) and center frequency accuracy (F_0 of 10.6784 MHz \pm 0.024%) are not achieved using previous methods for integrated radio IF filters. The complete chip, including clock and T&H, consumes 16 mW at 3.3 V, and this too is much less than recently reported SC and CT IF filters. However, the dynamic range of 61 dB is not yet good enough for portable FM radio applications and needs improving to about 70 dB (at the expense of extra power and die area).

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