A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure

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***Abstract*—This paper presents a low-power 10-bit 50-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) that uses a monotonic capacitor switching procedure. Compared to converters that use the conventional procedure, the average switching energy and total capacitance are reduced by about 81% and 50%, respectively. In the switching procedure, the input common-mode voltage gradually converges to ground. An improved comparator diminishes the signal-dependent offset caused by the input common-mode voltage variation. The prototype was fabricated using 0.13-μm 1P8M CMOS technology. At a 1.2-V supply and 50 MS/s, the ADC achieves an SNDR of 57.0 dB and consumes 0.826 mW, resulting in a figure of merit (FOM) of 29 fJ/conversion-step. The ADC core occupies an active area of only 195 $\times$ 265 μm^2.**

***Index Terms*—Analog-to-digital converter, energy efficient, low power, successive approximation register.**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) require several comparison cycles to complete one conversion, and therefore have limited operational speed. SAR architectures are extensively used in low-power and low-speed (below several MS/s) applications. In recent years, with the feature sizes of CMOS devices scaled down, SAR ADCs have achieved several tens of MS/s to low GS/s sampling rates with 5-bit to 10-bit resolutions [1]–[12].

Although flash and two-step ADCs are preferred solutions for low-resolution high-speed applications, time-interleaved [2]–[9] and multi-bit/step [6] SAR ADC structures have been demonstrated as feasible alternatives. Medium-resolution time-interleaved SAR ADCs suffer from channel mismatch [8]. Interleaved ADCs must use digital calibration or post-processing [9] to achieve sufficient performance. For single-channel architectures, the non-binary [10] and passive charge sharing [11], [12] architectures work at several tens of MS/s and medium resolution (8 to 10 bits) with excellent power efficiency and small area.

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An ADC with a medium sampling rate (a few tens to hundreds of MS/s) and a medium resolution is a necessary building block for 802.11/a/b/g wireless networks and digital TV applications where pipelined ADCs are extensively used. However, the pipelined architecture requires several operational amplifiers, which results in large power dissipation. Moreover, the restrictions for advanced CMOS processes make high performance amplifier design challenging. Drain-induced barrier lowering results in limited gain in short channel devices. Reduced supply voltage also limits the signal swing. With a limited signal swing, the sampling capacitance must be large enough to achieve a high signal-to-noise ratio (SNR), which leads to large current consumption. However, in SAR architectures, no component consumes static power if preamplifiers are not used. A SAR ADC can easily achieve a rail-to-rail signal swing, meaning that a small sampling capacitance is sufficient for a high SNR. The conversion time and power dissipation become smaller with the advancement of CMOS technologies. Since SAR ADCs take advantage of technological progress, for some high-conversion-rate applications, power- and area-efficient SAR ADCs can possibly replace pipelined ADCs in nanometer scaled CMOS processes.

In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator, and capacitive reference DAC network. Digital power consumption becomes lower with the advancement of technology. Technology scaling also improves the speed of digital circuits. On the other hand, the power consumption of the comparator and capacitor network is limited by mismatch and noise. Recently, several energy-efficient switching methods have been proposed to lower the switching energy of the capacitor network. The split capacitor method [4] reduces switching energy by 37%, and the energy-saving method [13] reduces energy consumption by 56%. Although these methods reduce the switching energy of capacitors, they make the SAR control logic more complicated due to the increased number of capacitors and switches, yielding higher digital power consumption.

This paper proposes a capacitor switching method that allows less than 1-mW power consumption for a 10-bit 50-MS/s SAR ADC fabricated using 0.13-μm CMOS technology [1]. The proposed monotonic switching method reduces power consumption by 81% without splitting or adding capacitors and switches. The total capacitance in the DAC capacitor network is reduced by 50%. In addition, the switching method improves the settling speed of the DAC capacitor network. Although the first prototype [1] demonstrated the effectiveness of the monotonic

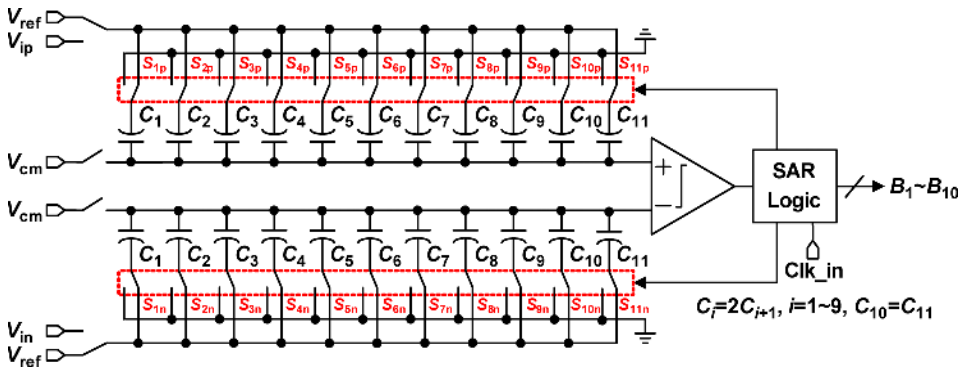

Fig. 1. A conventional 10-bit SAR ADC.

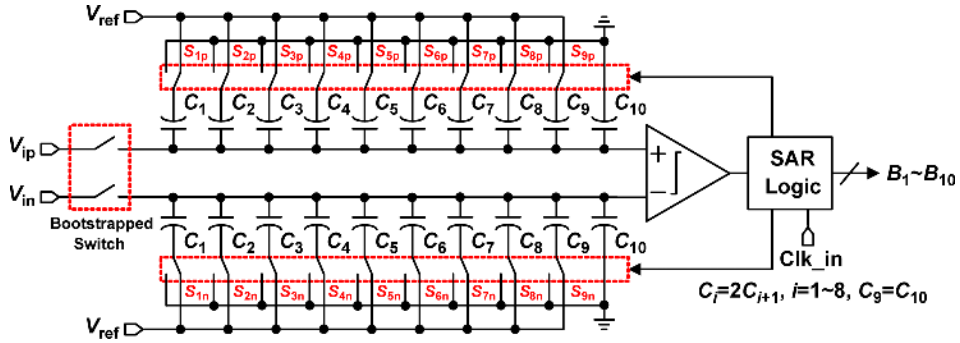

Fig. 2. The proposed SAR ADC architecture.

switching scheme, the signal-dependent offset caused by the variation of the input common-mode voltage degraded ADC linearity. Hence, this paper also presents an improved comparator design to avoid the linearity degradation. The revised prototype has a power efficiency of 29 fJ/conversion-step and occupies an active area of 0.052 mm^2.

The rest of this paper is organized as follows. Section II describes the design concept and architecture of the proposed SAR ADC. Section III presents the implementation of key building blocks. Section IV shows the measurement results. Conclusions are given in Section V.

II. ADC Architecture

To achieve 10-bit accuracy, a fully differential architecture suppresses the substrate and supply noise and has good common-mode noise rejection. SAR ADCs usually use a binary-weighted capacitor array rather than a C-2C capacitor array for better linearity. Fig. 1 shows a conventional 10-bit fully differential SAR ADC. The fundamental building blocks are the comparator, sample-and-hold (S/H) circuit, capacitor network, and successive approximation registers. In this charge-redistribution based architecture, the capacitor network serves as both a S/H circuit and a reference DAC capacitor array. Therefore, this architecture does not require a monolithic S/H circuit. Since this ADC is fully differential, the operation of the two sides is complementary. For simplicity, only the positive side of the ADC operation is described below. At the sampling phase, the bottom plates of the capacitors are charged to $V_{\rm ip}$, and the top plates are reset to the common-mode voltage $V_{\rm cm}$. Next, the largest capacitor C_1 is switched to $V_{\rm ref}$ and the other capacitors are switched to ground. The comparator then performs the first comparison. If $V_{\rm ip}$ is higher than $V_{\rm in}$, the most significant bit (MSB) B_1 is 1. Otherwise, B_1 is 0, and the largest capacitor is reconnected to ground. Then, the second largest capacitor C_2 is switched to $V_{\rm ref}$. The comparator does the comparison again. The ADC repeats this procedure until the least significant bit (LSB) is decided. Although the trial-and-error search procedure is simple and intuitive, it is not an energy efficient switching scheme, especially when unsuccessful trials occur.

Fig. 2 shows the proposed SAR ADC, where the proposed switching procedure can be either upward or downward. For fast reference settling, i.e., discharging through n-type transistors, downward switching was selected in this ADC. The proposed ADC samples the input signal on the top plates via bootstrapped switches, which increases the settling speed and input bandwidth. At the same time, the bottom plates of the capacitors are reset to $V_{\rm ref}$. Next, after the ADC turns off the bootstrapped switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor C_1 on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit

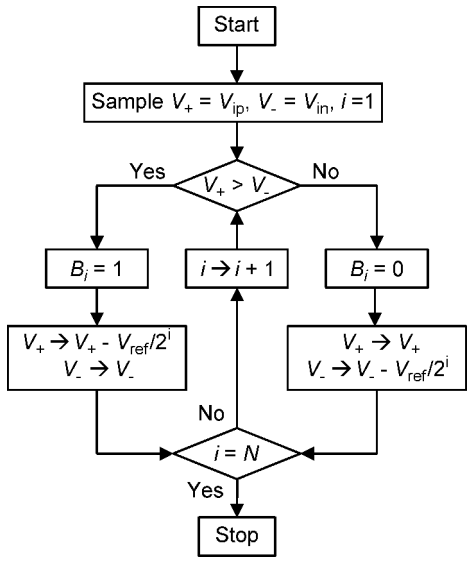

Fig. 3. Flow chart of the proposed ADC.

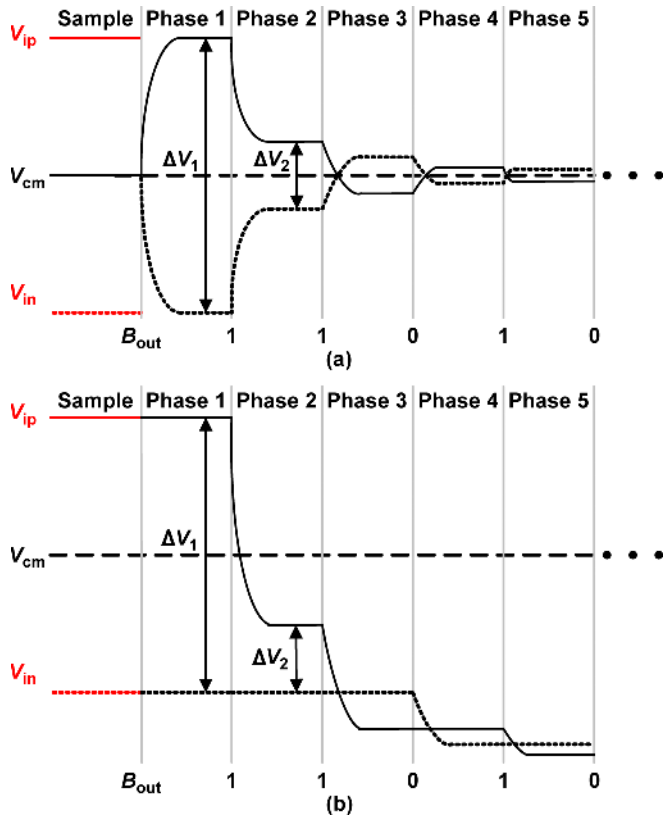

Fig. 4. (a) Waveform of conventional switching procedure. (b) Waveform of monotonic switching procedure.

and switch buffer, resulting in smaller power dissipation. The flow chart of the proposed successive-approximation procedure is shown in Fig. 3.

One of the major differences between the proposed method and the conventional one is that the common-mode voltage of the reference DAC gradually decreases from half $V_{\rm ref}$ to ground as shown in Fig. 4. The proposed switching sequence does not require upward transition. At the same transistor size, the on-resistance of a nMOS switch is only about 1/3 that of a pMOS one. Having no upward transition speeds up the DAC settling. In addition, since sampling is done on the top plate, the comparator can do the first comparison without any capacitor switching. For an n-bit ADC, the number of unit capacitors in a capacitor array is 2^{n-1}, only half that of the conventional one.

Fig. 5 shows 3-bit examples of the conventional and proposed switching methods. The conventional switching method is based on a trial-and-error search procedure. Fig. 5(a) shows all possible conversions. The quantitative energy consumption of each switching phase is also shown in the figure. The conventional switching sequence is efficient when all the attempts are successful, as in the upper cases. However, the switching sequence consumes a lot of energy when attempts are unsuccessful, as in the lower cases. Fig. 5(b) shows all possible switching cases of the proposed method. After the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. Therefore, the proposed switching sequence consumes no energy before the first comparison. In contrast, the conventional sequence consumes $4CV_{\rm ref}^2$ before the first comparison. The subsequent switching sequence of the proposed method is also more efficient than that of the conventional one.

For an n-bit conventional SAR ADC, if each digital output code is equiprobable, the average switching energy can be derived as

$$E_{\rm avg,conv} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1)CV_{\rm ref}^2. \tag{1}$$

The average switching energy for an n-bit SAR ADC using the proposed switching procedure can be derived as

$$E_{\rm avg,mono} = \sum_{i=1}^{n-1} (2^{n-2-i})CV_{\rm ref}^2. \tag{2}$$

For a 10-bit case, the conventional switching procedure consumes 1365.3 $CV_{\rm ref}^2$ while the proposed switching procedure consumes only 255.5 $CV_{\rm ref}^2$. The proposed technique thus requires 81% less switching energy than that of the conventional one. Split capacitor [4] and energy-saving [13] switching methods provide only 37% and 56% reductions, respectively. Fig. 6 shows a comparison of switching energy for the four methods versus the output code. The proposed method has the best power efficiency. Table I summarizes the features of the four methods. The proposed architecture not only has the lowest switching power consumption but also the fewest switches and unit capacitors, which simplifies digital control logic. Therefore, the proposed ADC is very hardware efficient as well.

III. Implementation of Key Building Blocks

The fundamental building blocks of the proposed ADC are a S/H circuit, a dynamic comparator, SAR control logic, and

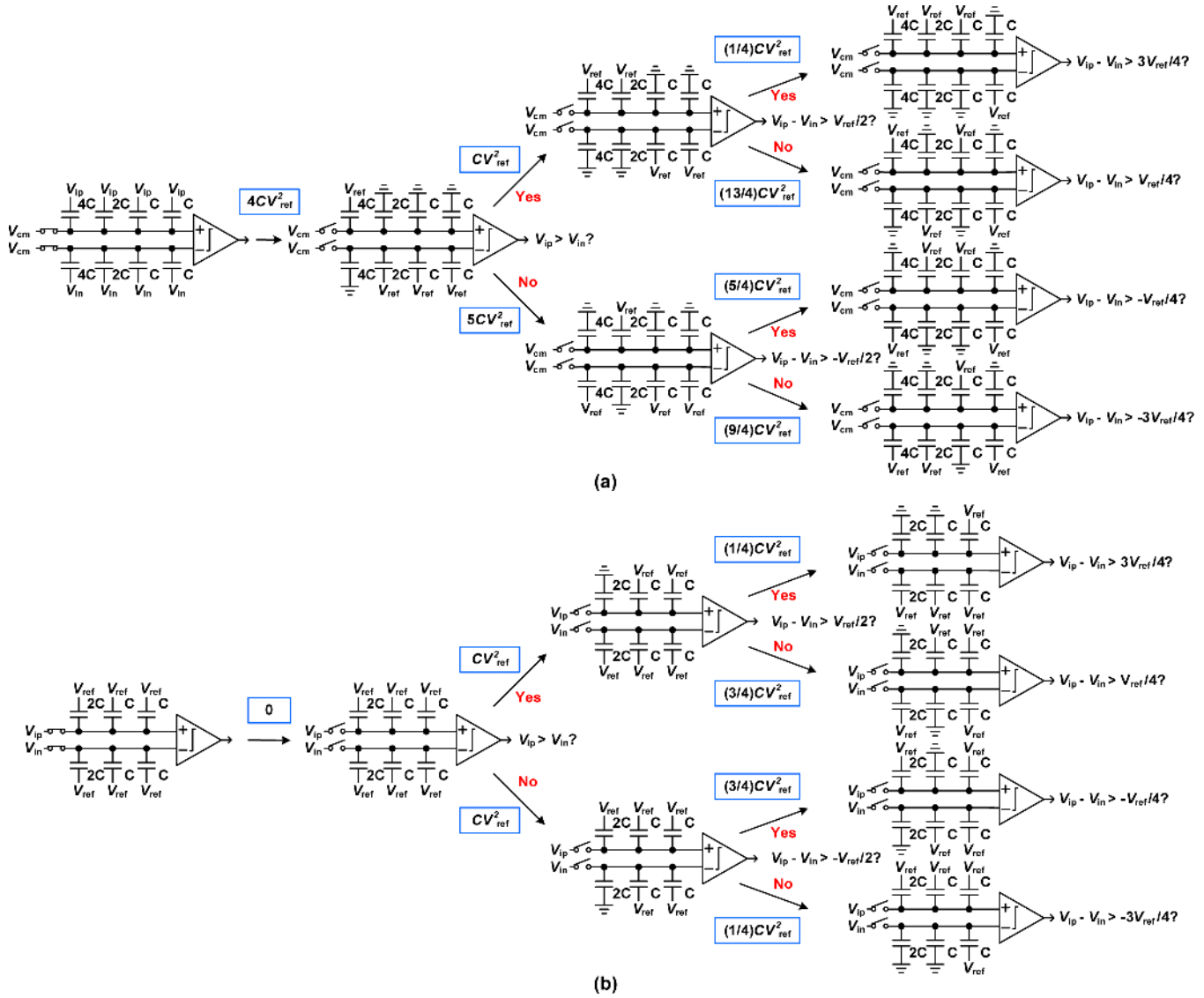

Fig. 5. (a) Conventional switching procedure. (b) Proposed monotonic switching procedure.

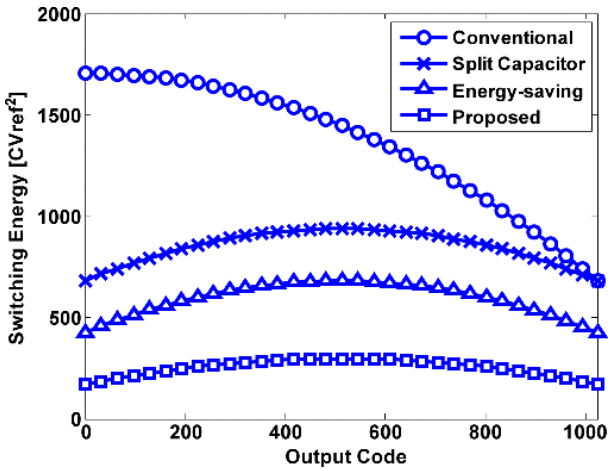

Fig. 6. Switching energy versus output code.

TABLE I
COMPARISON OF SWITCHING PROCEDURES

Switching Procedure	Conventional	Split Capacitor	Energy-saving	Proposed
Normalized Switching Power	1	0.63	0.44	0.19
No. of Switches	$4N+10$	$8N+6$	$8N+2$	$4N$
No. of Capacitors	$2N+2$	$4N$	$4N-2$	$2N$
No. of Unit Capacitors in Capacitor Array	2^N	2^N	2^N	2^{N-1}

a capacitor network. The design considerations of the building blocks are described in the following subsections.

A. S/H Circuit

The bootstrapped switch [14] shown in Fig. 7(a) performs the S/H function. With the bootstrapped switch, the gate-source voltage of the sampling transistor is fixed at the supply voltage

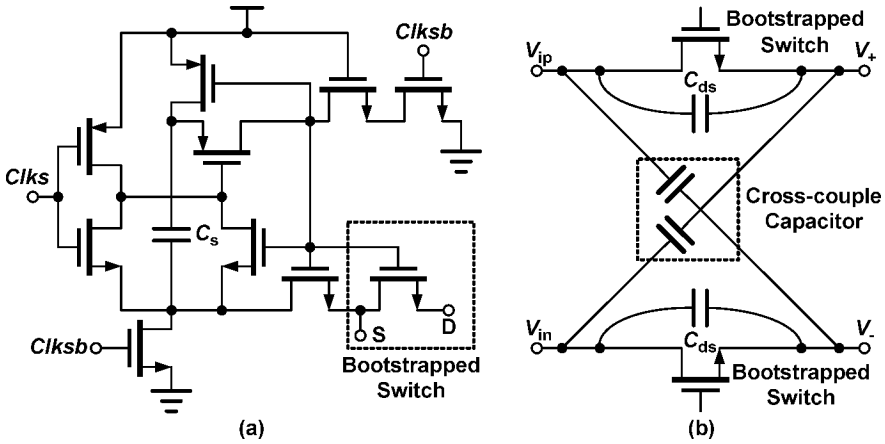

Fig. 7. (a) Bootstrapped switch. (b) Cross-coupled capacitors.

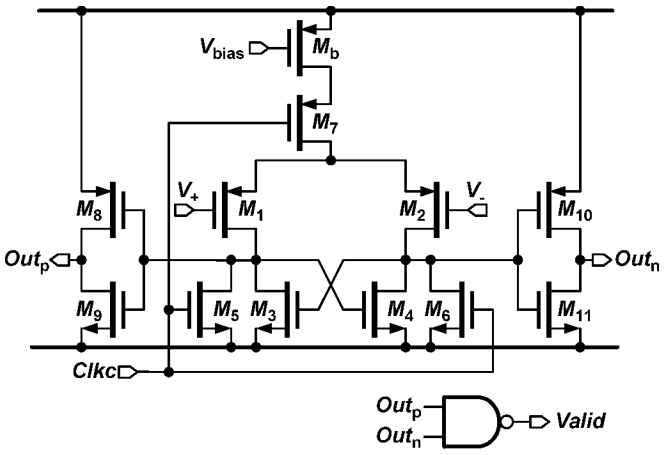

Fig. 8. Dynamic comparator with a current source.

$(V_{\rm DD})$, which makes the on-resistance a small constant value and thus improves the switch linearity. When the bootstrapped switch is off, the input signals couple to the sampling capacitors through the $C_{\rm ds}$ (around 5 fF) which is composed by the drain-source capacitor of the sampling transistor and the routing parasitic capacitance. The coupling effect degrades the high frequency performance because $C_{\rm ds}$ induces unequal charges in the comparison cycles, which results in a dynamic offset. Therefore, two cross-coupled metal-oxide-metal (MOM) capacitors (around 5 fF) are used to neutralize the effect [see Fig. 7(b)]. The two cross-coupled capacitors reduce the coupling effect to less than 1/2 LSB (2.5 fF) in the 10-bit case under processing variation. To achieve higher precision, dummy switches and dummy routing are alternative solutions to reduce the coupling effect.

B. Dynamic Comparator With a Current Source

Fig. 8 shows a schematic of the comparator. During the conversion phase, the input voltages of the comparator approach ground. For proper function within the input common-mode voltage range from half $V_{\rm ref}$ to ground, the comparator uses a p-type input pair. Because a dynamic comparator does not consume static current, it is suitable for energy efficient design.

When $Clkc$ is high, the comparator outputs $Out_{\rm p}$ and $Out_{\rm n}$ are reset to high. When $Clkc$ goes to low, the differential pair, M_1 and M_2, compares the two input voltages. Then, the latch regeneration forces one output to high and the other to low according the comparison result. Consequently, the *Valid* signal is pulled to high to enable the asynchronous control clock. The offset voltage of this comparator can be expressed as [15]

$$V_{\rm os} = \Delta V_{\rm TH1,2} + \frac{(V_{\rm GS}-V_{\rm TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right) \quad (3)$$

where $\Delta V_{\rm TH1,2}$ is the threshold voltage offset of the differential pair M_1 and M_2, $(V_{\rm GS}-V_{\rm TH})_{1,2}$ is the effective voltage of the input pair, $\Delta S_{1,2}$ is the physical dimension mismatch between M_1 and M_2, and ΔR is the loading resistance mismatch induced by M_3–M_6. The first term is a static offset which does not affect the performance of a SAR ADC. However, the second term is a signal-dependent dynamic offset. The effective voltage of the input pair varies with the input common-mode voltage. The dynamic offset degraded the performance of the first prototype [1].

There are several possible approaches to improve the dynamic offset. The comparator size can be enlarged, which results in larger power consumption. The effective voltage of the input pair can be reduced, but this decreases the comparison speed. The error tolerant non-binary search algorithm [10] is also a feasible method. A simple and reliable way is to cascode a biased MOS $(M_{\rm b})$ at the top of the switch MOS, as shown in Fig. 8. Because $M_{\rm b}$ is in the saturation region, the change of its drain-source voltage has only a slight influence on the drain current. Hence, $M_{\rm b}$ keeps the effective voltage of the input pair near a constant value when common-mode voltage changes. The dynamic offset thus has a minor influence on the conversion linearity.

C. SAR Control Logic

To avoid using a high-frequency clock generator, the proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals. Fig. 9 shows a schematic and a timing diagram of the asynchronous control logic. The dynamic comparator generates the *Valid* signal. $Clks$ is the control signal of the sampling switches, it turns on the switches at high potential and turns off the switches at low potential. The sampling phase is about 20% of the whole clock period. $Clkc$ is the control signal of the dynamic comparator. Clk_1 to Clk_{10}

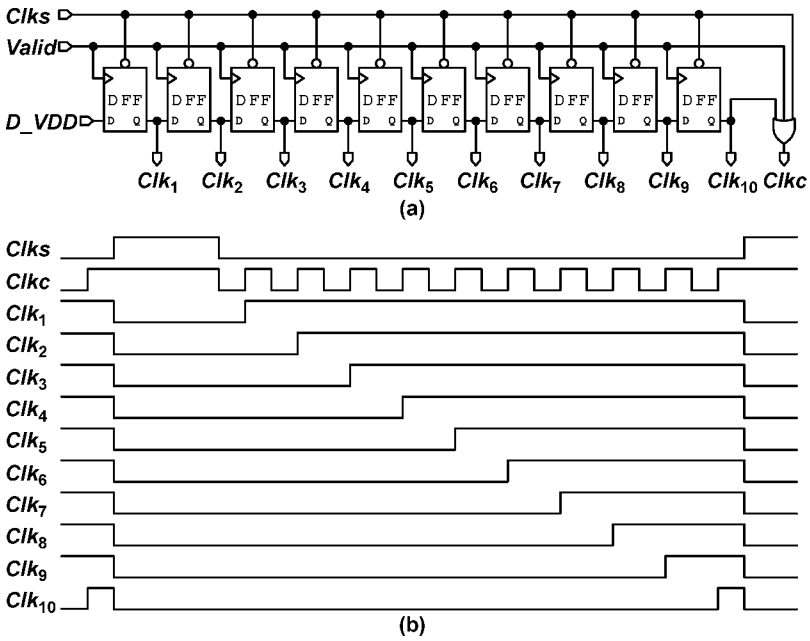

Fig. 9. Asynchronous control logic: (a) Schematic. (b) Timing diagram.

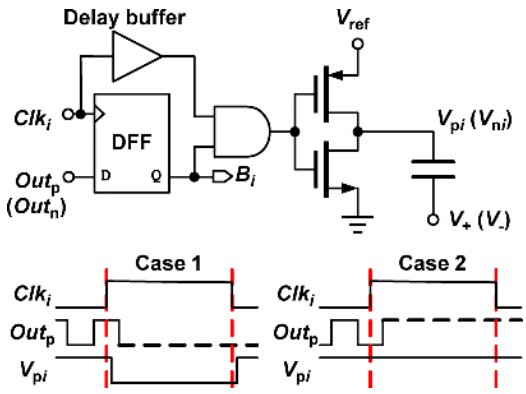

Fig. 10. DAC control logic.

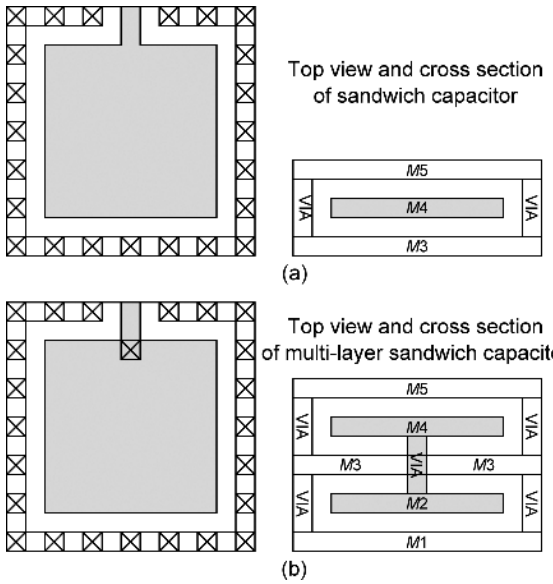

Fig. 11. (a) Sandwich capacitor. (b) Multi-layer sandwich capacitor.

sample the digital output codes of the comparator and serve as control signals for the capacitor arrays to perform the monotonic switching procedure.

Fig. 10 shows a schematic and a timing diagram of the DAC control logic. At the rising edge of Clk_i, a static flip-flop samples the comparator output. If the output is high, the relevant capacitor is switched from $V_{\rm ref}$ to ground. If the output is low, the relevant capacitor is kept connected to $V_{\rm ref}$. At the falling edge of Clk_i, all capacitors are reconnected to $V_{\rm ref}$. The delay buffer guarantees that Clk_i triggers the AND gate after the output of the static flip-flop. This timing arrangement avoids unnecessary transitions. This work uses an inverter as a switch buffer. The conventional architecture in Fig. 1 samples both the input signal and reference voltages on the bottom plates. If the input swing is nearly rail-to-rail, transmission gates are needed to sample input signal. This work uses bootstrapped switches to sample input signal onto top plate of the capacitors and uses inverter buffers to switch between positive and negative voltages. Hence, compared to the conventional architecture, no transmission gates are used, which enables high-speed and low-power operation.

To prevent unnecessary energy consumption and to keep the *RC* value the same, the sizes of the first six switch buffers are scaled down according to the driven capacitances and the buffers of the last three capacitors are unit size ones.

D. Capacitor Array

The first prototype used metal–insulator–metal (MIM) capacitors while the revised one uses metal–oxide–metal (MOM) capacitors to construct the capacitor array. Fig. 11(a) shows a

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D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
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D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	6	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
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D	1	1	1	1	1	1	1	1	2	2	2	2	3	3	4	4	5	10	3	3	2	2	2	2	1	1	1	1	1	1	1	1	D
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Fig. 12. The layout floorplan of the capacitor array.

sandwich capacitor [5], where the gray part is the top plate. The bottom plate encloses the top plate to minimize the parasitic capacitance. The capacitor consists of only three metals, yielding a small capacitance per unit area. For a SAR ADC, capacitors occupy most of the area. Therefore, increasing the unit capacitance greatly improves the area efficiency.

Fig. 11(b) shows a multi-layer sandwich capacitor which doubles the effective capacitor area. The capacitance of a unit multi-layer sandwich capacitor ($3.3\ \mu\text{m} \times 3.3\ \mu\text{m}$) is about 4.8 fF while that of a sandwich capacitor of the same size is only 2.4 fF. Therefore, the multi-layer sandwich capacitor is much more hardware efficient. The binary capacitor array of the proposed 10-bit SAR ADC uses 2^9 unit capacitors. Therefore, the total sampling capacitance of one capacitor network is 2.5 pF. The two capacitor networks occupy a total active area of $195\ \mu\text{m} \times 195\ \mu\text{m}$, about 72% of the whole ADC.

Due to the small unit capacitance, the routing parasitic capacitance has a considerable influence on the ratio of capacitances. The capacitors were placed in an intuitive way to simplify the layout routing. Fig. 12 shows the layout floorplan of the capacitor array.

IV. Measurement Results

The prototype was fabricated using a one-poly–eight-metal (1P8M) 0.13-μm CMOS technology. The full micrograph and the zoomed-in view of the core are shown in Fig. 13. The total area of the chip is 0.93 mm × 1.03 mm, with the ADC core taking up only $195\ \mu\text{m} \times 265\ \mu\text{m}$. The switches for capacitors are placed close to the capacitor arrays. In this improved work, the logic control circuit has been optimized for power consumption and area, and the layout of the digital logic circuit is more compact. Therefore, the core area is smaller than that of the first prototype. An on-chip 100-Ω resistor is placed between the differential input ports to match the 50-Ω resistance of the signal cable. The measurement results of the prototype are presented below.

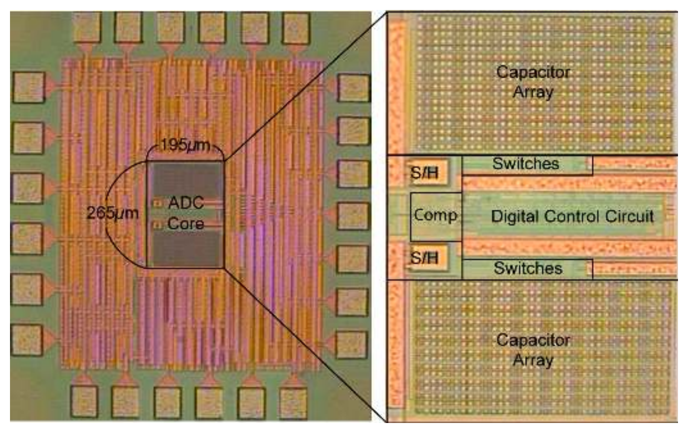

Fig. 13. Die micrograph and the zoomed view.

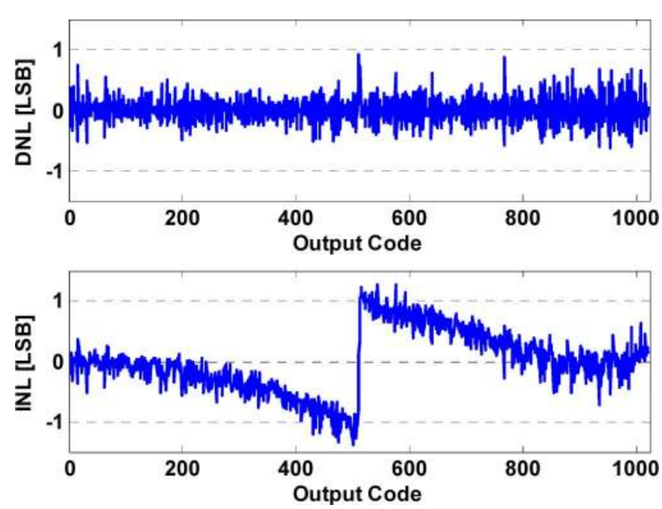

Fig. 14. Measured DNL and INL.

A. Static Performance

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 14. The peak DNL and INL are 0.91/−0.63 LSB and

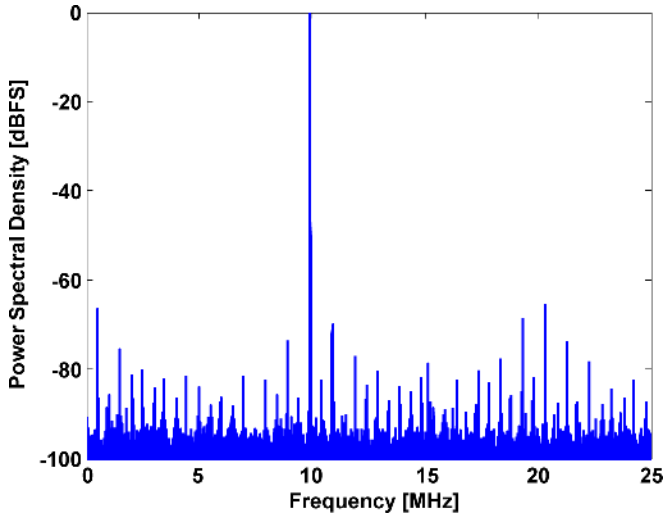

Fig. 15. Measured 32,768-point FFT spectrum at 50 MS/s.

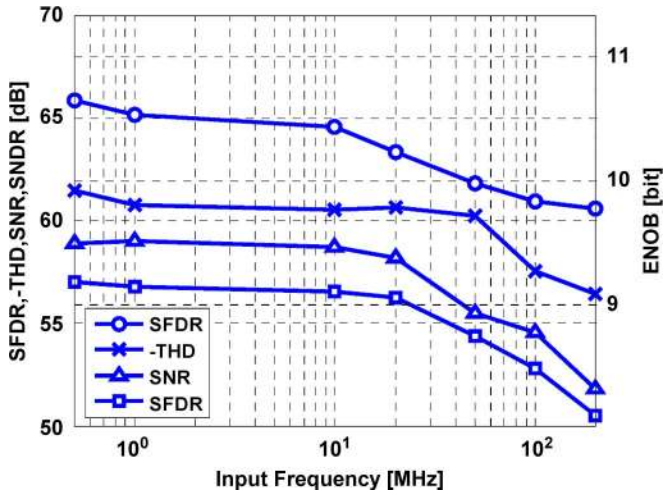

Fig. 16. Measured dynamic performance versus input frequency at 1.2 V and 50 MS/s.

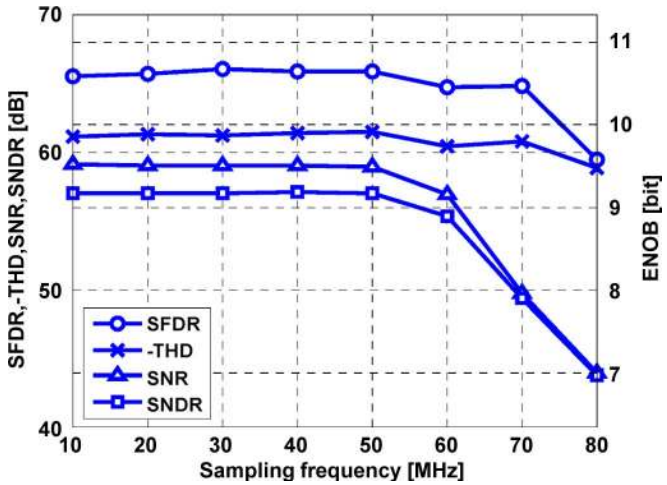

Fig. 17. Measured dynamic performance versus sampling frequency.

TABLE II
SPECIFICATION SUMMARY

Specification (Unit)	Experimental Result
Supply Voltage (V)	1.2
Input CM Voltage (V)	0.6
Input Range (V_{p-p})	2
Sampling Capacitance (pF)	2.5
Sampling Rate (MS/s)	50
Active Area (mm^2)	0.052
DNL (LSB)	0.91 / -0.63
INL (LSB)	1.27 / -1.36
SNDR/SFDR (dB)	57.0 / 65.9 (0.5 MHz)
	56.5 / 64.6 (10 MHz)
	54.4 / 61.8 (50 MHz)
ENOB (bit)	9.18
ERBW (MHz)	50
Power (mW)	0.826

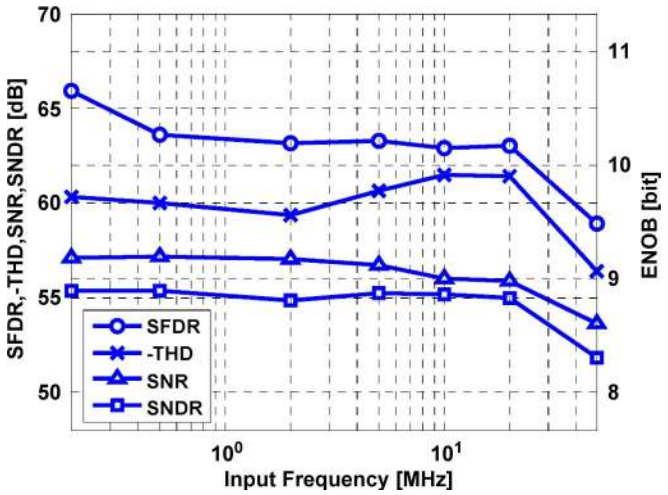

Fig. 18. Measured dynamic performance versus input frequency at 0.6 V and 10 MS/s.

TABLE III
SPECIFICATION SUMMARY AT DIFFERENT SUPPLY VOLTAGES

Specification (Unit)	Experimental Result			
Supply Voltage (V)	1.2	1.0	0.8	0.6
Input CM Voltage (V)	0.6	0.4	0.3	0.2
Input Range (V_{p-p})	2	1.6	1.2	0.8
Sampling Rate (MS/s)	50	40	20	10
ERBW (MHz)	50	50	20	20
ENOB (bit)	9.18	9.15	9.19	8.91
Power (mW)	0.826	0.496	0.154	0.046
FOM (fJ/Conv.-step)	29	22	13	9.6

1.27/−1.36 LSB, respectively. The figure shows that the INL has a jump at the middle of output codes. Since each test chip has this characteristic, the parasitic capacitance induced by the layout routing might be responsible for this inference. The MSB capacitance is around one LSB larger than the expected

TABLE IV
COMPARISON TO STATE-OF-THE-ART WORKS

Specifications	*ISSCC*'07 [11]	*ISSCC*'08 [12]	*VLSI*'08 [17]	*ISSCC*'07 [18]	*ISSCC*'08 [19]	First Prototype	This Work
Architecture	SAR	SAR	Pipelined	Pipelined	Pipelined	SAR	SAR
Technology	90 nm	90 nm	90 nm	90 nm	65 nm	0.13 μm	0.13 μm
Supply Voltage (V)	1	1	1.2	0.8	1.2	1.2	1.2
Sampling Rate (MS/s)	50	40	50	80	100	50	50
Resolution (bit)	9	9	9.4	10	10	10	10
Sampling Capacitance (pF)	10	5	0.09	0.5	0.8	5.12	2.5
ENOB (bit)	7.8	8.56	7.91	8.84	9.5	8.48	9.18
Power (mW)	0.7	0.82	1.44	6.5	4.5	0.92	0.826
FOM (fJ/Conv.-step)	65	54	119	178	62	52	29
Active Area (mm^2)	0.08	0.09	0.123	0.64	0.07	0.075	0.052

value. The performance of the ADC is mainly limited by this deterministic capacitor mismatch.

B. Dynamic Performance

Fig. 15 shows the measured FFT spectrum with an input frequency of close to 10 MHz at a 1.2-V supply and a 50-MS/s sampling rate. The measured SNDR and SFDR are 56.5 dB and 64.6 dB, respectively.

Fig. 16 plots the measured SNDR, SNR, SFDR, THD, and ENOB values versus the input frequency at 50 MS/s. At low input frequency, the measured SNDR and SFDR are 57.0 dB and 65.9 dB, respectively. The resultant ENOB is 9.18 bits. When the input frequency was increased to 50 MHz, the measured SNDR and SFDR were 54.4 dB and 61.8 dB, respectively. The effective resolution bandwidth (ERBW) is higher than 50 MHz.

Fig. 17 shows the measured performance versus the sampling frequency with a 0.5-MHz sinusoidal stimulus. When the sampling rate was 60 MS/s, the ENOB was still close to 9 bits. Further increasing the sampling rate rapidly degraded the performance because the conversion time was insufficient.

C. Power Consumption

At a 1.2-V supply, the analog part, including the S/H circuit and comparator, consumes 0.276 mW, and the digital control logic draws 0.42 mW. The ideal power consumption of the reference voltage $V_{\rm ref}$ is

$$P(V_{\rm ref}) = \frac{E_{{\rm avg},n{\rm bit}}}{T} = f \bullet \sum_{i=1}^{n-1} (2^{n-2-i}) C V_{\rm ref}^2. \qquad (4)$$

At a 1-V reference voltage, a 50-MS/s sampling rate, and a 4.8-fF unit capacitance, the expected power consumption is 0.062 mW. The measured value was 0.13 mW because the switch buffers consume dynamic current during transitions. The parasitic capacitors at the bottom plate and the drains of the switch MOS transistors also increase power consumption. Excluding the output buffers, the total power consumption of the active circuit is 0.826 mW. A summary of the ADC is listed in Table II.

D. Low Supply Voltage Performance

Because the ADC has no transmission gates or preamplifiers, it can operate at low supply voltage conditions. At 40 MS/s and a 1-V supply, the low frequency ENOB is 9.15 bits and the ERBW is around 50 MHz. At 20 MS/s and a 0.8-V supply, the low frequency ENOB is 9.19 bits and the ERBW is around 20 MHz. When the sampling rate and supply voltage were decreased to 10 MS/s and 0.6 V, respectively, the low frequency ENOB and ERBW were 8.91 bits and 20 MHz. Fig. 18 plots the performance versus input frequency at 0.6 V. Table III shows a performance summary for various supply voltages. The excellent low-voltage performance demonstrates that the proposed ADC is a feasible alternative to switched-operational-amplifier pipelined ADCs [16].

E. Comparison and Discussion

To compare the proposed ADC to other works with different sampling rates and resolutions, the well-known figure-of-merit (FOM) equation is used.

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min\{2 \times \text{ERBW}, \text{f}_\text{s}\}}. \qquad (5)$$

The FOM of the proposed ADC is 29 fJ/conversion-step at 50 MS/s and a 1.2-V supply. The FOM is 9.6 fJ/conversion-step when the sampling rate and supply voltage are 10 MS/s and 0.6 V, respectively. Table IV compares the proposed ADC with other state-of-the-art ADCs [11], [12], [17]–[19]. Although the proposed ADC was fabricated using older technology, it still has the lowest FOM and smallest active area compared to those of ADCs with similar sampling rates and resolutions.

V. CONCLUSION

In this paper, an efficient capacitor switching procedure for SAR ADCs was presented. The proposed switching procedure leads to both lower switching energy and smaller total capacitance. It also simplifies the digital logic control circuit. The biased comparator reduces the dynamic offset induced by input common-mode voltage variation. The prototype achieves a 50-MS/s operation speed with power consumption of less than

1 mW. It has a FOM of 29 fJ/conversion-step and occupies an active area of only 0.052 mm^2. The experiment results demonstrate the power and hardware efficiency and also the high-speed potential of the proposed SAR ADC.

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