

A 10-bit DC-20 GHz Multiple-Return-to-Zero DAC with
>48 dB SFDR

Dissertation

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Abstract

Recent trends in 5G and radar systems have revealed the need for high-frequency DACs with minimal spurious emissions. Amplitude and timing errors in the DAC have proven to be a significant hindrance to linearity performance and have an increasing impact with frequency. Primary contributors to these errors are impedance mismatches in the current combining network as well as device mismatches.

This work presents a frequency-domain approach to SFDR analysis in which the contribution of each individual cell on the output spectrum is analyzed and errors are applied as transfer functions in the frequency domain. Using this method, static amplitude and timing errors can be examined through a Monte Carlo (MC) analysis using only numerical computation, thus eliminating the need to run a transient simulation for each MC sample. Moreover, unlike the conventional analysis, the frequency-domain approach is amenable to the small-signal models produced by EM simulations, enabling the incorporation of complex output summing node structures with little impact to simulation time and convergence.

The frequency-domain analysis is used to produce a 10-bit 3.35 GS/s MRZ DAC capable of synthesizing frequencies from DC to 20 GHz with greater than 48 dB SFDR. The design includes a vertically-stacked tree (VST) interconnect structure that minimizes attenuation and phase mismatches in the output summing node. Additionally,

a per-cell timing adjustment circuit is proposed, which, along with static current calibration, is used to minimize the remaining errors. Measurement results show that the calibration provides up to 7 dB improvement in SFDR at 20 GHz. The combination of the VST and calibration techniques yield the highest reported SFDR at 20 GHz, while synthesizing the highest instantaneous bandwidth among RF DACs.

For Alicia, Mom, and Dad

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Chapter 1: Introduction

Recent years have seen an extreme growth in the complexity and capabilities of communications and radar systems. The ever-increasing bandwidth demands of communications systems will soon require clever techniques for operation within the increasingly crowded frequency spectrum. Similarly, the desire for radar systems capable of reliable operation in any environment is growing. A promising solution to both of these application spaces is the cognitive radio which brings about several new and interesting design challenges which must be tackled to enable the wireless systems of the future.

1.1 Motivation: The Cognitive Radio

The cognitive radio, illustrated in Figure 1.1, is a key enabling technology for future wireless systems [1]. The architecture comprises a receiver for spectrum sensing followed by digital processing and a reconfigurable transmitter, dubbed the software-defined radio (SDR). Cognitive radios enable a new class of wireless systems that sense and respond to the environment to achieve optimum performance. The potential applications to 5G communications [2] and advanced radar systems [3] have made the cognitive radio a highly coveted technology.

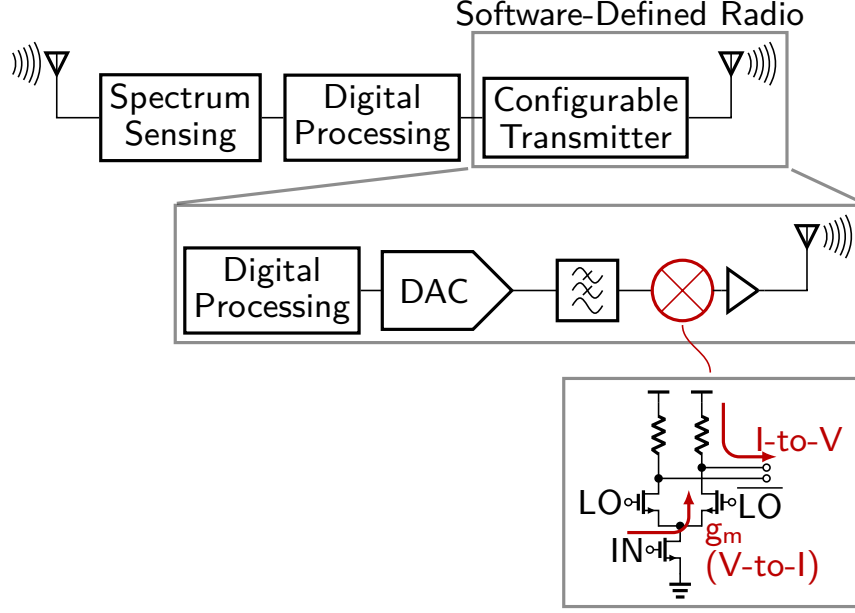


Figure 1.1: Block diagram of the cognitive radio

1.2 The Ideal: Software-Defined Radio

A key component of the cognitive radio is the software-defined radio (SDR); a fully reconfigurable transmitter capable of operation over GHz of bandwidth. Conventionally, a direct-conversion architecture is used to implement the SDR as shown in Figure 1.1. Although this direct conversion approach can produce high frequency signals, the challenges of linearizing the mixer g_m stage over a large instantaneous bandwidth relegate its use to narrowband systems [4]. To widen the bandwidth, direct radio-frequency (RF) synthesis, illustrated in Figure 1.2, has been proposed which removes the mixer from the system [5]. Unfortunately the DAC in the direct RF approach must simultaneously achieve high output frequency, high linearity, and

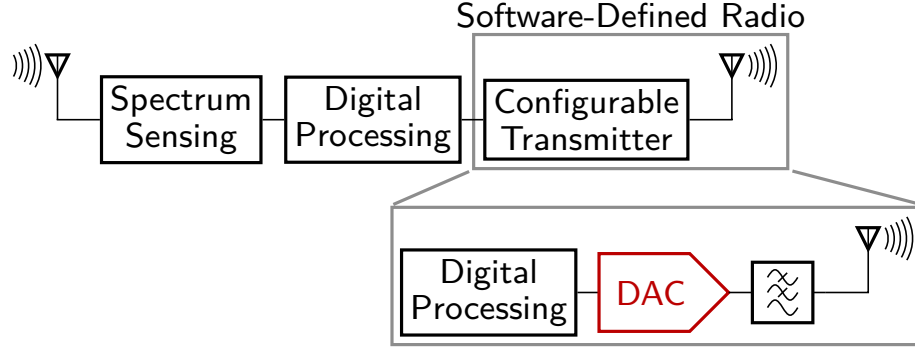


Figure 1.2: Block diagram of the cognitive and software-defined radio with an RF DAC

high output power; three conflicting tradeoffs that place this system out of the reach of current state-of-the-art technology for wireless systems in the GHz range.

1.3 An Initial Step: Radio-Frequency DACs

To alleviate some of the extreme requirements that the ideal SDR places on the DAC, this work pursues a more feasible architecture which utilizes a radio-frequency (RF) DAC. The RF DAC incorporates an up-conversion of the signal, allowing for a reduced sample rate that makes the linearity requirements easier to reach. Additionally, the architecture includes a power amplifier, alleviating the output power requirements for the RF DAC. By reducing the sample rate and output power requirements, the RF DAC brings the cognitive radio within reach of state-of-the-art technology. While the design of any DAC presents a multitude of mixed-signal design complications, the foray into gigahertz and mm-wave frequencies introduces unique and daunting challenges. In order to successfully navigate this broadening design

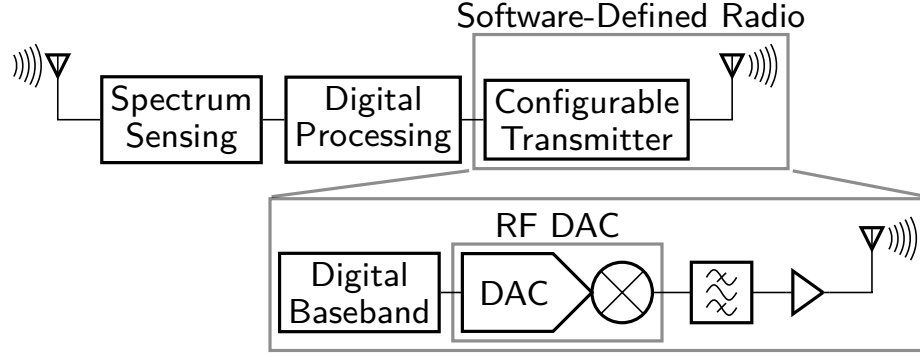


Figure 1.3: Block diagram of the cognitive and software-defined radio with an RF DAC

space, new analysis, simulation, and design techniques are vital to meet the demand of future wireless systems.

1.4 Dissertation Outline

This research develops novel analysis and design techniques to minimize the spurious emissions of an RF DAC for use in an SDR system. Chapter 2 introduces the challenges of DAC design at GHz and mm-wave frequencies. Chapter 3 discusses a frequency-domain SFDR analysis that allows for the quick and accurate prediction of SFDR and uniquely enables the inclusion of electromagnetic simulations which are becoming increasingly critical to the design process as frequencies approach the GHz and mm-wave domain. Chapter 4 details a DC-20GHz DAC which uses an improved output summing and timing calibration circuitry to achieve state-of-the-art linearity. Finally, Chapter 5 discusses the critical pathways for future research and provides concluding remarks.

Chapter 2: High-Frequency DAC Challenges

As DACs take over larger portions of the transmit chain, their spectral emissions become a primary concern. The output spectrum of a DAC, illustrated in Figure 2.1, contains the desired signal, f_1 , along with image replicas that repeat every $f_s/2$ in accordance with the Shannon-Nyquist theorem. In the presence of circuit nonidealities, harmonically-related spurs can also arise at the output. Because the spurs are within the same Nyquist-zone as the signal, they can not be filtered out with the image replicas. Thus, the design of the DAC should minimize such nonidealities to avoid excessive spurious emissions.

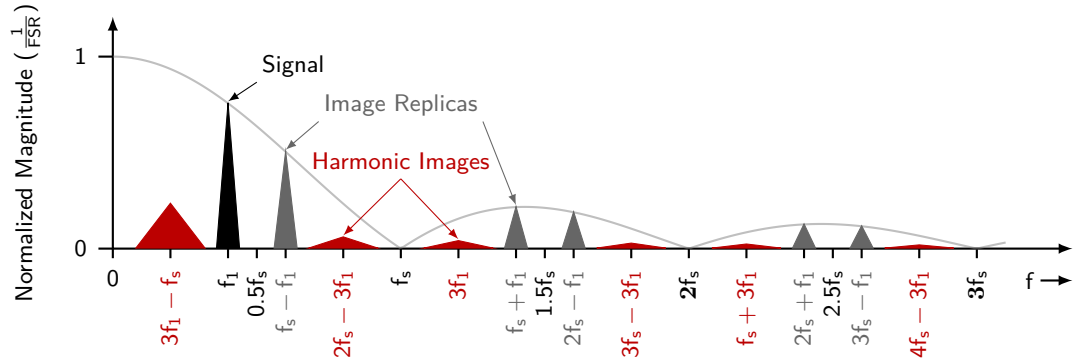


Figure 2.1: DAC output spectrum with nonlinearities

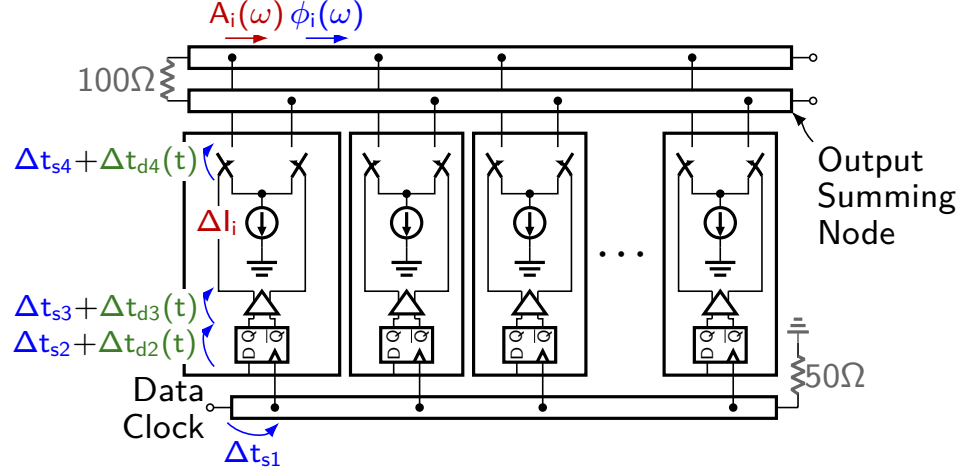


Figure 2.2: A non-return-to-zero current-steering DAC with a tapped transmission line summing node

2.1 The Non-Return-to-Zero Current-Steering DAC

Recently reported GHz and mm-wave DACs exclusively use the current-steering architecture shown in Figure 2.2. The DAC comprises an array of switched current cells which direct current to and from the output node. Typically, each cell includes a retiming flip-flop which synchronizes the data to a common data clock. The output current of each cell is combined via the output summing node. The current-mode operation of this architecture lends itself to fast switching enabling higher sampling rates than the alternative R-2R or switched-capacitor DACs.

2.2 DAC Nonidealities

Figure 2.3(a) shows a simple model of a binary DAC with nonidealities. The DAC data is separated into individual bits, D_i , with each bit receiving a binary scale. Each bit, then has a unique amplitude (α) and timing (τ) error applied before being

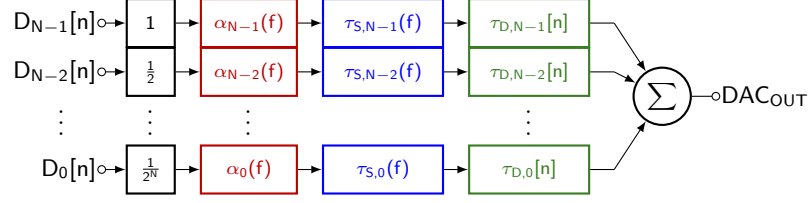


Figure 2.3: A simple model of DAC nonidealities

summed to produce the output. While the amplitude error is frequency-dependent, the timing error is separated into static ($\tau_{S,i}(f)$) and data-dependent ($\tau_{D,i}[n]$) components.

In a current-steering DAC, shown in Figure 2.2, the SFDR performance depends on the precise matching of amplitude and timing between each current cell across frequency [6]. While amplitude errors such as current mismatch (ΔI_i) limit the low frequency SFDR, timing errors have an increasing impact with frequency as they consume a growing portion of the clock period. Static time errors are time-invariant and are caused by mismatches in clock routing (Δt_{s1}), clock-to-Q and propagation delay (Δt_{s2} , Δt_{s3}), and switching speed (Δt_{s4}) [6]. Dynamic time errors vary over each clock period and are caused by deterministic jitter in the data path (Δt_{d2} , Δt_{d3}) as well as data-dependent offset in the switches caused by fluctuations in the common source node (Δt_{d4}) [6, 7].

The difficulty of high-frequency DAC design generally lies with timing errors which arise during any time the output is switching from one value to another. As the clock frequency increases, these transitions occur more often, resulting in a larger contribution to nonlinearities. Data-dependent timing errors are particularly concerning as

they can not be easily compensated, however several DAC architectures have been proposed in the literature in which that issue is specifically addressed.

As frequencies approach the GHz and mm-wave domains the output summing node also plays a critical role in SFDR performance. A common approach to the summing node for mm-wave operation is the tapped transmission line (TTL), shown in Figure 2.2, in which a transmission line is used to carry the current from each cell to the output. The distributed capacitance presented by the current cells can be incorporated into the transmission line, allowing for a well-controlled mm-wave environment with minimal reflections. However, as shown in Section 3.2, the mismatches in attenuation ($A_i(\omega)$) and phase shift ($\phi_i(\omega)$) for each cell result in severe degradation of SFDR. In contrast to static current mismatch, the amplitude errors caused by the output summing node vary with frequency, which, along with the additional phase shift, exacerbates linearity degradation at high frequency. Characterization of errors in the summing node is especially challenging as the wavelength of operation approaches the physical dimensions of the DAC where inductance and transmission line effects begin to dominate the linearity performance. Although these effects can be analyzed using electromagnetic (EM) simulations, the measurement of SFDR typically requires a time-domain simulation in which EM models are impractically slow or even fail to converge.

2.3 Conventional SFDR Analysis

In order to ensure post-fabrication performance, the DAC nonidealities must be carefully accounted for in simulations during the design phase. The conventional SFDR analysis, illustrated in Figure 2.4, begins with a transient simulation of the

N-bit DAC with input data ($b_i, i = 0 \dots N$) to produce a single tone. The simulation captures N_D clock cycles with an oversampling ratio, OSR. The time-domain waveform is then converted into the frequency domain via a numerical computation of the fast Fourier transform (FFT) with a length of $N_{\text{fft}} = N_D \cdot \text{OSR}$. The SFDR is obtained from the ratio of the signal to the largest spur in the resulting output spectrum. A fundamental drawback to this approach is the lengthy transient simulation required to achieve an accurate prediction of SFDR. The stop time of the transient simulation, which is proportional to N_D , determines the frequency resolution of the FFT. It must be chosen such that the noise spectral density is below the power of the largest spur, and that multiple spurs in close proximity can be resolved separately. Figure 2.5(a) shows the impact of N_D on the SFDR measurement of a 10-bit behavioral DAC model, indicating that $N_D \geq 512$ is necessary to predict SFDR within 0.5 dB. Moreover, due to its sampled nature, the DAC produces spurious content at all frequencies. Therefore, the output of the DAC must be sampled at a sufficiently high frequency (by increasing OSR) to ensure that the power of the high-frequency content that is inevitably aliased into the bandwidth of interest is negligible. As shown in Figure 2.5(b), $\text{OSR} \geq 128$ is required to predict SFDR within 0.5 dB.

The long transient simulation is especially troublesome for the analysis of random amplitude and timing errors due to process mismatch which is typically accomplished via Monte Carlo (MC) simulation. To estimate the 99.7% yield with just a 75% confidence [8], more than 10^3 transient simulations are required, drastically increasing the length of the design cycle. Moreover, to accurately predict dynamic time errors, the transient simulation must fully account for layout parasitics in the design, resulting in larger netlists and additional increases simulation time.

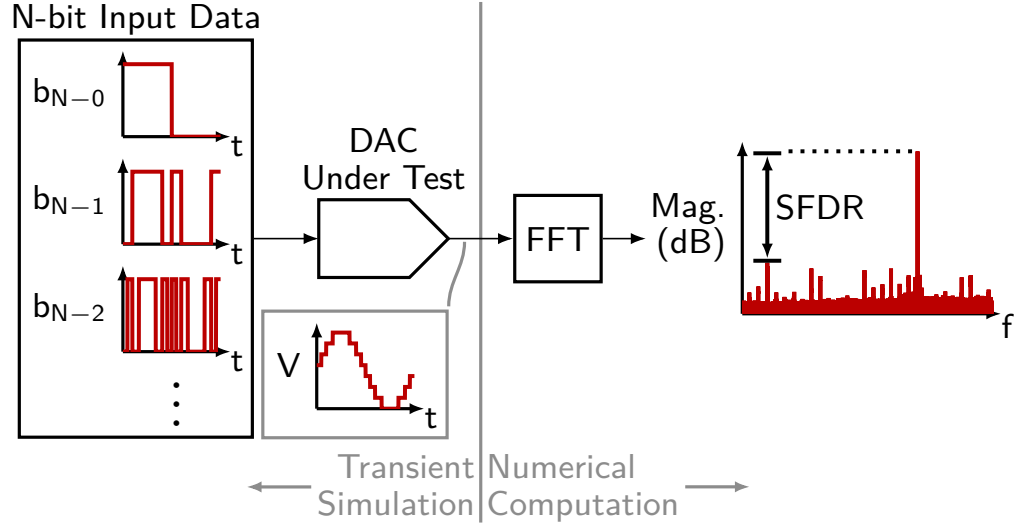


Figure 2.4: Diagram of the conventional SFDR analysis flow.

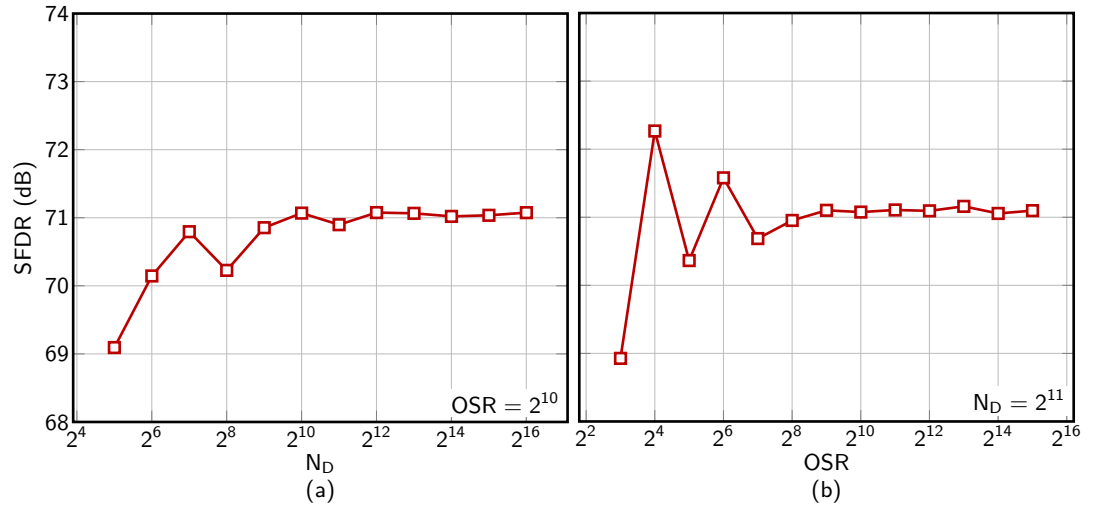


Figure 2.5: The effect of (a) N_D and (b) OSR on the accuracy of the conventional SFDR analysis.

In addition to random process mismatches, the designer must carefully account for deterministic errors in the physical layout of the DAC. EM simulations in particular, especially for the output summing node, are critical to SFDR prediction at GHz and mm-wave frequencies. Figure 2.6 shows the simulated SFDR for a 10-bit DAC with three output summing node models: 1) ideal, 2) resistor and capacitor parasitic extracted, and 3) EM simulated. While the RC extracted model indicates a 10 dB degradation in SFDR due to the summing node, the EM model predicts a 50 dB difference. This disparity is caused by the inclusion of inductance effects in the summing node which are only captured in the EM model.

Although the inclusion of an EM model is absolutely necessary to accurately predict the SFDR of the DAC, inclusion of such a model into the transient simulation required for SFDR analysis is no easy task. To demonstrate the challenge of incorporating an EM model in the conventional SFDR analysis, Figure 2.7 shows the simulation time for the simulations of Figure 2.6. While the inclusion of the RC extracted model increases simulation time by about 24%, the EM model adds nearly two orders of magnitude. It is worth noting that a very simple EM model of the tapped transmission line structure was used to produce Figure 2.7 in order to avoid convergence issues. More complex structures, such as the VST introduced in Section 4.2.2, fail to converge in this testbench.

Excessively long simulation times can be alleviated through the use of analytical models to quickly ascertain linearity performance without a transient simulation. Early work on the analysis of quantized signals [9, 10] developed close form expressions for the output spectrum, however only the effect of ideal quantization is considered, thus neglecting many error sources that arise within the DAC. Theoretical analyses

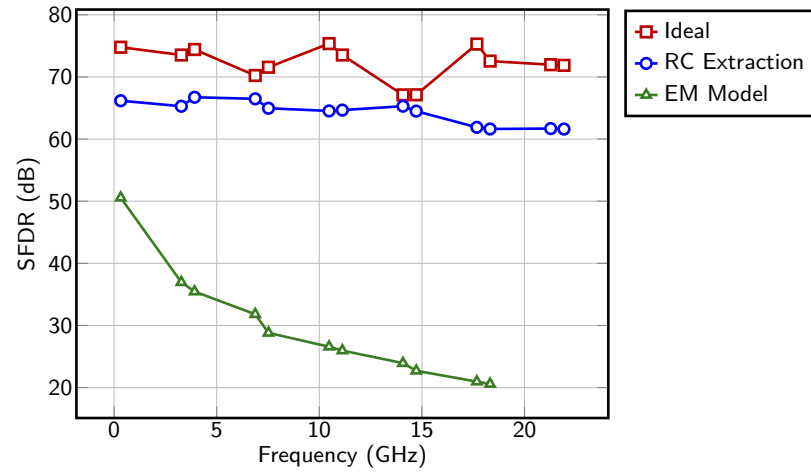


Figure 2.6: SFDR simulation results for using ideal, RC extracted, and EM models for the summing node

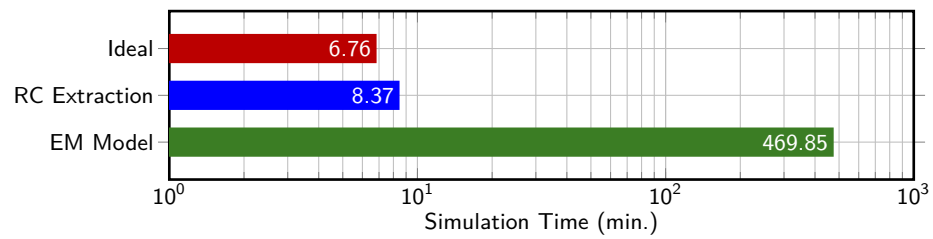


Figure 2.7: Simulation time for the conventional SFDR analysis using ideal, RC extracted, and EM models for the summing node

of amplitude errors have been reported, but focus on static metrics (i.e. integral and differential nonlinearity) and thus overlook how these errors manifest as spurs in the frequency domain [11–13]. Furthermore, these analyses neglect frequency-dependent amplitude and phase variations, relegating their use to low-frequency DACs. An extensive analysis of static timing errors has been report in [14]. However this analysis assumes that the errors are linearly distributed throughout a unary DAC, limiting its accuracy and making it difficult to generalize to other architectures.

2.4 High-Speed DAC Architectures

To improve SFDR performance across frequency, recently reported GHz DACs have largely focused on techniques to mitigate the expanding impact of deterministic jitter on SFDR as sample rates increase [15]. Return-to-zero (RZ) techniques can be used to de-glitch the data path, both reducing these dynamic errors and allowing synthesis in the second Nyquist zone without substantial zero-order hold (ZOH) loss. Unfortunately, dynamic errors still affect a sizable portion of the sample clock period, limiting reported RZ DACs to 7 GHz and 55 dB SFDR [16–20]. To further alleviate sampling requirements, interleaving has been proposed to synthesize a high effective sampling rate by operating multiple DACs in parallel, yielding 50 dB and 27 dB at 5.5 GHz and 25 GHz, respectively [21–24]. However, amplitude and timing mismatches between each interleaved DAC introduce additional spurs at the output that can limit SFDR, while the increased area required to accommodate multiple DACs can exacerbate mismatches in the clock distribution. Alternatively, the output frequency can be decoupled from the sampling rate via a mixer incorporated into the DAC to perform direct up-conversion of the signal to the desired RF band [25]. A

recent mixing DAC has demonstrated 50 dB SFDR across the Nyquist zone at 5 GHz with a sample rate of 1.75 GS/s [26, 27]. Unfortunately, mixing DACs do not perform de-glitching of the data path and require careful alignment of the sample and mixing clocks, creating a challenging trade-off between sample rate, output frequency, and SFDR, consequently limiting the instantaneous bandwidth of the system. To address these shortcomings, the multiple-return-to-zero approach (MRZ) approach, discussed in Section 2.5, combines RZ and mixing functionality to simultaneously suppress deterministic jitter and enable direct up-conversion [28, 29]. Recently, an MRZ DAC has achieved 42 dB SFDR at 9.45 GHz with a sample rate of 2.7 GS/s without calibration, making it a promising approach to high-frequency synthesis with minimal spurious emission [29].

In addition to the choice of DAC architecture, the selection of process technology is critical to achieving high linearity. CMOS technologies have greatly benefited from process scaling, leading to reduced parasitic and fast switching speeds, however the limited output impedance results in large dynamic amplitude and timing errors that can limit SFDR [21, 22, 30]. Although bipolar implementations in SiGe BiCMOS and InP processes can provide higher output impedance and switching speed than their CMOS counterparts, the large footprint of such devices exacerbates mismatches in the clock distribution and summing node, resulting in only small improvement in SFDR [18–20, 29].

2.5 The MRZ DAC Architecture

As noted in Section 2.4, the MRZ architecture is a composite of the RZ and mixing DAC techniques. These three architectures can simply be conceptualized as

a conventional NRZ baseband DAC followed by multiplication with an RZ or LO waveform. As shown in Figure 2.8(a), the RZ DAC multiplies the output with zero for half of each clock period ($f_{rz} = f_s = 1/T_s$), during which the input data is switched to improve SFDR by effectively blocking deterministic jitter in the data path from the output. Moreover, the frequency response of the RZ technique, shown in Figure 2.9, locates the first null at $2f_s$. This enables synthesis in the second Nyquist zone, relaxing the required sample rate by a factor of two for a given output frequency (f_{OUT}) at the cost of a 6 dB reduction output power compared to NRZ. However, to achieve 20 GHz operation, a sample rate of >40 GS/s is still required, limiting linearity performance due to coupling of the high-speed data-dependent signals to the RZ clock. To further reduce f_s independent of f_{OUT} , the RZ clock can be replaced with an LO ($f_{LO} = m_{mx}f_s$), as shown in Figure 2.8(b), to realize a mixing DAC in which the signal is upconverted to the Nyquist zones adjacent to f_{LO} . The frequency response of the mixing DAC, shown in Figure 2.9, exhibits a lobe centered at f_{LO} with a peak amplitude of -3.8 dB relative to the DAC full-scale range (FSR). While the mixing DAC can achieve arbitrarily high f_{OUT} for a given f_s , deterministic jitter from the data path feeds directly to the output, requiring significant reduction in sample rate to achieve the desired linearity performance. Additionally, the SFDR performance depends on the precise alignment between DCLK and LO. It has been shown that an alignment of less than 20° of the LO is required, introducing yet another source of error that deteriorates linearity with increasing f_{OUT} [27].

The MRZ architecture solves several of the shortcomings of RZ and mixing DACs by multiplying the RZ frequency with an integer number ($f_{rz} = m_{rz}f_s$) as shown in Figure 2.8. Note that RZ is a special case of MRZ in which $m_{rz} = 1$. As with the RZ

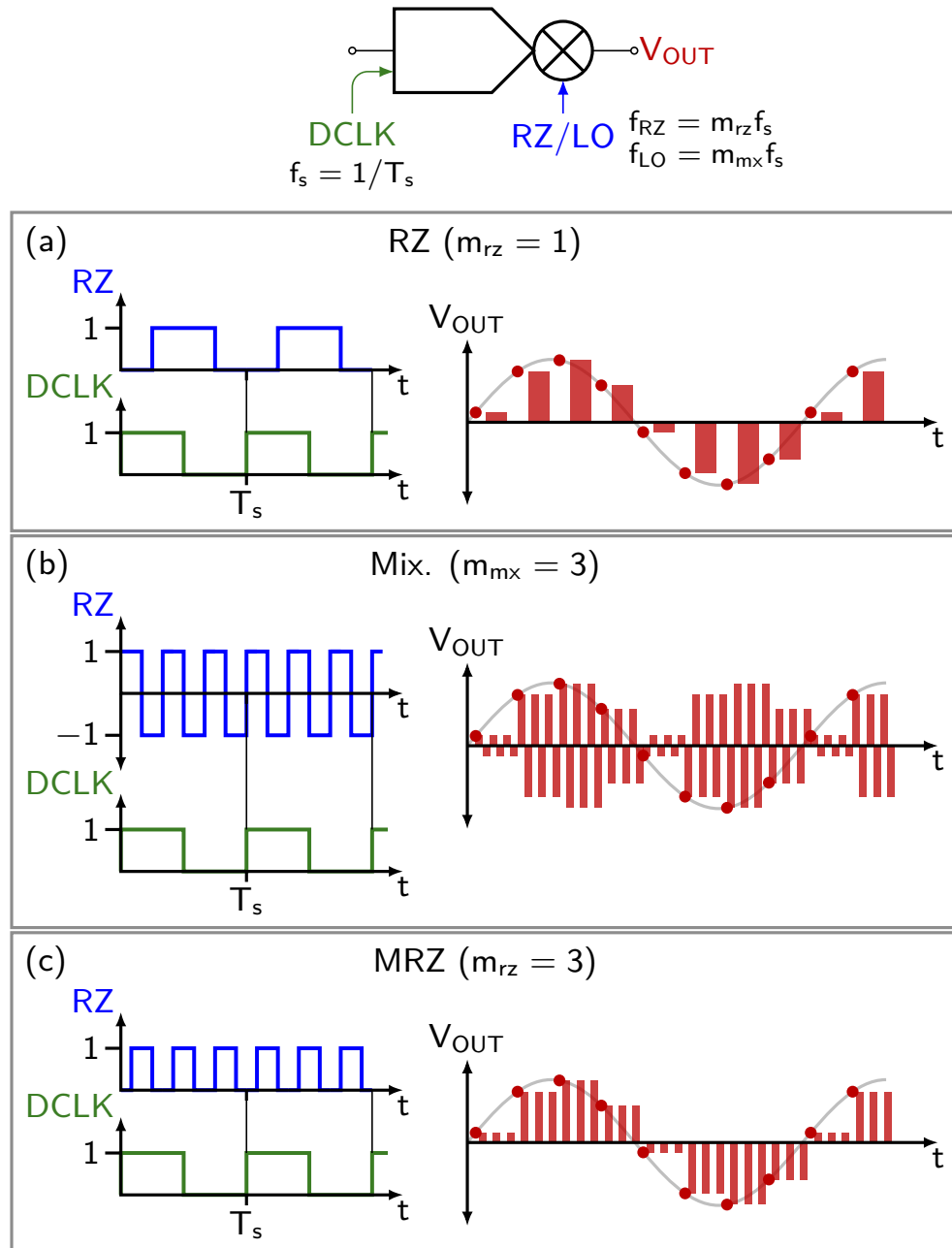


Figure 2.8: Example clock and output waveforms for (a) an RZ DAC, (b) a mixing DAC with $m_{\text{mx}} = 3$, and (c) an MRZ DAC with $m_{\text{rz}} = 3$

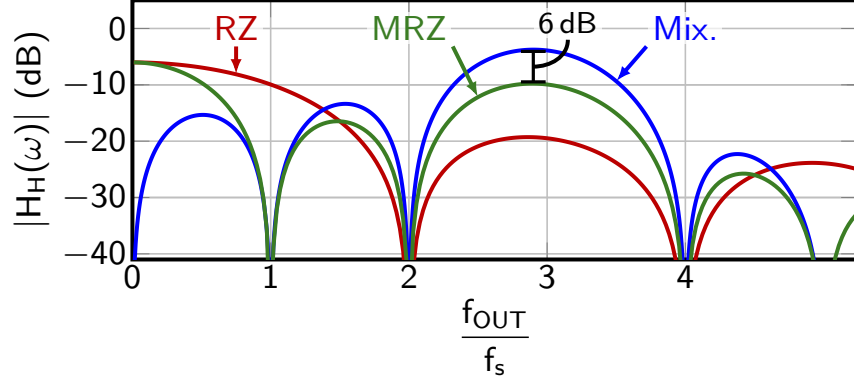


Figure 2.9: Magnitude of the frequency response for RZ, mixing, and MRZ waveforms

DAC, the MRZ approach mitigates deterministic jitter by resetting the output while the input data switches and only ideally requires alignment of DCLK to within 180° of the RZ clock period for optimal linearity. The effect of the MRZ operation can be determined from the frequency response of the hold shaping. The continuous-time Fourier transform (CTFT) of a rectangular pulse centered on $t = 0$ and having a width of T_W is given by

$$H_P(\omega) = T_W \frac{\sin\left(\frac{1}{2} T_W \omega\right)}{\frac{1}{2} T_W \omega} \quad (2.1)$$

Assuming a 50 % duty cycle, the MRZ frequency response can be found by summing m_{rz} pulses with appropriate width and phase

$$H_{MRZ}(\omega) = H_P(\omega) \Big|_{T_W = \frac{T_s}{2m_{rz}}} \cdot e^{\frac{-j\omega T_s}{2m_{rz}}} \sum_{m=0}^{m_{rz}-1} e^{\frac{-j\omega T_s}{m_{rz}} m} \quad (2.2)$$

The summation term of (2.2) can be simplified as a geometric series, yielding

$$H_{MRZ}(\omega) = H_P(\omega) \Big|_{T_W = \frac{T_s}{2m_{rz}}} \cdot e^{\frac{-j\omega T_s}{2}} \frac{\sin\left(\frac{\omega T_s}{2}\right)}{\sin\left(\frac{\omega T_s}{2m_{rz}}\right)} \quad (2.3)$$

As shown in Figure 2.9, $H_H(\omega)$ exhibits a major lobe centered on f_{rz} , with a normalized peak amplitude of -9.4 dB. Compared to a mixing DAC, this results in a

6 dB reduction in output power around the frequency of interest. Nonetheless, the mitigation of deterministic jitter and relaxed timing alignment provided by the RZ operation make MRZ a compelling option for achieving high linearity at 20 GHz and beyond.

2.6 Calibration of Static Errors

Although the DAC architecture can significantly mitigate the effect of deterministic jitter, static errors in amplitude and timing between unit cells remain the limiting factor in SFDR performance. At high frequency, both amplitude and timing errors can be caused by variation in the frequency response of the summing node for each cell, while mismatches in the clock distribution network and unit cell transistors create additional timing mismatch that must be accounted for. To compensate for these errors, amplitude calibration has been extensively studied [31–36], however timing calibration has received less attention. Current-starved inverters have been proposed to provide a per-cell programmable delay [37]. However, these circuits vary timing by degrading the rise/fall time of the clock, limiting their maximum operating frequency. Alternatively, mapping techniques have provided effective timing calibration without the need for additional analog circuitry [26, 38, 39]. Unfortunately, the effectiveness of such techniques depends on the use of many unary unit cells, increasing the area of the DAC and exacerbating clock distribution mismatches. Furthermore, this limits the application to CMOS technologies, precluding the use of larger SiGe or III-V devices which can potentially improve high-frequency performance with faster switching speeds and higher output impedance than their CMOS counterparts [18–20, 29].

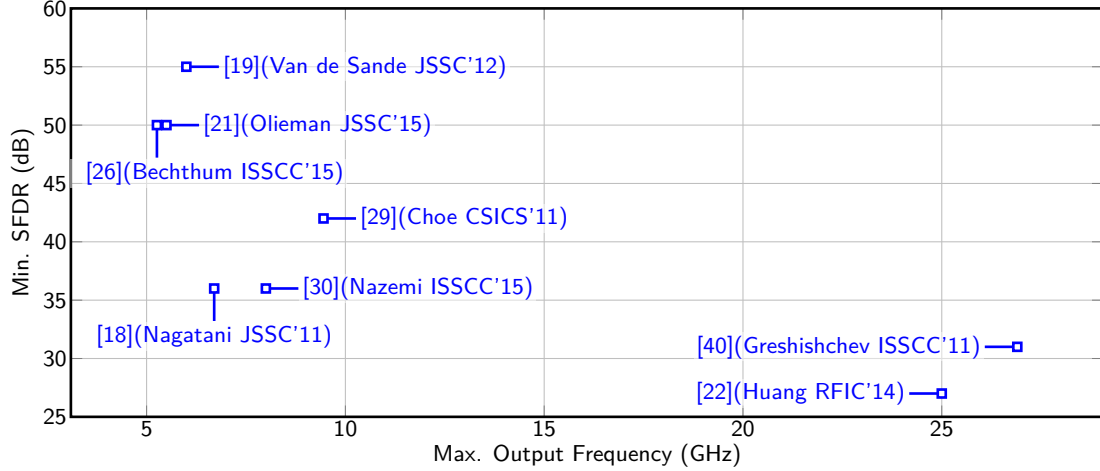


Figure 2.10: The maximum output frequency and worst-case SFDR for recently published DACs with $f_{\text{out}} > 5$ dB

2.7 The State of the Art

Figure 2.10 plots the maximum output frequency and worst-case SFDR of all DACs published in the past five years with output frequencies greater than 5 GHz. Due to the significant challenges in high-frequency DAC design, most of this work has been focused on frequencies below 10 GHz, while achieving less than 55 dB SFDR. The few DACs that exceed 20 GHz achieve less than 32 dB SFDR and are targeted towards wireline communications where linearity is not critical. Table 2.1 gives the detailed performance for each reported DAC. It is interesting to note that even very advanced technologies such as 28 nm CMOS and InP have been used to achieve the state-of-the-art performance. While these processes provide transistors with very high-speed operation, it is clear that many of the challenges in high-speed DAC design have yet to be addressed.

Table 2.1: Performance overview of recently published DACs

Reference	[40]	[22]	[29]	[30]	[18]	[19]	[21]	[26]
Tech. [nm]	65	28	500	28	1000	130	28	65
	CMOS	CMOS	InP	CMOS	InP	BiCMOS	CMOS	CMOS
Pwr [W]	0.75	2.5	1.6	0.144	0.95	8.3	0.11	0.38
P_{out} [dBm]	-3.5	-5	-15	-0.97	-10	1	-6.5	-8
f_S [GS/s]	56	100	2.7	18	28	12	11	1.75
f_{out} [GHz]	26.9	25	9.45	8	6.7	6	5.5	5.26
Min. SFDR [dB]	31	27	42	36	36	55	50	50
IM3@Freq. [dBc]/[GHz]	—	—	—	—	—	—	51@5.5	58@5

Chapter 3: A Frequency-Domain SFDR Analysis

This chapter presents a frequency-domain approach to SFDR analysis in which the contribution of each individual cell is analyzed and errors are applied as transfer functions in the frequency domain. Unlike the conventional analysis discussed in Section 2.3, the frequency-domain approach works well with the small-signal models produced by EM simulations, enabling the incorporation of complex output summing node structures with little impact to simulation time and convergence. As discussed in Chapter 4, this method has been applied to a state-of-the-art 10-bit multiple-return-to-zero (MRZ) DAC, achieving more than 48 dB SFDR performance from DC to 20 GHz [41].

3.1 Analyzing SFDR in the Frequency Domain

The frequency-domain (FD) analysis, illustrated in Figure 3.1 for a 3-bit binary DAC, is founded upon the assumption that the DAC output, $Z(\omega)$, is a linear superposition of the output of each current cell $Y_i(\omega)$. After finding $Y_i(\omega)$ through analytical derivation (Section 3.1.1) or transient simulation (Section 3.1.2), per-cell errors are applied with a transfer function, $H_i(\omega)$, in the frequency domain. This allows for the analysis to account for any source of error that can be expressed as a linear time-invariant (LTI) transfer function, including static amplitude and timing

errors as well as frequency-dependent attenuation and phase in the output summing node. Moreover, these errors can be studied using numerical computation or small-signal analysis, avoiding the expensive recalculation of the time-domain waveforms and enabling quick integration of EM models.

The assumption of linear superposition precludes some complex sources of errors, namely deterministic jitter and nonlinear output impedance. Nonetheless, it will be shown in Section 3.2 that time-invariant errors typically dominate performance at GHz and mm-wave frequency, enabling substantial improvements in SFDR in the state-of-the-art DAC discussed in Chapter 4.

3.1.1 Analytical Derivations

Analytical derivations are useful to develop an intuition of the contribution of each ideal current cell. For simplicity, this section develops analytical models for a 3-bit DAC of various configurations: 1) binary, 2) unary, and 3) segmented. The derivation follows a procedure similar to that of [42] and can be summarized as follows:

1. Develop an expression for the transfer function for each bit $x_{Q_i}(x)$.
2. Let $x = \sin(\omega_0 t)$ and solve for the quantized waveform of each bit, $x_{Q_i}(t)$.
3. Find $X_{Q_i}(\Omega)$, the continuous-time Fourier transform of $x_{Q_i}(t)$.
4. Apply a sample and hold to the signal to produce the discrete-time Fourier transform, $Y_i(\omega)$.

Binary DAC

Figure 3.2(a) shows the transfer function, $x_{Q_n}(x)$ ($n = 2 \dots 0$) for each bit in a $N = 3$ -bit binary quantizer. It will be assumed that the quantizer has a full-scale

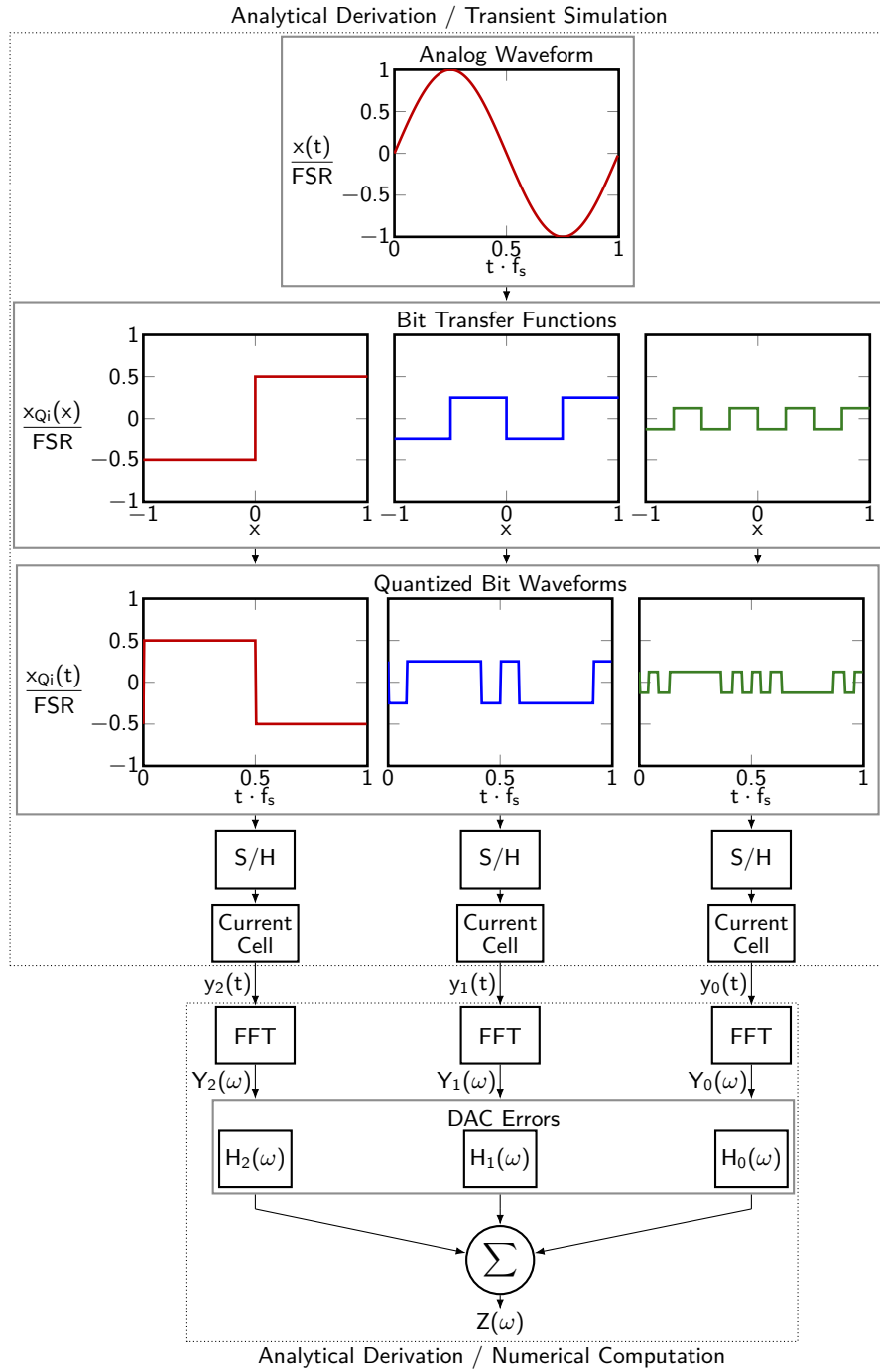


Figure 3.1: Block diagram of the frequency-domain analysis for a 3-bit binary DAC.

range of $\text{FSR} = 2$, such that the input is bound to $-1 < x < 1$. Outside of this range, it can be assumed that $x_{Qn}(t)$ is periodic without affecting the analysis, forming a square wave of amplitude 2^{N-n+1} and period $\text{FSR}/2^{N-n}$. Thus, the binary bit transfer functions for an N-bit quantizer can be expressed using the well-known Fourier series for a square wave

$$x_{Qn}(x) = \frac{-4 \text{FSR}}{\pi 2^{N-n}} e^{j\pi 2^{N-n-1}} \cdot \sum_{k=1}^{\infty} \frac{1}{2k-1} \sin \left[(2k-1) \frac{2^{N-n}}{\text{FSR}} \pi x \right] \quad (3.1)$$

Applying a single tone, $x(t) = \sin(\omega_0 t)$, to the quantizer yields the time-domain waveform for each bit

$$x_{Qn}(t) = \frac{-4 \text{FSR}}{\pi 2^{N-n}} e^{j\pi 2^{N-n-1}} \cdot \sum_{k=1}^{\infty} \frac{1}{2k-1} \sin \left[(2k-1) \frac{2^{N-n}}{\text{FSR}} \pi \sin(\omega_0 t) \right] \quad (3.2)$$

The sine term of (3.2) can be simplified using a Jacobi-Anger expansion to produce

$$x_{Qn}(t) = \sum_{p=0}^{\infty} A_n(2p+1) \sin [(2p+1) \omega_0 t] \quad (3.3)$$

where $A_n(q)$ is the amplitude of each harmonic which can be separated into even and odd harmonics

$$A_n(q) = \begin{cases} A_{no}(q) & \text{odd } q \\ 0 & \text{even } q \end{cases} \quad (3.4)$$

$$A_{no}(q) = \frac{-8 \text{FSR}}{\pi 2^{N-n}} \sin(\pi 2^{N-n-1} + \pi/2) \cdot \sum_{k=1}^{\infty} \frac{1}{2k-1} J_q \left[(2k-1) \frac{2^{N-n}}{A_B} \pi \right] \quad (3.5)$$

where $J_n(z)$ is the Bessel function of the first kind. With (3.3) expressed as a sum of sinusoids, it is trivial to develop the continuous-time Fourier transform (CTFT)

$$X_{Qn}(\Omega) = \frac{\pi}{j} \sum_{q=0}^{\infty} A_n(2q+1) \cdot [\delta(\Omega - (2q+1) \omega_0) - \delta(\Omega + (2q+1) \omega_0)] \quad (3.6)$$

Figure 3.2(b) plots $A_n(q)$ for each bit of the quantizer with the finite summation computed up to $k = 10^6$. From (3.3), (3.5) and (3.11), it is clear that each current cell

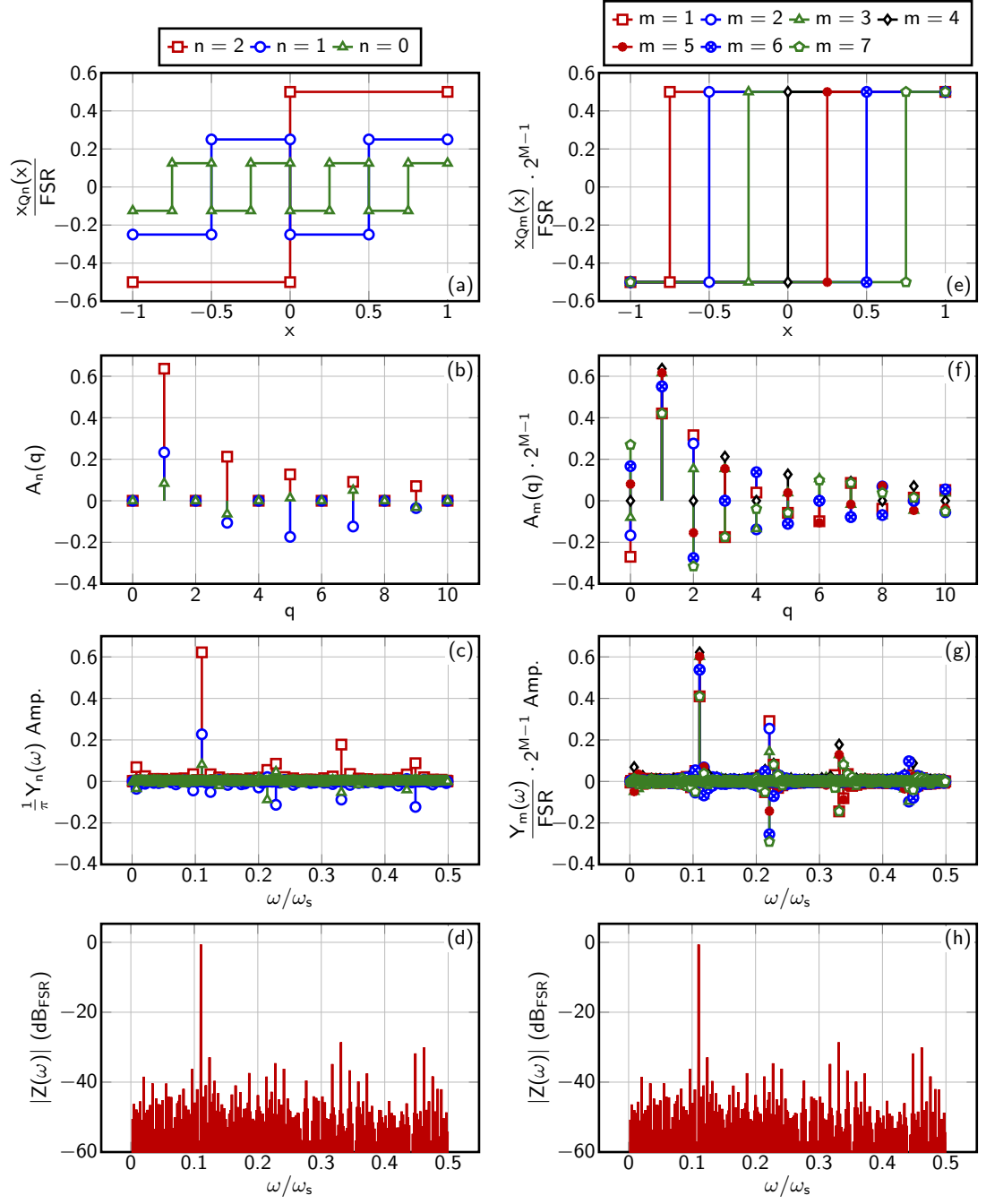


Figure 3.2: Analytical results for (b)–(d) a 3-bit binary DAC and (e)–(h) a 3-bit unary DAC

in the DAC is producing a tremendous amount of spurious content. It is worth noting that the top three bits of any binary DAC with $N > 3$ will have waveforms as shown in Figure 3.2, with additional bits added as LSBs. Each bit added to the quantizer cancels a portion of the spurs generated by the bits before it, confirming the importance of amplitude and phase matching to preserve this cancellation. Furthermore, each bit of the quantizer produces only odd harmonics, indicating that no amount of LTI errors can induce second-order spurs. Therefore, any second-order frequency content observed at the output of the a binary DAC must be caused by data-dependent amplitude or timing errors which are unaccounted by the frequency-domain analysis [7, 14].

To complete the derivation, the quantized waveform described in (3.6) must undergo sampling and holding which can be applied by aliasing the signal to each Nyquist zone and applying the hold attenuation, yielding

$$Y_n(\omega) = H_H(\omega) \sum_p X_{Qn}(\omega - p\omega_s) \quad (3.7)$$

where $\omega_s = 2\pi f_s$ and f_s is the sample rate of the DAC. Assuming a non-return-to-zero first-order hold, its CTFT is given by the well-known rectangular pulse

$$H_H(\omega) = e^{-j\frac{\omega}{2f_s}} \frac{\sin\left(\frac{\omega}{2f_s}\right)}{\frac{\omega}{2f_s}} = e^{\frac{j\omega}{2f_s}} \text{sinc}\left(\frac{f}{f_s}\right) \quad (3.8)$$

Although the sample and hold operation changes the phase of every harmonic, the phase relationship between each cell remains the same. For easy visualization, the phase of each harmonic can be normalized to that of the MSB cell. Figure 3.2(c) plots the amplitude of $Y_n(\omega)$ for the first 10^4 harmonics with $\omega_s = 1024/113$. Note that what is typically considered the quantization “noise” floor in a DAC arises from the folding of all quantization harmonics into the band of interest. Figure 3.2(d) shows

the power spectral density (PSD) of the combined DAC output exhibiting 27.98 dB. After accounting for 0.175 dB of hold attenuation, this gives an error of less than 0.74 dB from the 27.07 dB SFDR of an ideal 3-bit DAC [43].

Unary DAC

Figure 3.2(e) shows the transfer function, $x_{Qm}(x)$ ($m = 7 \dots 1$), for each bit in a $M = 3$ -bit unary-encoded quantizer comprising $2^M - 1$ unit cells. Following a procedure identical to that of the binary DAC, the bit transfer functions can be expressed as rectangular pulse trains with a period of $T = 2 \text{FSR}$, duty cycle of $1 - m \cdot 2^{-M}$, and amplitude of $\pm 2^{-M}$, giving the CTFT

$$x_{Qm}(t) = \frac{1}{2^M} \left(\frac{m}{2^{M-1}} - 1 \right) + \frac{m}{2^{2(M-1)}} \cdot \sum_{k=1}^{\infty} \text{sinc} \left(\pi k \frac{m}{2^M} \right) \cos \left[\frac{2}{\text{FSR}} \pi k x(t) + \frac{m}{2^M} k \pi \right] \quad (3.9)$$

After applying the Jacobi-Anger expansion, the quantized waveforms can be separated into DC, odd, and even order components

$$x_{Qm}(t) = A_m(0) + \sum_{q=1}^{\infty} A_m(2q) \cos(2q\omega_0 t) + A_m(2q+1) \sin(2q\omega_0 t) \quad (3.10)$$

where

$$A_m(q) = \begin{cases} A_{mDC} & q = 0 \\ A_{mo}(q) & \text{odd } q \\ A_{me}(q) & \text{even } q \neq 0 \end{cases} \quad (3.11)$$

$$A_{mDC} = \frac{1}{2^M} \left(\frac{m}{2^{M-1}} - 1 \right) + \frac{m}{2^{2(M-1)}} \cdot \sum_{k=1}^{\infty} J_0 \left(\frac{2}{\text{FSR}} k \pi \right) \text{sinc} \left[\pi k \frac{m}{2^M} \right] \cos \left[\pi k \left(\frac{m}{2^M} - 1 \right) \right] \quad (3.12)$$

$$A_{me}(p) = 2 \frac{m}{2^{2(M-1)}} \sum_{k=1}^{\infty} J_{2p} \left(\frac{2}{\text{FSR}} k \pi \right) \text{sinc} \left[\pi k \frac{m}{2^M} \right] \cdot \cos \left[\pi k \left(\frac{m}{2^M} - 1 \right) \right] \quad (3.13)$$

$$A_{mo}(q) = -2 \frac{m}{2^{2(M-1)}} \sum_{k=1}^{\infty} J_{2q-1} \left(\frac{2}{\text{FSR}} k\pi \right) \cdot \text{sinc} \left[\pi k \frac{m}{2^M} \right] \sin \left[\pi k \left(\frac{m}{2^M} - 1 \right) \right] \quad (3.14)$$

In contrast to binary DACs, unary current cells generate a significant amount of second-order spurs. Interestingly, the m^{th} cell cancels all of the second-order harmonics of cell $M - m$, indicating that the pairs of cells should be well-matched in amplitude and phase. This insight can be used to guide decisions for the layout of the DAC core in order to yield optimal SFDR performance.

As with binary DACs, sampling of the unary quantized waveform simply folds harmonics into every Nyquist zone

$$\begin{aligned} X_{Qm}(\Omega) = & A_m(0)\delta(\Omega) + \sum_{q=1}^{\infty} \pi A_m(2q) [\delta(\Omega - 2q\omega_0) + \delta(\Omega + 2q\omega_0)] \\ & + \frac{\pi}{j} A_m(2q+1) [\delta(\Omega - (2q+1)\omega_0) - \delta(\Omega + (2q+1)\omega_0)] \end{aligned} \quad (3.15)$$

as shown in Figure 3.2(g) where the phase of each harmonic was referred to the middle cell ($m = 4$). The combined DAC output shown in Figure 3.2(h) is finally given by

$$Y_m(\omega) = H_H(\omega) \sum_p X_{Qm}(\omega - p\omega_s) \quad (3.16)$$

As expected, the combined output of the unary DAC matches that of the binary DAC in Figure 3.2(d).

Segmented DAC

With the analyses of binary and unary DACs from Sections 3.1.1 and 3.1.1, respectively, it is easy to derive similar results for a segmented DAC. Consider an L -bit segmented DAC with M unary-encoded MSB cells, and $N = L - M$ binary-encoded LSB cells. The M unary cells will have an identical response to an M -bit unary-encoded DAC, while the N LSB cells will have the same response as the lowest N

cells of an L -bit binary DAC. Thus, the analysis of a segmented DAC simply yields

$$Y_i(\omega) = \begin{cases} Y_n(\omega)|_{n=i} & 0 \leq i < N \\ Y_m(\omega)|_{m=i-N+1} & N \leq i \leq N + M \end{cases} \quad (3.17)$$

All of the previous observations for binary and unary DACs apply to the corresponding cells of the segmented DAC. For instance, if a segmented DAC produces second-order spurs in the presence of LTI errors, these spurs must be caused by the unary-encoded cells.

3.1.2 Simulation-Based Approach

Although the analytical derivations provide excellent insight into the manifestations of harmonic content within a DAC, they involve infinite summations that require lengthy computations, and the ideal current cell assumption can produce optimistic results. A far simpler approach is to obtain the time-domain output of each cell, $y_i(t)$ in Figure 3.1, via transient simulation and transform the results to the frequency-domain using numerical computation. In addition to simple computation, this approach can accommodate transistor-level designs for the current cells and any preceding circuitry. Notably, this will account for some deterministic jitter errors, such as those induced by the digital circuitry in the data path. For these reasons, this approach was chosen to aide in the design of the state-of-the-art DAC presented in Chapter 4.

Figures 3.3(a) and (b) show the frequency-domain contribution of the behavioral 3-bit binary and unary DACs, respectively, from a transient simulation. As in Section 3.1.1, the phase of each harmonic has been normalized to the phase of the corresponding harmonic in the MSB ($n = 2$) of the binary DAC and the middle cell ($m = 4$) of the unary DAC. The simulation-based approach produces similar results

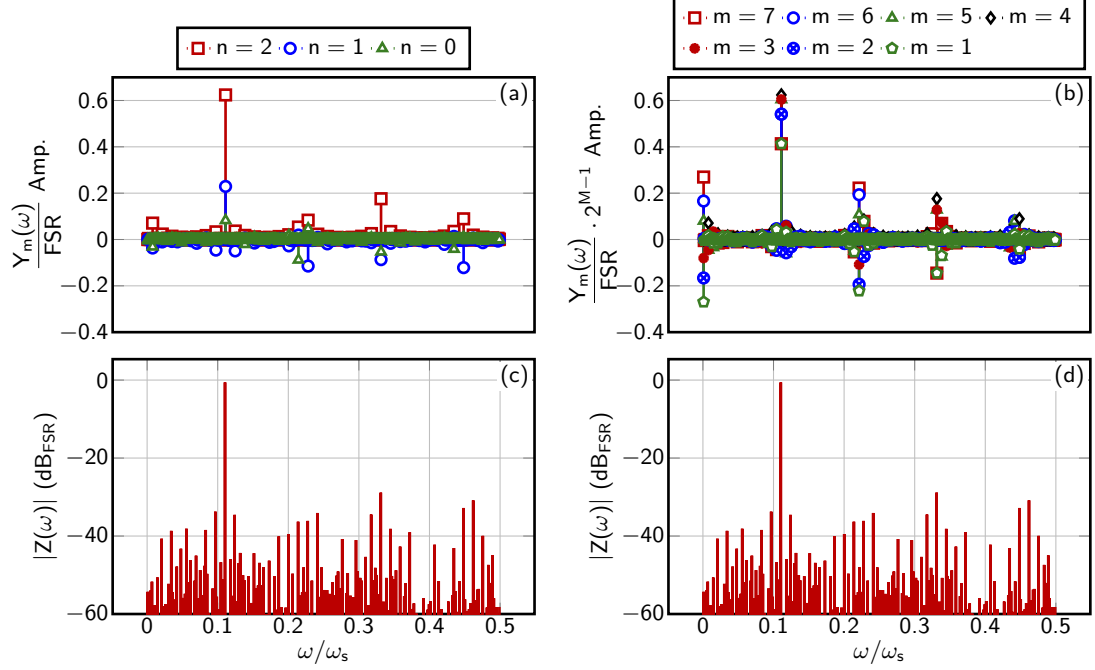


Figure 3.3: The frequency-domain analysis using the simulation-based approach including (a), (c) the amplitude of tones and (b), (c) the combined output of a 3-bit binary and 3-bit unary DAC, respectively

to that of the analytical derivations. Figures 3.3(a) and (b) show the combined outputs of the binary and unary DAC, respectively. Although the dominant spurs match those of the analytical results, there are some differences apparent in the spurs below -50 dB due to limited accuracy in the finite summations of the analytical results.

3.2 Application to the Output Summing Node

While the FD analysis is capable of accounting for any static amplitude and timing errors, it is uniquely suitable to frequency-dependent errors in the output summing node, detailed in Section 2.2. To perform the analysis, an EM model of the output summing node is created, after which it is attached to the DAC in a small-signal

analysis to obtain the frequency response for each cell. As shown in Figure 3.1, this frequency response is then applied to the FD analysis as $H_i(\omega)$ to determine the combined output.

Figure 3.4(a) shows the frequency response of the TTL for each cell in the 10-bit DAC of Section 4.1 with a spacing of $L = 25$ m. The attenuation variation throughout the DAC is 0.8 dB, indicating that there is a significant disparity in impedance between each cell and the output. Furthermore, the phase is spread out by more than 20° , indicating that variations in the time-of-flight for the output of each cell also contribute to the SFDR degradation.

Figure 3.5 shows the simulated SFDR using an EM model of the TTL, assuming that all current cells are clocked at the same time. As shown, the frequency-domain analysis predicts the SFDR degradation to within 4 dB of the transient simulation. With an ideal summing node, the DAC achieves > 70 dB SFDR up to 20 GHz, indicating outstanding deterministic jitter and output impedance characteristics. However, even a short $L = 10$ m between cells degrades the SFDR by over 30 dB.

The degradation in SFDR is caused in part by the phase variation shown in Figure 3.4. A common solution is to use a tapped transmission line to distribute the data clock to each cell such that the delay of the clock offsets the delay of the output node as shown in Figure 2.2. Fortunately, the FD analysis provides a quick and easy way to study the impact of this kind of design modification by applying an ideal timing compensation to each cell to simulate a data clock distribution that perfectly offsets the output delays. Figure 3.6 shows the SFDR of the TTL with this timing compensation, yielding an SFDR improvement of 10 dB. This result is still 20 dB lower than the ideal due to variations in the attenuation in the output node. Nonetheless,

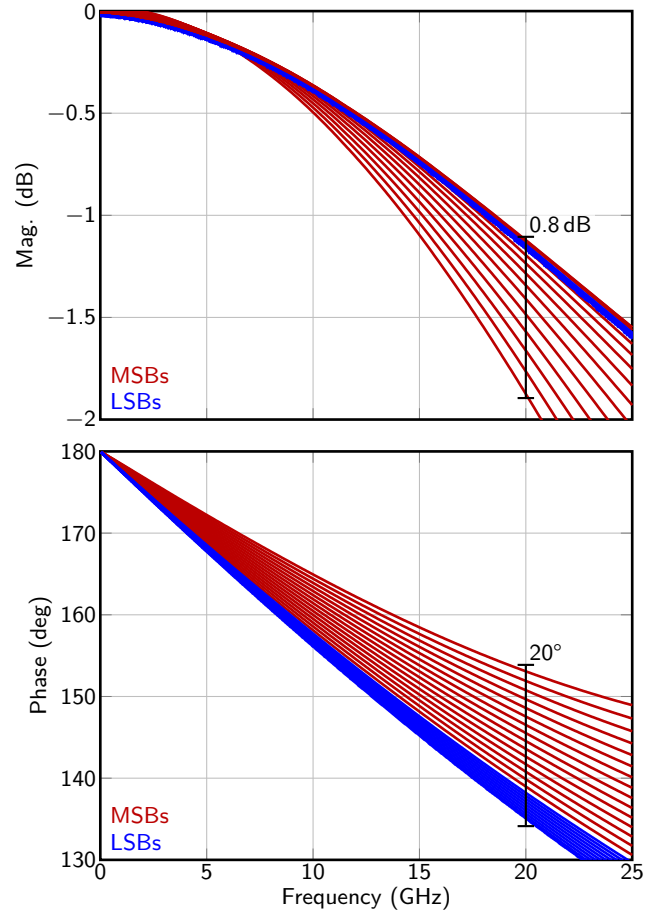


Figure 3.4: Frequency response for each cell for a TTL summing node

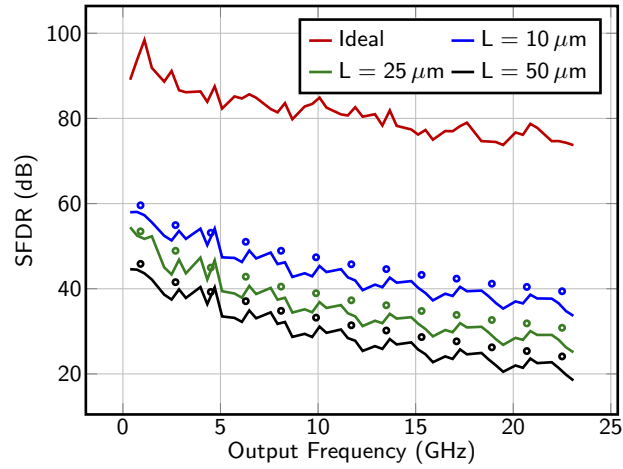


Figure 3.5: SFDR simulation of the TTL summing node

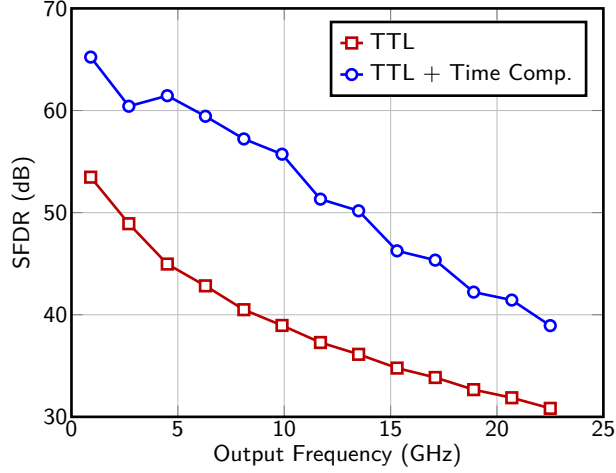


Figure 3.6: SFDR analysis using various models of the TTL summing node

mismatches are inevitable due to differences between the clock distribution and output node, so the measured performance will realistically lie between the two curves. To overcome the limitation of the TTL Section 4.2.2 introduces a new output summing node structure which provides significant improvements to the matching of phase and amplitude between cells.

Chapter 4: A DC-20GHz DAC with >48 dB SFDR

This chapter presents a 10-bit 3.35 GS/s MRZ DAC capable of synthesizing frequencies from DC to 20 GHz with greater than 48 dB SFDR. The design includes a vertically-stacked tree (VST) interconnect structure, developed using the frequency-domain analysis of Section 3.1, to minimize attenuation and phase mismatches in the output summing node. Additionally, a per-cell timing adjustment circuit is proposed, which, along with static current calibration, is used to minimize the remaining errors. The combination of the VST and calibration techniques yield the highest reported SFDR at 20 GHz, while synthesizing the largest instantaneous bandwidth among RF DACs.

4.1 The 10-bit MRZ DAC Architecture

The proposed 10-bit MRZ DAC architecture is shown in Figure 4.1. To perform the MRZ operation, each unit cell includes a local set of RZ switches which steer the current to the power supply or DAC output on the positive and negative RZ clock phases, respectively. In contrast to global RZ switching, local switching divides the return-to-zero process into inherently linear 1-bit operations [17, 44]. The linearity then largely depends only on matching of the amplitude and phase in the summing node and clock distribution.

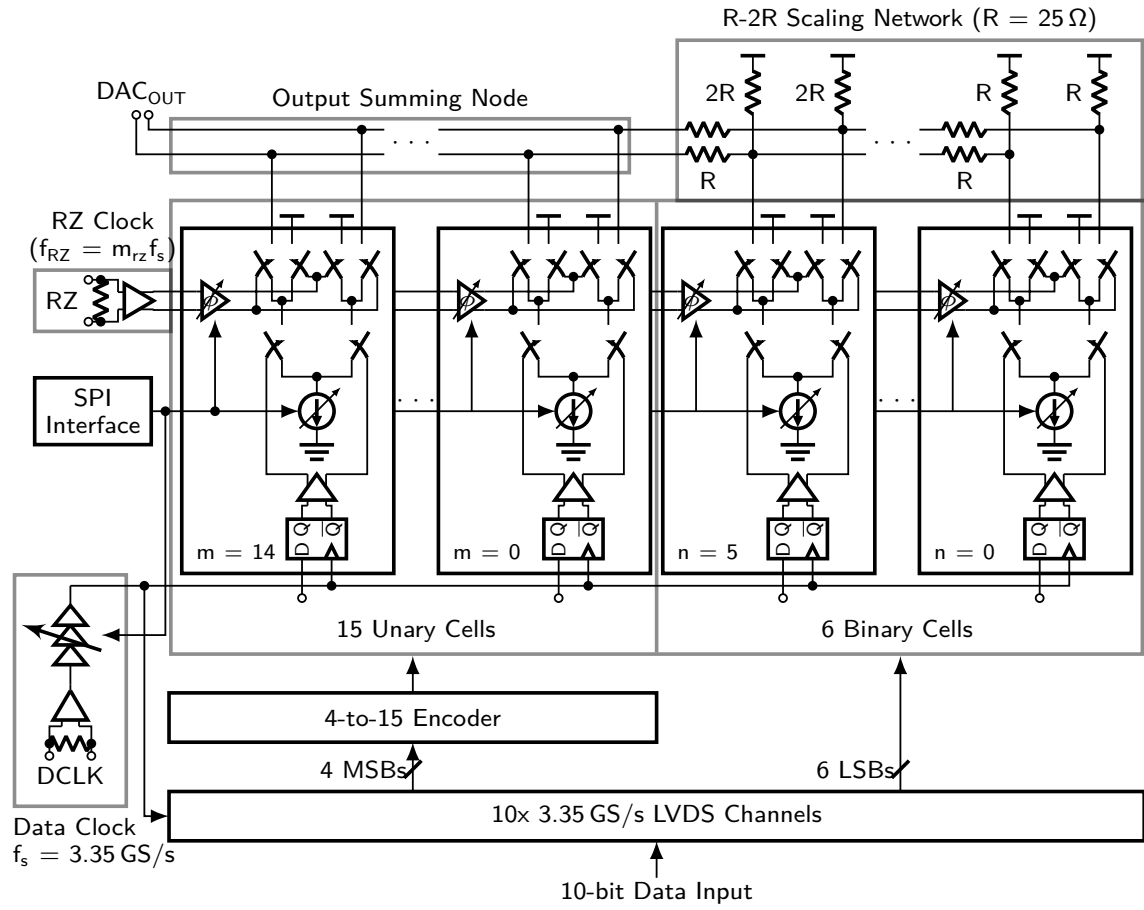


Figure 4.1: Block Diagram of the MRZ DAC architecture

As a trade-off between area, output power, and current matching, the DAC architecture uses a segmented architecture comprising 15 unary-weighted MSB cells and 6 binary-weighted LSBs. Binary scaling for the LSBs is achieved using an R-2R attenuation network which additionally provides a $100\,\Omega$ differential on-chip termination [17, 20, 29]. This configuration enables the use of identical current cells for MSBs and LSBs, minimizing timing mismatch by ensuring uniform loading of the RZ clock distribution. Furthermore, the R-2R network is particularly advantageous in BJT implementations wherein the f_T of the device is proportional to its current density and the minimum device size is much larger than that of CMOS. Conventional binary current scaling results in very small currents in the LSB cells which are far too small to support optimum f_T in a minimum size device, resulting in slower switching than the MSBs. In contrast, the R-2R network avoids these timing errors by allowing for a uniform current density, and therefore switching speed, throughout all DAC cells. Although the addition of the R-2R network prevents variations in the clock distribution and device switching speed caused by binary scaling of the current cells, it introduces additional amplitude and timing errors at the output of the LSBs. Specifically, each LSB must propagate through a different number of R-2R stages, incurring variations in attenuation and phase due to the RC time constant of each stage. However, ensuring that $(2\pi RC)^{-1}$ is small relative to the frequency of operation results in a relatively minor deterministic effect that can be corrected with the calibration circuitry detailed in Section 4.3.

4.2 The Output Summing Node

The recent literature discussed in Chapter 1 has largely focused on linearity enhancements in the DAC core circuitry and calibration for random current and timing errors. However, Section 3.2 has shown that as the wavelength of operation approaches the physical size of the DAC, variations in attenuation and phase shift in the output summing node can lead to frequency-dependent amplitude and timing errors among MSB cells which dominate the SFDR performance. The frequency-dependent nature of these errors makes measurement, and therefore calibration, over large bandwidths quite challenging. Instead, this section introduces improvements to the output summing node structure to inherently minimize mismatches across frequency, enhancing the linearity performance without the need for calibration.

4.2.1 The Vertically-Stacked Tree

The vertically-stacked tree structure shown in Figure 4.3 is proposed as an alternative to the TTL to improve the frequency response matching between each cell. The tree provides identical path lengths for each cell, minimizing variations in both attenuation and phase. Furthermore, metal extensions at each level equalize capacitive coupling between adjacent levels of the tree. To minimize area and capacitive loading, each branch of the tree is stacked vertically using successive metal layers. The R-2R network is tied to the VST with the top metal, forming a transmission line that connects to the output pads.

As shown in Figure 4.4(a), the VST achieves a significant reduction in frequency response variation among the MSBs, resulting in just 0.15 dB and 1° of amplitude and phase mismatch, respectively. Figure 4.5 shows the SFDR of the DAC using the

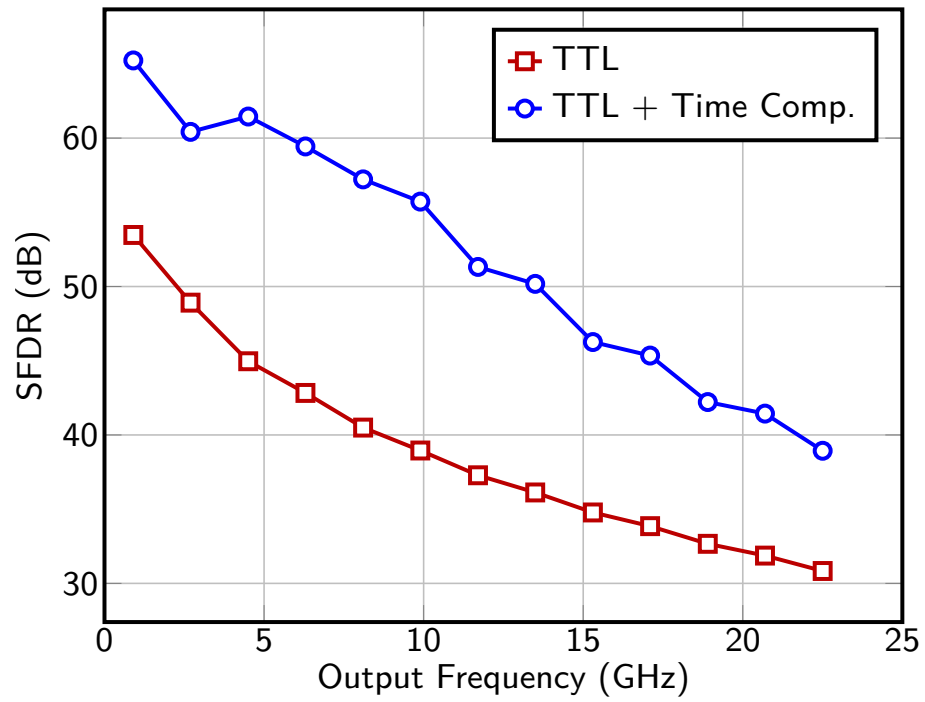


Figure 4.2: The SFDR performance of the TTL transmission line assuming an ideal DAC

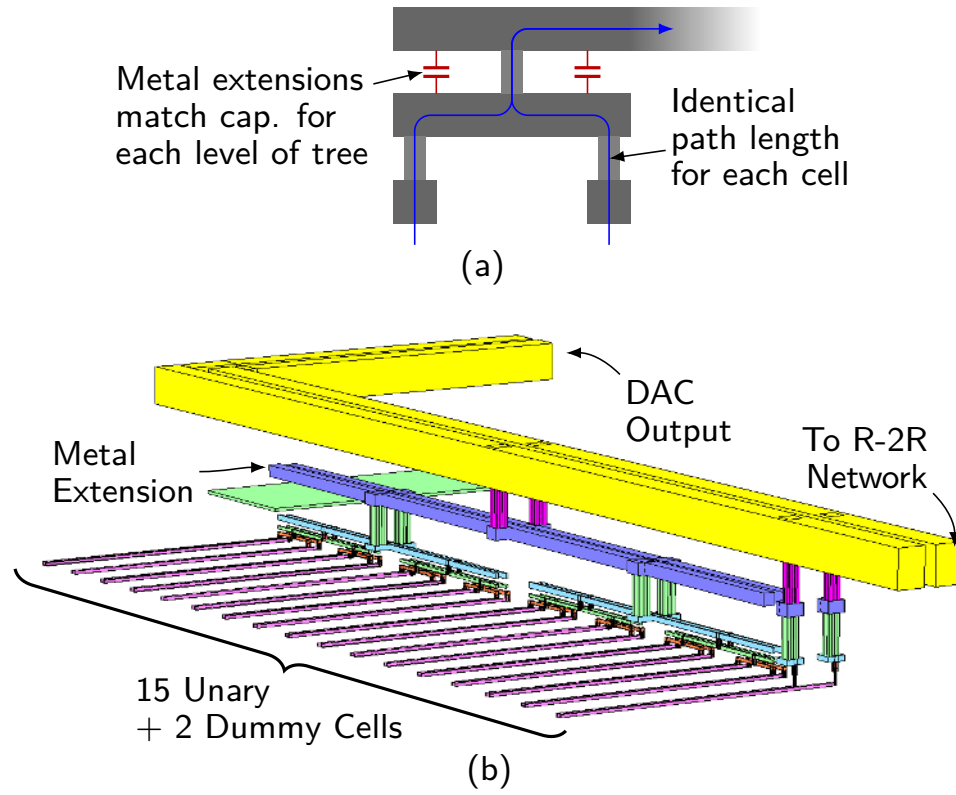


Figure 4.3: (a) An illustration of the VST structure and (b) the 3D model used for electromagnetic simulation

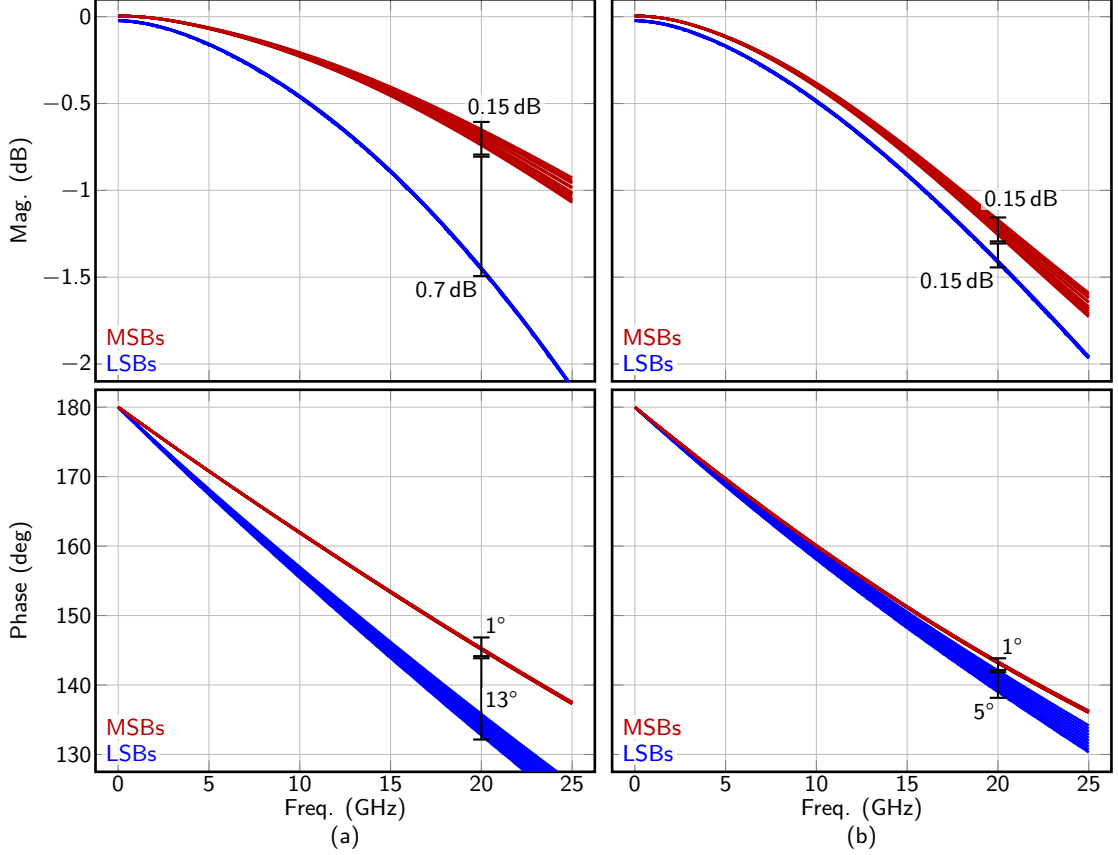


Figure 4.4: Frequency response of the VST summing node with (a) $C_{FF} = 0$ and (b) $C_{FF} = 105$ fF

VST, yielding an 8 dB improvement in SFDR at 20 GHz compared to the TTL with ideal timing compensation.

4.2.2 The Feedforward Network

While the VST ensures tight matching among the unary cells, there is significant mismatch between the LSBs and MSBs. This is caused by the RC attenuation formed by the last R-2R resistor and the lumped capacitance presented by the MSB cells and VST. To compensate for this effect, a feed-forward network (R , C_{FF}), shown

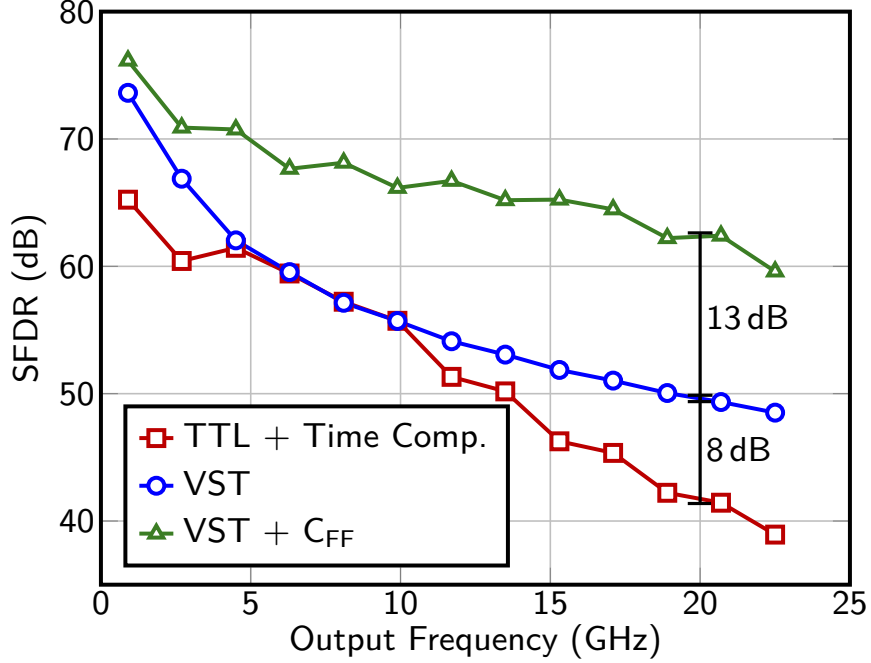


Figure 4.5: SFDR performance of the VST summing node

in Figure 4.6, is added to advance the phase of the binary cells and further attenuate the unary cell outputs, aligning the frequency responses of both segments. As shown in Figure 4.4(b), choosing $C_{FF} = 105$ fF reduces the total attenuation and phase mismatch between MSBs and LSBs to 0.3 dB and 6° .

As shown in Figure 4.5, the feed-forward network provides an additional 11 dB improvement to the VST, yielding an SFDR of 61 dB at 20 GHz. Figure 4.7 shows the SFDR for various values of C_{FF} . The maximum SFDR occurs with $C_{FF} = 105$ fF. A 5% variation in C_{FF} yields < 2 dB reduction in SFDR, indicating that this approach is resilient to process variations.

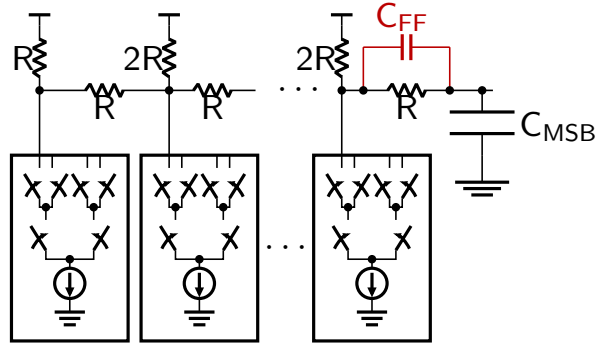


Figure 4.6: The vertically-stacked tree structure and feed-forward network.

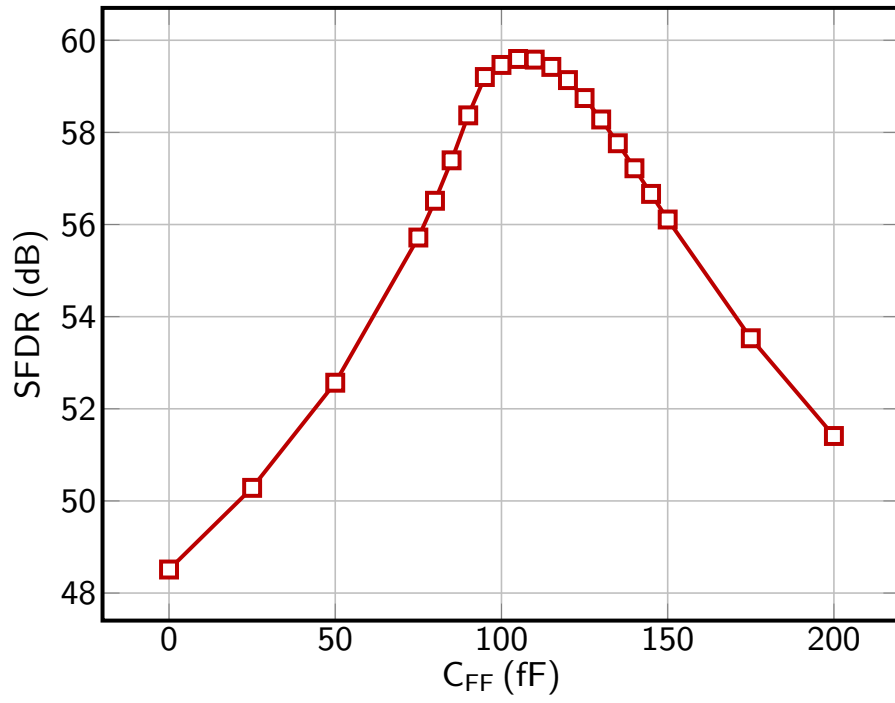


Figure 4.7: Impact of C_{FF} on SFDR at 20 GHz

4.3 Circuit Implementation

4.3.1 The DAC Unit Cell

A schematic of the MRZ DAC unit cell is shown in Figure 4.8, highlighting the local RZ and data drivers common to each cell. The DAC cell makes use of SiGe HBTs for the switching pairs which, although large, exhibit superior switching speeds and output impedance compared to their CMOS counterparts. The HBTs are biased at a current density of $1 \text{ A}/\mu\text{m}$ to provide an $f_T = 190 \text{ GHz}$. To improve current matching among the DAC cells, each unit cell current source is large and is implemented with interdigitation and common-centroid layout techniques. Current matching is further improved with a X bit calibration DAC implemented with parallel, binary-weighted current sources. The drain of each current source is then cascoded with an HBT to enhance its impedance and isolate the data switches from the current source routing and drain capacitance.

4.3.2 Local RZ Driver with Timing Control

The proposed VST structure and feed-forward path minimize the deterministic static mismatches in the amplitude and timing of the output network. However, random mismatches within the RZ switches and clock distribution introduce further static variations in the DAC cells, limiting SFDR performance. This SFDR degradation is shown in Figure 4.9 where the results of a Monte Carlo (MC) simulations of a behavior MRZ DAC model are given, the results representing a 99.73 % SFDR yield with a 95 % confidence level. As expected, the impact of these errors varies with frequency, resulting in a 20 dB reduction from $m_{rz} = 1$ to $m_{rz} = 6$. For an SFDR $> 50 \text{ dB}$ at $m_{rz} = 6$, the static σ_t must be less than 75 fs requiring an RZ

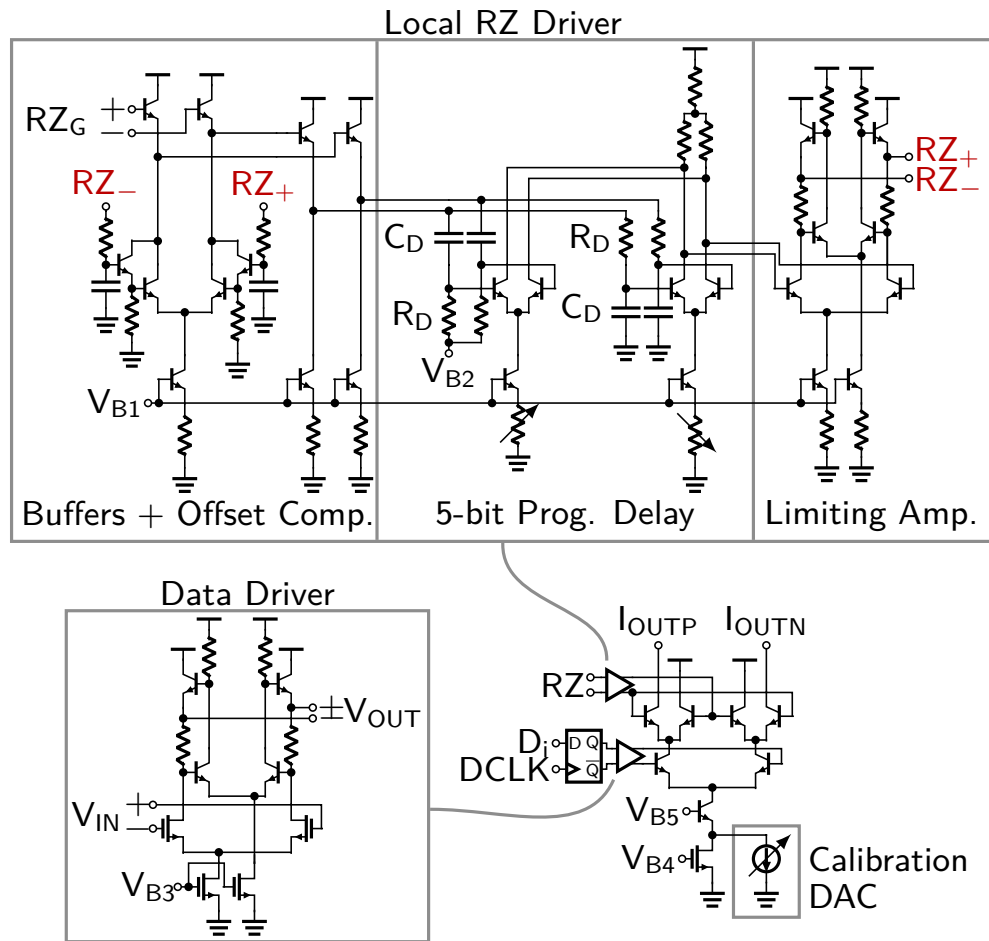


Figure 4.8: Schematic of the DAC unit cell

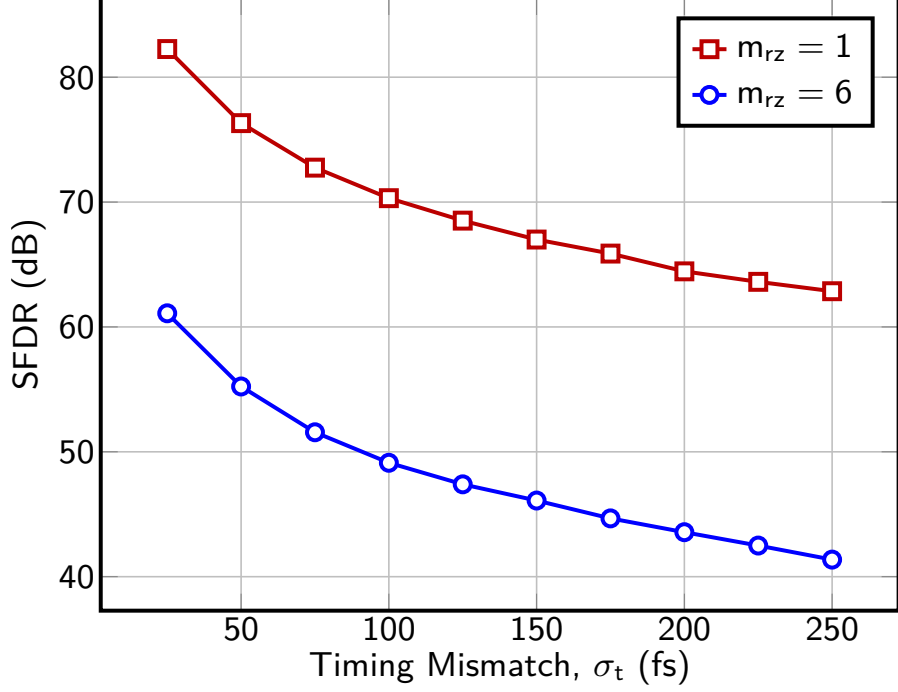


Figure 4.9: Behavioral simulation of static timing mismatches

clock accuracy within 225 fs ($3\sigma_t$) for each DAC cell. To achieve this, the MRZ DAC utilizes local clock drivers with per-cell timing adjustment.

A block diagram of the local RZ driver with timing adjustment is shown in Figure 4.10. The global RZ clock (RZ_G) is buffered and is then used to generate in-phase and quadrature components via phase shifters formed by R_D and C_D . The in-phase and quadrature components are then weighted (A_I , A_Q) and summed to produce the local RZ clock.

The transfer function of the local RZ driver is derived as

$$H_{RZ}(\omega) = \frac{RZ}{RZ_G} = A_I \frac{1}{1 + sR_D C_D} + A_Q \frac{sR_D C_D}{1 + sR_D C_D} \quad (4.1)$$

$$= A_I \frac{1 + sR_D C_D \frac{A_Q}{A_I}}{1 + sR_D C_D} \quad (4.2)$$

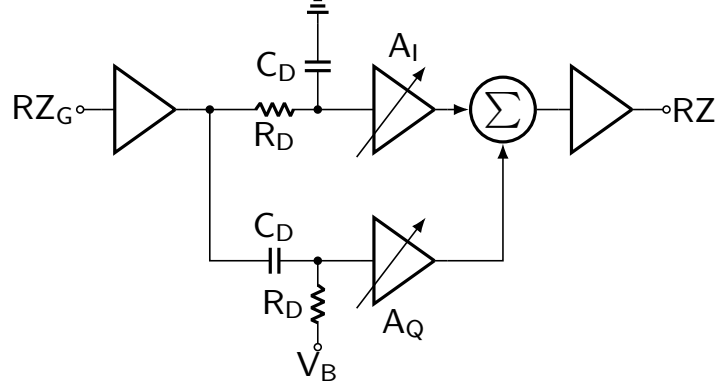


Figure 4.10: Block diagram of the timing adjustment circuit

The delay can be obtained from the phase of (4.1)

$$\Delta t = \frac{\angle H_{RZ}(\omega)}{\omega} \quad (4.3)$$

$$= \frac{1}{\omega} \left[\arctan \left(\omega R_D C_D \frac{A_Q}{A_I} \right) - \arctan (\omega R_D C_D) \right] \quad (4.4)$$

Using the identity

$$\arctan x - \arctan y = \arctan \left(\frac{x - y}{1 + xy} \right) \quad (4.5)$$

the delay can be simplified to

$$\Delta t = \frac{1}{\omega} \arctan \left[\frac{\omega R_D C_D \left(\frac{A_Q}{A_I} - 1 \right)}{1 + \omega^2 R_D^2 C_D^2 \frac{A_Q}{A_I}} \right] \quad (4.6)$$

Assuming $0 \leq \frac{A_Q}{A_I} \leq 1$ The full-scale range of the timing adjustment is given by

$$\text{FSR}_t = \Delta t \Big|_{\frac{A_Q}{A_I}=1} - \Delta t \Big|_{\frac{A_Q}{A_I}=0} = \frac{1}{\omega} \arctan(\omega R_D C_D) \quad (4.7)$$

For $\omega \ll (R_D C_D)^{-1}$ the small angle approximation yields

$$\text{FSR}_t \approx R_D C_D \quad (4.8)$$

and the FSR is independent of frequency.

The precision of the timing adjustment can be found by determining the change in delay versus the control $A = A_Q/A_I$ (4.7)

$$\frac{\delta\Delta t}{\delta A} = \frac{R_D C_D (1 + \omega^2 R_D^2 C_D^2)}{(1 + \omega^2 R_D^2 C_D^2 A)^2 + \omega^2 R_D^2 C_D^2 (A - 1)^2} \quad (4.9)$$

Insight into (4.9) can be obtained by evaluating at $A = 0$ and $A = 1$.

$$\left. \frac{\delta\Delta t}{\delta A} \right|_{A=0} = R_D C_D \quad (4.10)$$

$$\left. \frac{\delta\Delta t}{\delta A} \right|_{A=1} = \frac{R_D C_D}{1 + \omega^2 R_D^2 C_D^2} \quad (4.11)$$

At $A = 0$, the timing precision is independent of frequency and increases linearly with $R_D C_D$. However, for $A = 1$ and $\omega^2 R_D^2 C_D^2 \gg 1$, the precision decreases with frequency. If $R_D C_D$ becomes too large, $\delta\Delta t/\delta A$ tends toward zero, rendering the upper portion of the control range ($A \rightarrow 1$) ineffective. Therefore, the choice of $R_D C_D$ is a tradeoff between FSR_t and diminishing returns on circuit complexity. A reasonable choice is to let the maximum frequency of operation $\omega_m \approx (R_D C_D)^{-1}$ such that

$$\left. \frac{\delta\Delta t}{\delta A} \right|_{A=1} = 0.5 \left. \frac{\delta\Delta t}{\delta A} \right|_{A=0} \quad (4.12)$$

and

$$FSR_t \Big|_{\omega=\omega_m} = \frac{\pi}{4\omega_m} \quad (4.13)$$

Figure 4.8 shows the implementation of the local RZ clock driver circuit. The input of the local RZ driver includes two stages of emitter-followers, the first biased by an offset compensation circuit to alleviate duty cycle mismatch which, as shown by (2.3), manifests as an amplitude mismatch for the cell. The following stage implements the 5-bit programmable delay. The weighted sum is achieved via switched resistors to

control the bias current of two differential pairs, exploiting the linear relationship between bias current and HBT g_m . The programmable resistors for the in-phase and quadrature paths are switched in opposite directions such that the sum of the two amplifier currents is constant, resulting in a stable output swing across control value. Finally, the RZ output stage uses a Cherry-Hooper amplifier to ensure sharp edges for the RZ switches of the unit cell.

Figure 4.11 shows a transient simulation of the local RZ clock driver at 20 GHz, exhibiting a peak amplitude of about 350 mV and full-scale control range of 4.5 ps. A worst-case precision of 200 fs, meeting the 3σ requirement of 225 fs. Additionally, the circuit maintains an edge rate independent of control value, ensuring that all cells exhibit identical switching speeds. In Figure 4.12 the delay for each control and m_{rz} setting is shown. Across m_{rz} , the FSR ranges from 3.9 ps to 5.5 ps. Fortunately, the lower end of that range corresponds to $m_{rz} = 1$, where timing calibration is less critical to SFDR performance.

In addition to the static mismatch within the DAC cell, it is important that the FSR accounts for the delay mismatch in the clock driver itself. Figure 4.13(a) shows a MC simulation of the driver with the control value set to the middle of the full scale range (with $m_{rz} = 6$). The local driver delay varies by < 1 ps, leaving > 3.5 ps remaining to calibrate the static mismatches within the clock routing, output node, and current cell. Figure 4.13(b) shows a MC simulation of the duty cycle, exhibiting less than 0.7% variation which corresponds to 0.06 dB of attenuation mismatch which can be subsequently mitigated using the amplitude calibration circuitry.

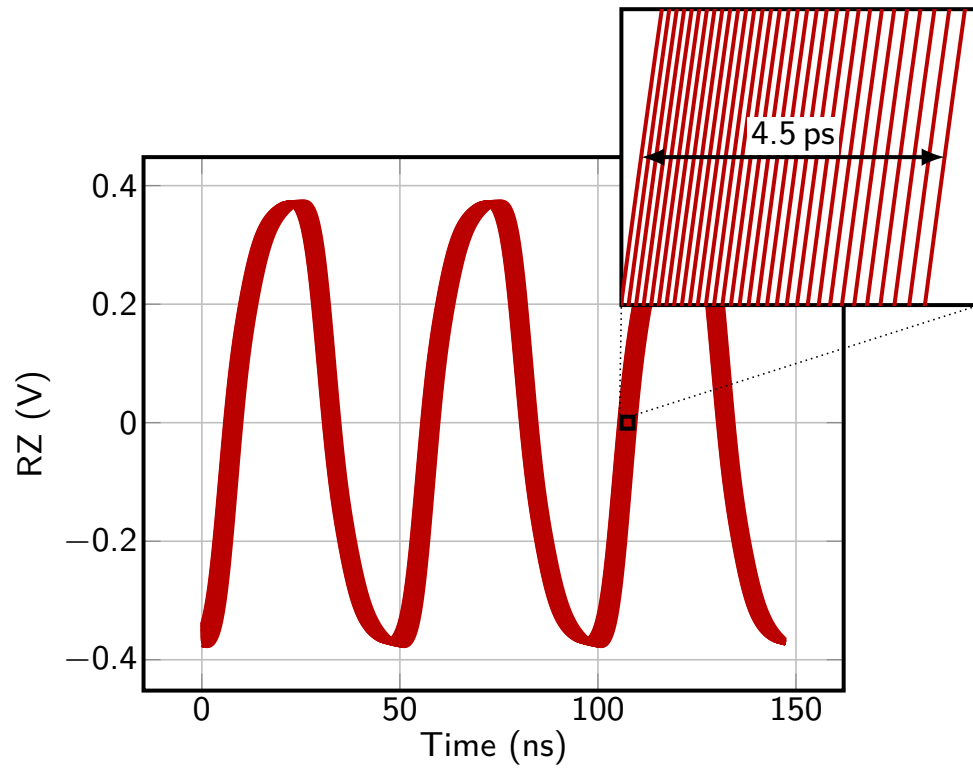


Figure 4.11: Transient simulation of the local RZ clock driver circuit for each control value

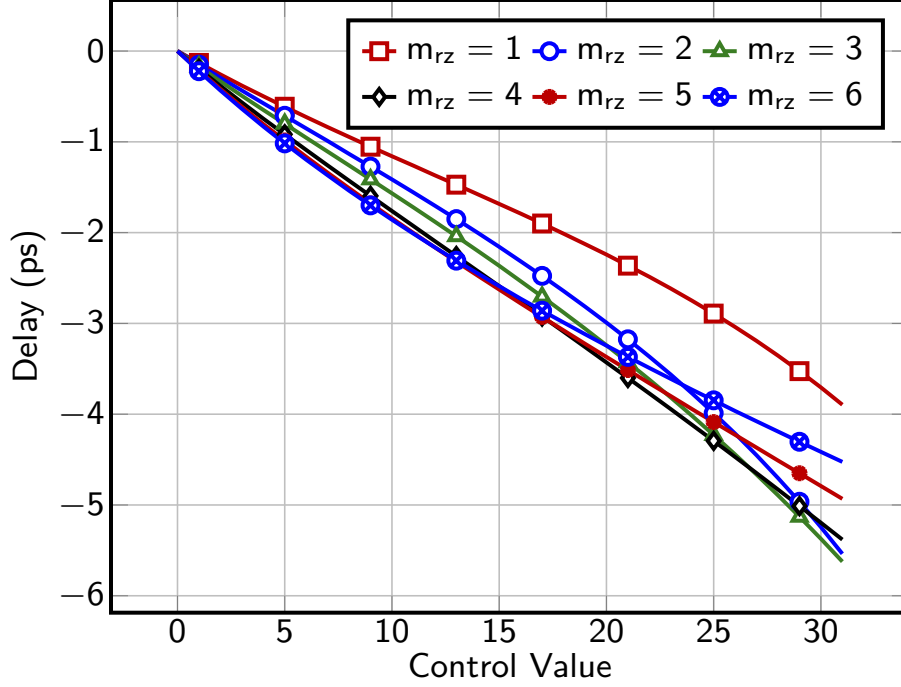


Figure 4.12: Delay of the local RZ clock driver for various control values

4.3.3 Amplitude Calibration

In addition to the timing calibration, the DAC also faces demanding requirements on amplitude matching between cells. A Monte Carlo simulation of a behavioral model of the DAC with static current mismatch is shown in Figure 4.14, which plots the 97.7% yield line using a 95% confidence level. As expected, static current mismatch has the same impact at both $m_{rz} = 1$ and $m_{rz} = 6$. A mismatch of $\sigma_I/I_{MSB} < 0.1\%$ is required to obtain an SFDR of about 70 dB. To achieve this within a reasonable area, the CMOS current source is designed for a 0.3% mismatch, while a 9-bit calibration DAC, shown in Figure 4.8, is used to fine tune the current of each cell. The calibration DAC has a FSR of 10% of the primary cell current to account for mismatches in the current source, base currents in the data and RZ switches, and RZ clock duty cycle.

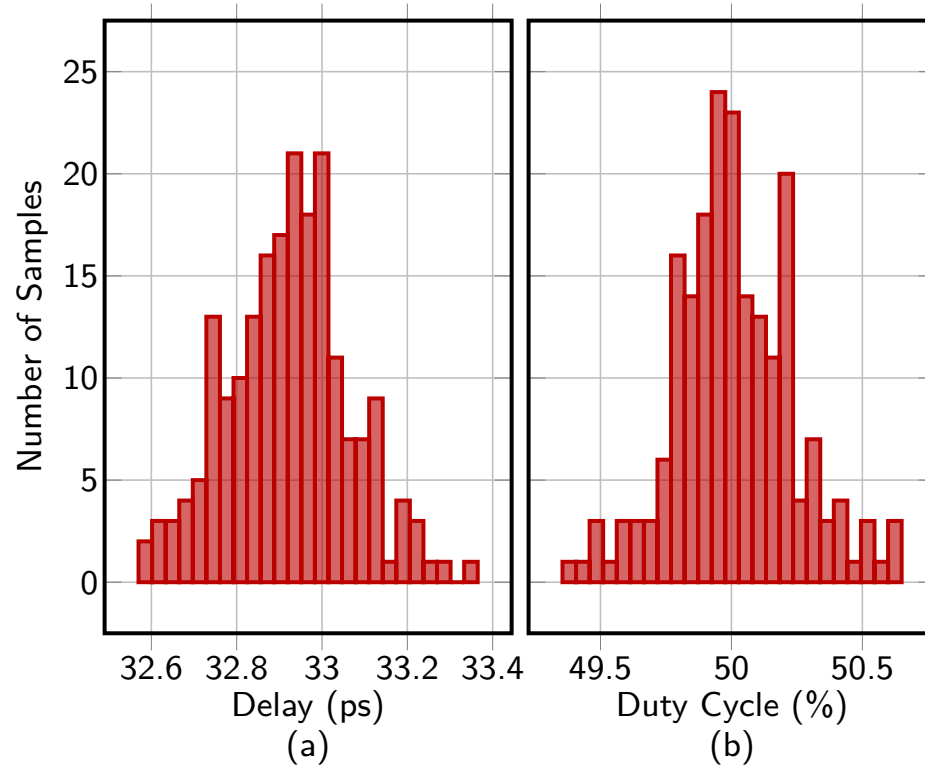


Figure 4.13: Monte Carlo simulation of the (a) delay and (b) duty cycle of the local RZ clock driver

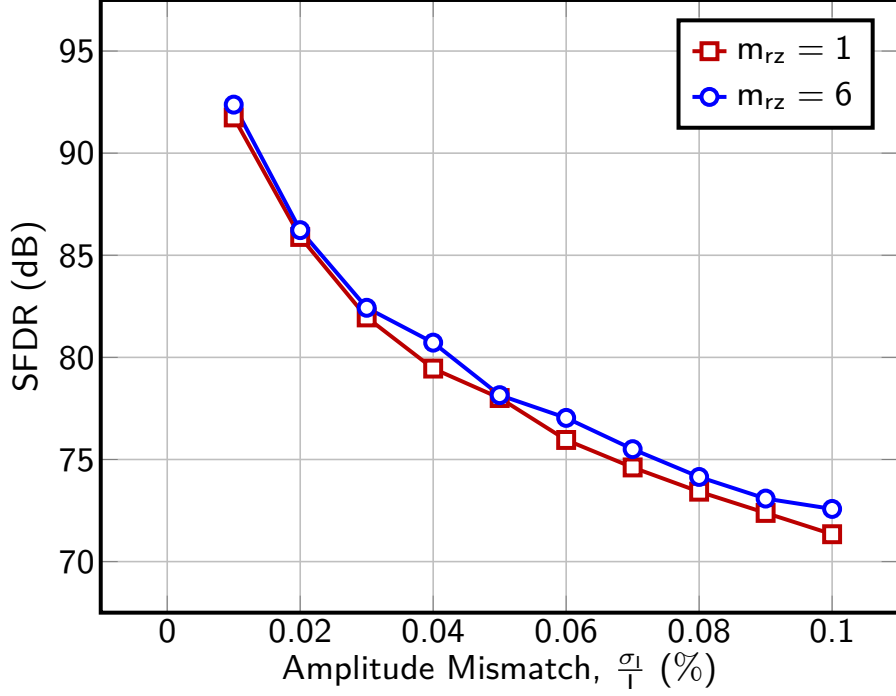


Figure 4.14: Behavioral simulation of static amplitude mismatches

4.3.4 The Data Path

A primary benefit of the MRZ architecture is the relaxation of deterministic jitter requirements in the data path. As long as the peak-to-peak deterministic jitter is less than the width of the RZ pulse, the output will be largely unaffected. The data path, shown in Figure 4.8, includes a CMOS D-type retiming flip-flop (RTFF) to synchronize the data arriving to each cell. The CMOS architecture allows for the use of CMOS levels for DCLK, resulting in significant power savings for both the RTFF and clock distribution by avoiding current-mode logic circuits [23]. The flip-flop is followed by a data driver, implemented as a Cherry-Hooper limiting amplifier, that

level-shifts the data and ensures that the input to the data switches fully transitions within the RZ clock pulse.

4.3.5 Layout Considerations

At an operating frequency of 20 GHz, the layout of the DAC core, shown in Figure 4.15, plays an important role in its performance. The unit cell array comprises 25 active current cells and 7 dummy cells, each with a width of $25\text{ }\mu\text{m}$. The total of 32 cells allows for balanced clock distribution trees to minimize timing errors. The CMOS current source and calibration DAC are located outside of the cell array to allow for compact interdigitation with matched routing to each cell to minimize drain-induced current variations. Decoupling capacitors are distributed throughout each unit cell to minimize deterministic jitter induced by cell-dependent supply and bias variations.

4.4 Measurement Results

The 10-bit MRZ DAC has been fabricated in a $0.13\text{ }\mu\text{m}$ SiGe BiCMOS process. The chip, pictured in Figure 4.16, measures $2.5\text{ mm} \times 2.5\text{ mm}$ and integrates 10 LVDS data channels, the MRZ DAC with VST and feedforward network, and a digital SPI control for the calibration settings. Table 4.1 summarizes the power consumption of the major circuit blocks in the DAC, which consumes a total of 1.91 W. The primary consumers of power are the 20 GHz RZ drivers, which utilize nearly 60 % of the total due to the elevated power supply and current required to obtain sufficient high-frequency performance.

The DAC is mounted in a wafer probe station and interfaced to the test equipment via a probe card. The test setup, shown in Figure 4.17, utilizes an Agilent 81250

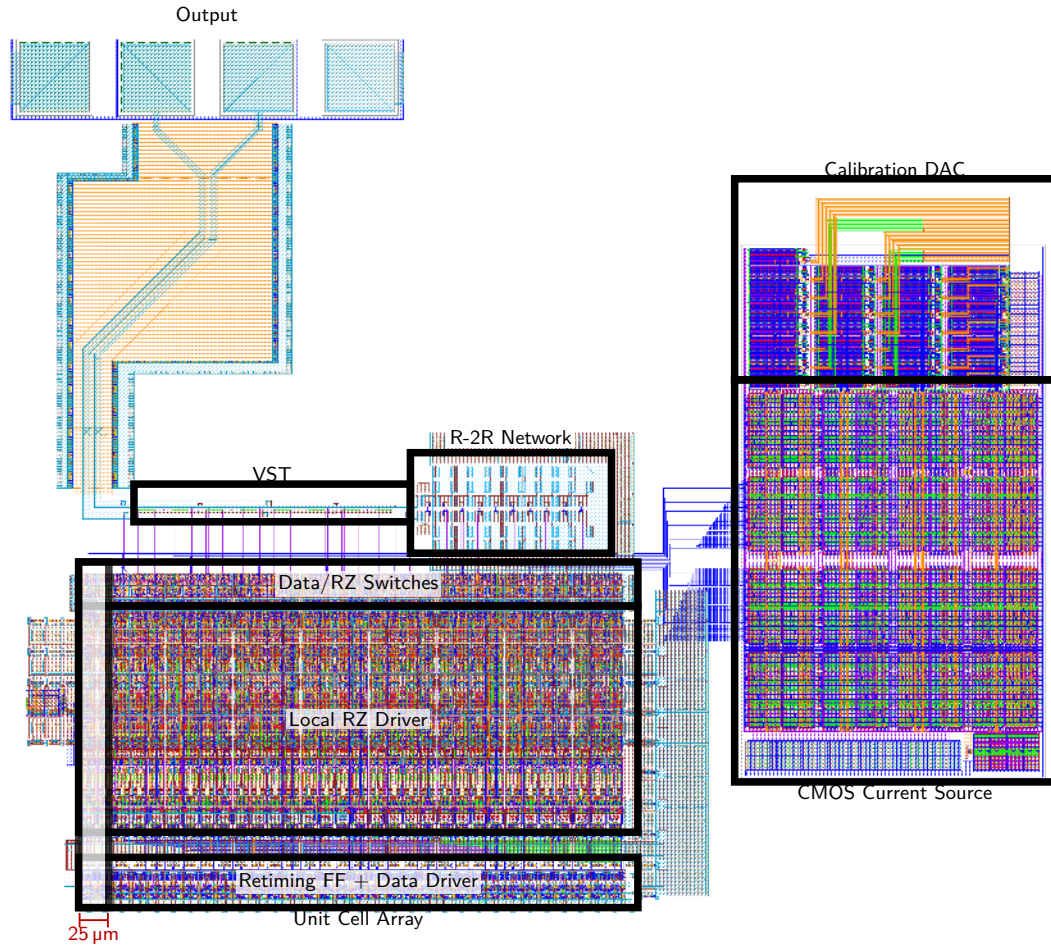


Figure 4.15: Layout of the DAC core

Table 4.1: Power consumption of circuit blocks in the DAC

Circuit	Supply (V)	Power (W)
Current Cells	3.5	0.10
Data Drivers	2.0	0.28
RZ Drivers	4.0	1.12
Digital	1.5	0.41
Total		1.91

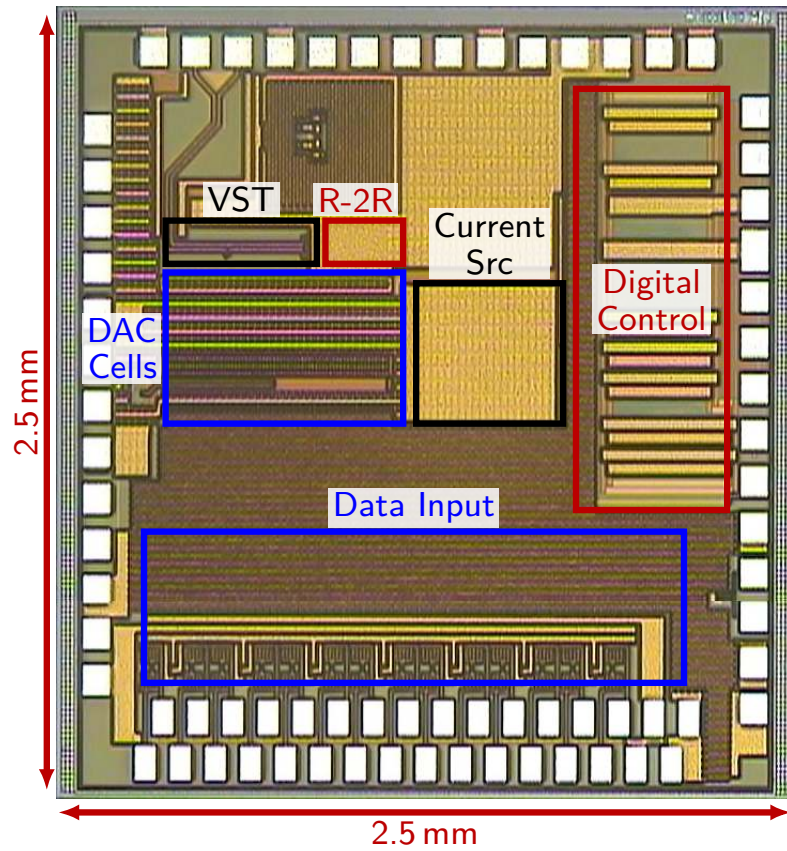


Figure 4.16: Photograph of the DAC chip

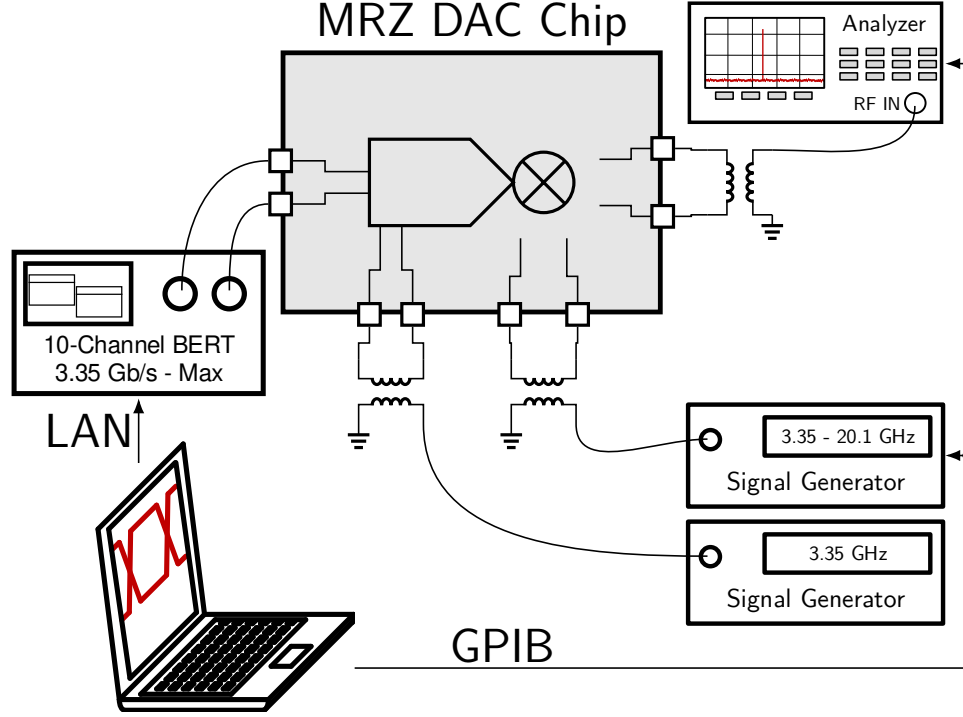


Figure 4.17: Test setup for the DAC chip

ParBERT to feed 10-bit 3.35 GS/s data to the DAC. The data and RZ clocks are generated and aligned by two Agilent E8367D signal generators. Three baluns are used to perform differential to single-ended conversion for the DAC output and clocks. To cover the the full frequency range from DC to 20 GHz, three balun variants are required: Picosecond Pulse Labs 5310A, Narda 4346, and a Krytar 4060265.

The calibration is performed externally using the spectrum analyzer as the measurement device and is controlled via Python scripts on a laptop with GPIB and LAN control of the test equipment. Amplitude measurements are obtained by applying a square wave to one bit at a time and measuring the amplitude of the fundamental component. To calibrate timing errors, successive coarse and fine searches through

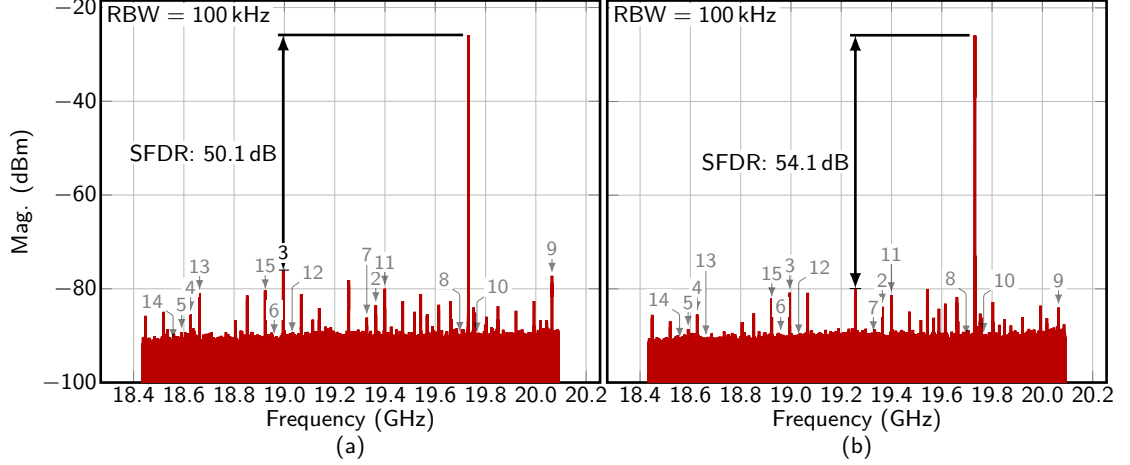


Figure 4.18: Measured single-tone spectrum for a signal in the 12th Nyquist zone ($m_{rz} = 6$) (a) before and (b) after calibration. Spurs from the first 15 harmonics are labeled. Losses from the measurement setup are included.

the delay control values for each bit are performed to optimize SFDR at a single frequency point. The DAC is calibrated once in each Nyquist zone to properly account for frequency-dependent amplitude and timing variations.

Figure 4.18(a) shows the output of the DAC prior to calibration for a single-tone input in the 12th Nyquist zone ($m_{rz} = 6$, $f_{rz} = 20.1$ GHz), including losses in the measurement setup. At this frequency, the DAC exhibits an SFDR of 50.1 dB and is dominated by images of the 3rd and 9th harmonics. Figure 4.18(b) shows the single-tone spectrum after calibration, giving a significant reduction in all of the odd-order spurs for a 4 dB improvement in SFDR. The post-calibration dominant tone is unrelated to any harmonic image, and therefore is likely the result of a more complex error mechanism such as a mixing product due to coupling of internal DAC nodes to the RZ clock .

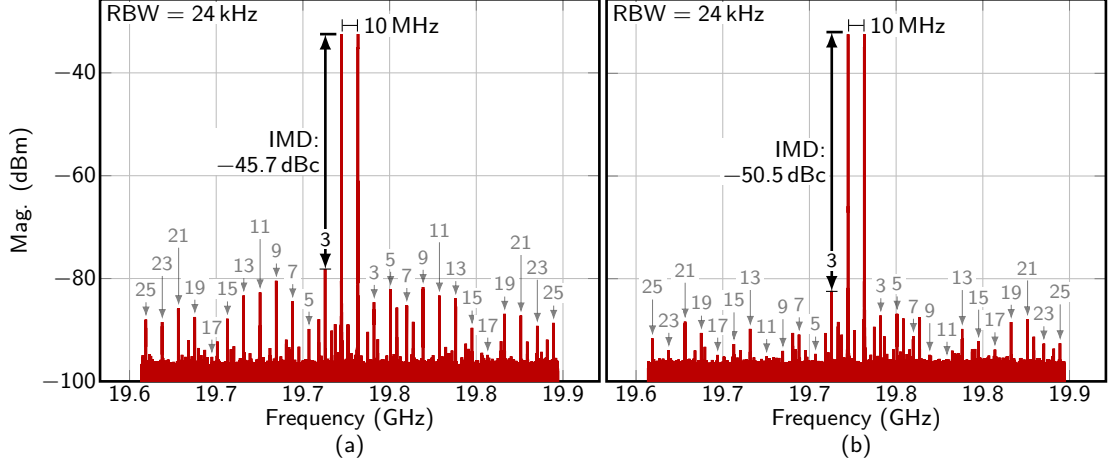


Figure 4.19: Measured two-tone spectrum for a signal in the 12th Nyquist zone ($m_{rz} = 6$) (a) before and (b) after calibration. The first 25 intermodulation products are labeled. Losses from the measurement setup are included.

Figure 4.19(a) shows the output of the DAC prior to calibration for a two-tone input with a 10 MHz spacing in the 12th Nyquist zone, including losses in the measurement setup. The uncalibrated DAC exhibits an IMD of -45.7 dBc, dominated by the 3rd-order product. After calibration, the two-tone spectrum, shown in Figure 4.19(b), exhibits a significant reduction in all intermodulation products, resulting in a 4.8 dBc improvement resulting in an IMD of -50.5 dBc.

The DAC is provided with inputs ranging from DC to $0.4f_s$ with the RZ clock swept from $m_{rz} = 1 \dots 6$ to output frequencies up to the 13th Nyquist zone. Figure 4.20 shows the simulated and measured output power (P_{OUT}) of the DAC. The simulation uses an RC extracted model of the full DAC cell array including the power, clock distribution, and output pads. Losses in the cables, connectors, and baluns in the setup are measured with a network analyzer and de-embedded from the output power results. The measured output power exhibits a variation of about 4 dBm within

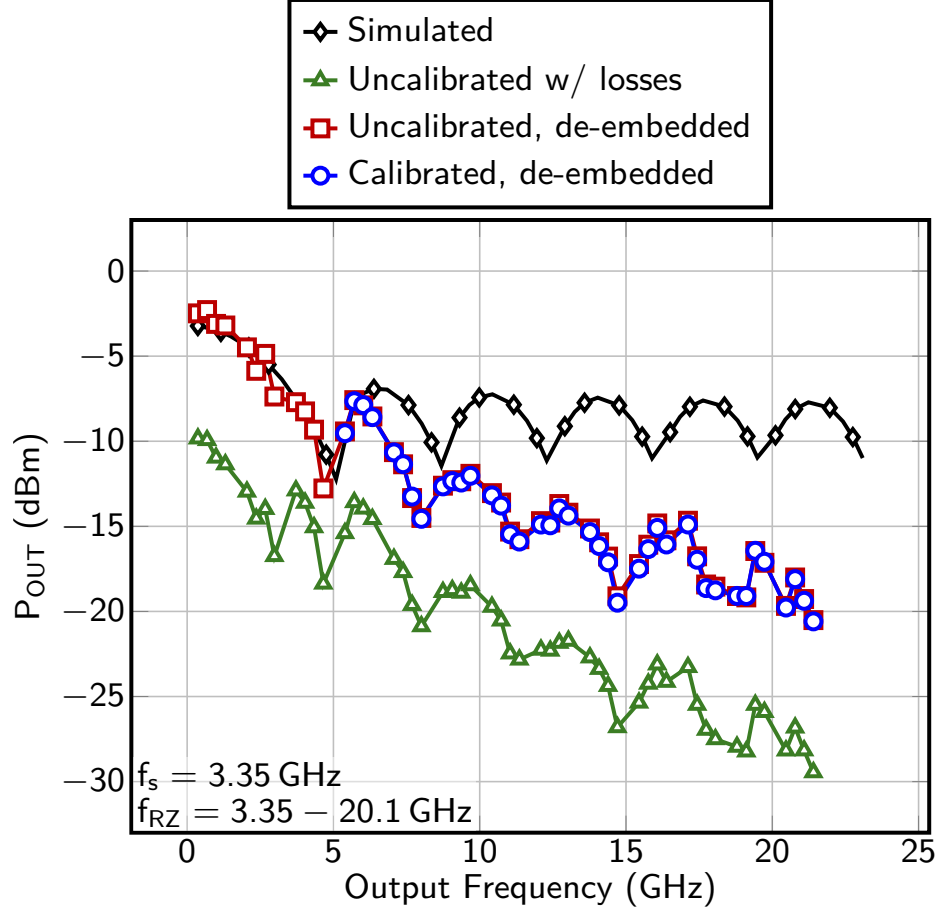


Figure 4.20: Measured output power for signals swept through the first 13 Nyquist zones ($m_{rz} = 1 \dots 6$). Simulation include an RC extracted model of the full DAC cell array and output node

each Nyquist zone with a peak power of -3 dBm at DC, closely matching simulated results. At 20 GHz, the measured power falls about 8 dBm below simulation to a -18 dBm. This discrepancy is primarily a combination of the inability to de-embed some parts of the measurement setup such as the probes (up to 1 dB), probe card, and spectrum analyzer frequency response (up to 3 dB), as well as the neglected inductance in the RC extracted model.

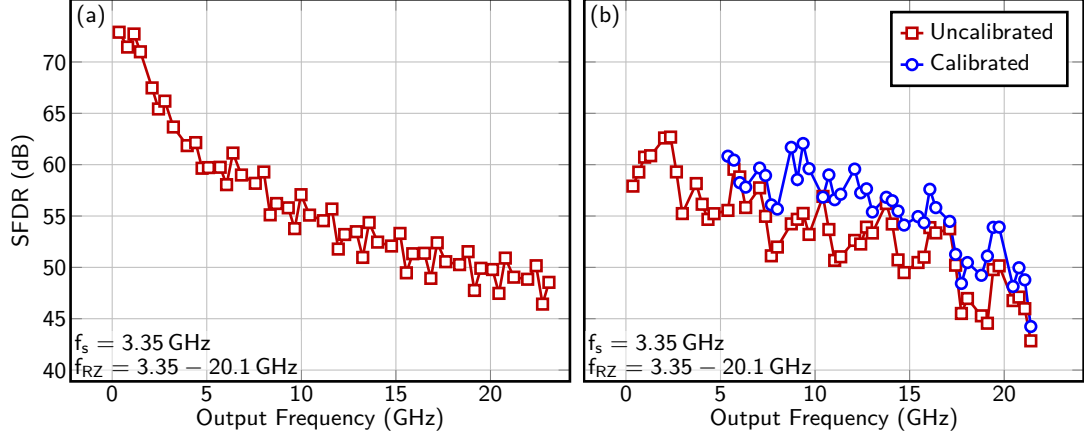


Figure 4.21: Measured SFDR for signals swept through the first 13 Nyquist zones ($m_{rz} = 1 \dots 6$). Simulations include an RC extracted model of the full DAC cell array and output node

Figure 4.21(a) and Figure 4.21(b) show the simulated and measured SFDR, respectively. The simulated SFDR ranges from 72 dB at DC to 47 dB at 20 GHz. The measurement results give a maximum SFDR of 63 dB at low frequencies, resulting in a large discrepancy due to the absence of device mismatches in the simulation. At 10 GHz and above, the measured DAC exhibits an SFDR greater than 45 dB and matches within 5 dB of simulation. It is worth noting that the VST and feedforward network allow the uncalibrated DAC to achieve 4 dB better SFDR at 20 GHz than an ideal DAC with a TTL and ideal timing compensation (Figure 4.2). Calibration results in up to 7 dB improvement across frequency, giving greater than 48 dB SFDR from DC to 20 GHz. Figure 4.22 shows the measured IMD across frequency before and after calibration. Prior to calibration, a worst-case IMD of -42 dBc is observed. Calibration provides up to 6 dBc improvement in IMD, yielding better than -46 dBc up to 20 GHz.

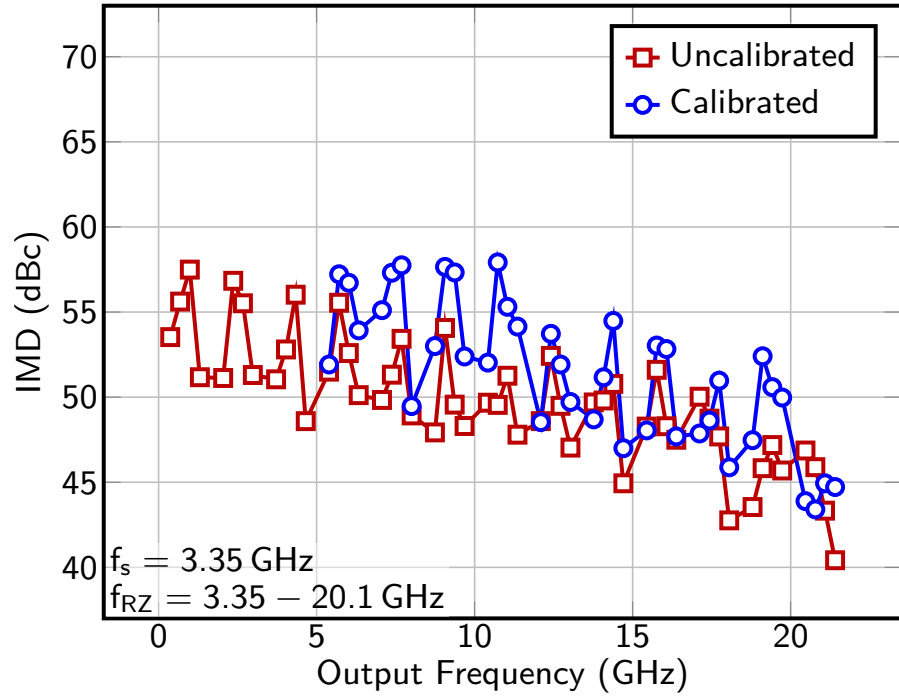


Figure 4.22: Measured IMD for signals swept through the first 13 Nyquist zones ($m_{rz} = 1 \dots 6$)

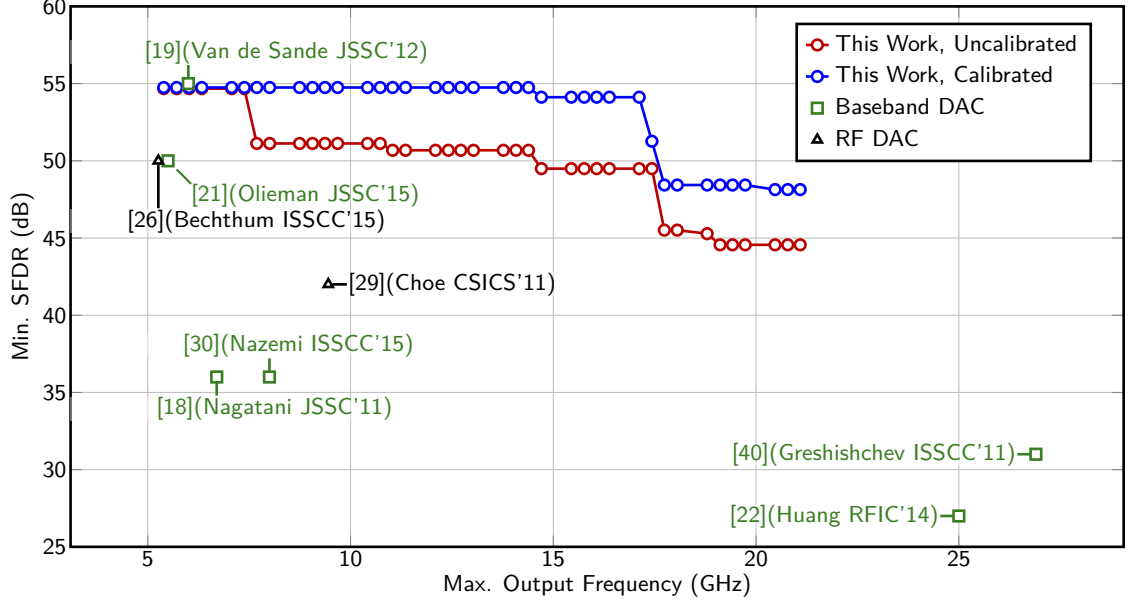


Figure 4.23: SFDR comparison with recently published DACs

Figure 4.23 and Table 4.2 show a comparison with DACs that report SFDR above 5 GHz. Three of the reported DACs achieve SFDR over 50 dB across the Nyquist zone, however, the output frequencies of these designs are limited to less than 6 GHz [19, 21, 26]. In [29], the SFDR drops to 42 dB at 10 GHz. The implemented DAC achieves >48 dB SFDR up to 20 GHz where other reported DACs are limited to 31 dB [22, 40]. Furthermore, the highest sample rate, and hence the largest synthesizable bandwidth, is achieved among RF DACs [26, 29].

4.5 Conclusion

A 10-bit multiple-return-to-zero DAC is presented in this work, demonstrating > 48 dB SFDR from DC to 20 GHz. The DAC utilizes a vertically-stacked summing node structure and capacitive feedforward network which significantly improves the

Table 4.2: Performance comparison with recently published DACs

	This	[40]	[22]	[29]	[30]	[18]	[19]	[21]	[26]
Tech. [nm]	130	65	28	500	28	1000	130	28	65
	BiCMOS	CMOS	CMOS	InP	CMOS	InP	BiCMOS	CMOS	CMOS
Resolution [bits]	10	6	8	12	8	6	12	9	16
P _{wr} [W]	1.91	0.75	2.5	1.6	0.144	0.95	8.3	0.11	0.38
P _{out} [dBm]	-18	-3.5	-5	-15	-0.97	-10	1	-6.5	-8
f _s [GS/s]	3.35	56	100	2.7	18	28	12	11	1.75
f _{out} [GHz]	20.0	26.9	25	9.45	8	6.7	6	5.5	5.26
Min. SFDR [dB]	48	31	27	42	36	36	55	50	50
IMD [dBc]@[GHz]	46@20	—	—	—	—	—	—	51@5.5	58@5

matching in attenuation and phase between each cell and the output, yielding a 21 dB improvement in SFDR over the conventional TTL summing node. Moreover, the improved summing node enables the use of SiGe HBTs within the unit current cells, despite their large footprint. Additionally, the DAC utilizes per-cell amplitude and timing calibration circuitry to correct any remaining deterministic errors as well as additional errors induced by random process mismatches. The DAC is implemented in a 0.13 μm SiGe BiCMOS technology and achieves more than 48 dB SFDR and -46 dBc IMD from DC to 20 GHz after calibration with an instantaneous bandwidth of up to 1.675 GHz. Compared to recently reported DACs, the highest linearity performance above 6 GHz is achieved, while supporting the largest instantaneous bandwidth among the RF DACs.

Chapter 5: Conclusion

This work describes the analysis and design of GHz and mm-wave digital-to-analog converters which will be critical to the next generation of software-defined and cognitive radios. A new approach to SFDR analysis has been developed in which the contribution of each individual cell is analyzed and errors are applied as transfer functions in the frequency domain. Unlike the conventional analysis, the frequency-domain approach works well with the small-signal models produced by EM simulations, enabling the incorporation of complex output summing node structures with little impact to simulation time and convergence.

The frequency-domain analysis was then applied to a DC-20GHz multiple-return-to-zero DAC to achieve state-of-the-art linearity performance. The DAC utilizes a vertically-stacked summing node structure and capacitive feedforward network which significantly improves the matching in attenuation and phase between each cell and the output, yielding a nearly 19 dB improvement in SFDR over the conventional TTL summing node. Furthermore, the DAC utilizes per-cell amplitude and timing calibration circuitry to compensate for random process mismatches. The calibrated design achieves more than 48 dB SFDR from DC to 20 GHz with an instantaneous bandwidth of up to 1.675 GHz.

5.1 Future Work

Although this work has provided significant advancement to the development of GHz and mm-wave DACs, a significant amount of research remains in the journey towards high-frequency software-defined radios. This research should focus on both continued improvement to the DAC linearity as well as the enhancement of other features beneficial to the SDR system such as high output power and the suppression of signal images.

5.1.1 Process Scaling

The proposed design achieves state-of-the-art performance in a relatively old 0.13 μm SiGe BiCMOS process. Today, a 90 nm SiGe BiCMOS process exists, and scaling trends will ensure that even smaller processes will soon be available. Such scaling has the potential to dramatically decrease the power consumption of the DAC. In addition power reduction in the supporting CMOS circuitry, even a small improvement to the 20 GHz local RZ clock drivers will yield substantial power savings. Moreover, CMOS process scaling could even enable a CMOS implementation of much of the RZ clock path with the potential to reduce power by an order of magnitude.

5.1.2 High-Power Output

As discussed in Section 1.3, an SDR using the proposed DAC will require a power amplifier. The measured output power of -18 dBm at 20 GHz is simply not enough to directly drive the antenna. Although this can be achieved by increasing the current of the unit cells, such a change is accompanied by many challenges. Namely, the increased output swing will lead to more coupling between the output and internal

DAC nodes, leading to an increase in deterministic jitter. This is particularly troublesome as the techniques discussed in this thesis focus on static errors and depend on the MRZ architecture to mitigate the effects of deterministic jitter. Therefore, improvements to the MRZ architecture will be required to further isolate these internal nodes from the output. Additionally, the injection of larger switching transients on the power supply will further complicate the power supply routing and decoupling.

5.1.3 Anti-Alias Filtering

A critical component to the SDR which has yet to receive much attention is the filter at the output of the DAC. While the design minimizes spurious emissions within the Nyquist zone, a large amount of emissions remain in the images that arise from sampling. The design of the anti-aliasing filter is no small task; it will need to have a configurable pass band along with a sharp transition from the pass band to the stop band to maximize the usable portion of the Nyquist zone. Moreover, the filter must preserve the linearity performance of the DAC which will become even more challenging as the DAC output power increases.

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