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A 10 MHz GaNFET Based Isolated High Step-Down DC-DC Converter: Design and Magnetics Investigation

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***Abstract*— This paper presents design of an isolated high-step-down DC-DC converter based on a class-DE power stage, operating at a 10 MHz switching frequency using enhancement mode Gallium Nitride (GaN) transistors. The converter operating principles are discussed, and the power stage design rated for 20 W is presented for a step-down from 200-300 V to 0-28 V. Commercially available magnetic materials were explored and the high-frequency (HF) resonant inductor and transformer designs using a low-loss Fair-Rite type 67 material are presented. Finite element simulations have been performed to estimate the parameters of magnetics at 10 MHz. Experimental results are presented at 12 W, 254 V to 22 V and 5 W, 254 V to 14 V on a laboratory prototype operating at 10 MHz. At 20 W the experimental prototype achieved an efficiency of 85.2%.**

Keywords*— *DC-DC conversion, Gallium Nitride, High frequency, Resonant conversion, Soft switching, Class-DE, Finite-element modeling

I. INTRODUCTION

The motivation to operate at high switching frequency is not just to reduce the size of passive components but also to provide very fast dynamic load response. Most RF communication systems use power amplifiers (PA) to convert low-power signals into larger power RF signals for driving the antenna of a specific transmitter. The majority of PA designs utilize switched-mode pulse-width-modulating (PWM) converters as the power source to operate RF amplifiers. Envelope tracking PAs use dynamically changing supply voltage to achieve high efficiency for the PA over the full power range. To achieve successful envelope tracking, the power supply must be capable of switching at frequencies greater than 5 MHz, as most modern RF waveforms observe a bandwidth of 1 to 5 MHz [1], [2].

The envelope tracking power supply considered in this paper has to operate with an input voltage range of 200 V to 300 V at 10 MHz switching frequency. Several designs at 10 MHz switching are reported in literature for different applications. A 10-MHz GaN 16 to 34-V boost converter with above 90% efficiency is presented in [3]. A 94% efficient 10-MHz, 100 W buck-boost type DC-DC converter is studied in [4]. A 10 MHz, 10.8-16 V to 0.65-2 V, 2 A multiphase buck converter is implemented in [5]. A 10-MHz, 12 V to 5 V, 5 W buck converter is investigated in [6]. All of these designs are at low operating voltage (few tens of volts).

Traditional hard switching switched-mode power supply (SMPS) topologies are extremely lossy at such high frequencies. This has led to the development of resonant soft-switching converters. With the emergence of Gallium Nitride (GaN) based power switches, power electronic converters tend to be even faster, smaller and more efficient [7]. Resonant converters are often designed in two parts; an inverter converting the DC input voltage to an AC current and a rectifier converting the AC current to a DC output voltage. The two parts are designed individually, but the design of the inverter depends on the input impedance of the rectifier [8], [9].

The most common topologies for the inverter part are based on class E, which could either be a class E, a class EF2 (φ2), a resonant SEPIC or a resonant boost converter. The choice of the topology is based on the complexity and losses associated with a high-side gate drive for operation in the HF range. A class E derived inverter imposes significant voltage stress across the MOSFET. The voltage stress for the class E, the resonant SEPIC and resonant boost is 3.6 times the input voltage with a duty cycle of 50%, and for the class EF2 this stress is reduced to approximately 2.3-3 times. The semiconductor switches in the class DE inverter are directly connected to the input and the voltage across them is limited to the input voltage. The class DE inverter [10]-[12] has two other great advantages over the other topologies. Firstly, it only requires a single inductor. Secondly, due to the lower peak voltage across the MOSFET, the stored energy is approximately ten times lower, compared to aforementioned topologies. But the need for high side gate driver increases the complexity.

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Avoiding high di/dt and dv/dt can help to reduce EMI at the source. Soft-switching resonant topologies usually have lower EMI than hard-switching converters. The time domain characteristics of trapezoidal and S-shaped switching transitions are reported in [13]. The S-shaped transitions seen in the switch node voltages (Fig. 4) have lower high-frequency harmonic content. The slew rate of the voltage transition is relatively low (compared to the high switching frequency used here) due to slow switching transition and large dead-time used on the high-voltage bridge GaNFETs. The dead-time used here is 32% of the period which is significantly large compared to conventional design approaches. This large dead-time also reduces the energy required in the resonant tank for discharging the output capacitance C_{oss} of the GaNFETs. This paper presents a GaN-based and magnetic core-based 10 MHz isolated DC-DC converter using a Class-DE resonant soft-switching power stage [14]. Section II describes the converter operation, design and simulation results. Section III discusses the choice of 10 MHz magnetics, and the design of inductor and transformer using Fair-Rite 67 material. Section IV provides the experimental results, and Section V discusses the power loss distribution, followed by the conclusions in Section VI.

II. Resonant Converter Analysis and Design

A. Converter analysis

A class-DE based isolated DC-DC converter is depicted in Fig. 1. The main input power stage consists of switches S_1 and S_2. Compared to the conventional Class-DE amplifiers, additional switches S_3 and S_4 are connected in parallel with the rectifier diodes D_3 and D_4, to achieve synchronous rectification and also for active rectification to control the output voltage and power. The converter achieves ZVS, zero voltage derivative switching (ZVDS), and ZCS at the turn-on instant. In this converter, the effective impedance of the secondary rectifier is used for designing the series resonant tank components C_r and L_r. A transformer with a turns ratio n is used for providing isolation as well as stepping down the input voltage. The power is transferred from input to output due to the resonance between the resonant tank elements C_r and L_r. Hence, the current flowing through the resonant tank is almost sinusoidal in shape. Based on the fundamental harmonic approximation (FHA), the ac-equivalent circuit of the proposed Class-DE DC-DC converter is shown in Fig. 2.

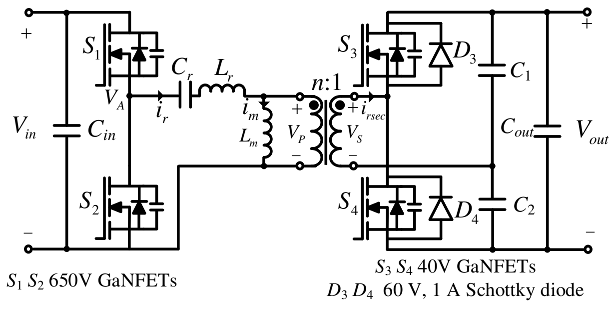

Fig. 1. Schematic of the Class-DE based isolated synchronous DC-DC converter.

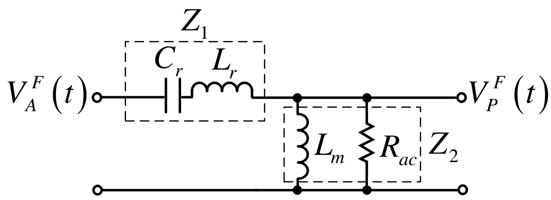

Fig. 2. AC equivalent circuit of the resonant tank based on FHA.

The design equations of the proposed isolated class-DE topology are given below. The AC equivalent load resistance (input resistance of the rectifier) is calculated as [10]

$$R_{ac} = \frac{2R_L n^2}{\pi\left[\pi + \omega R_L C_{oss,sec}\right]} . \tag{1}$$

where $\omega = 2\pi f_{sw}$, R_L is the load resistance, n is the transformer turns ratio, f_{sw} is the switching frequency, and $C_{oss,sec}$ is the output capacitance of the secondary GaNFETs S_3 and S_4.

The RMS switch-node voltage on inverter side with respect to negative rail is given by (assuming trapezoidal waveform) [12]

$$V_{A,RMS} = V_{in}\sqrt{\frac{D_{pri}+1}{3}} , \tag{2}$$

Similarly, the RMS switch-node voltage on rectifier side with respect to negative rail, and referred to primary side is given by

$$V_{P,RMS} = V_{out} n\sqrt{\frac{D_{sec}+1}{3}} , \tag{3}$$

where D_{pri} and D_{sec} are the duty cycles of primary and secondary GaNFETs, respectively.

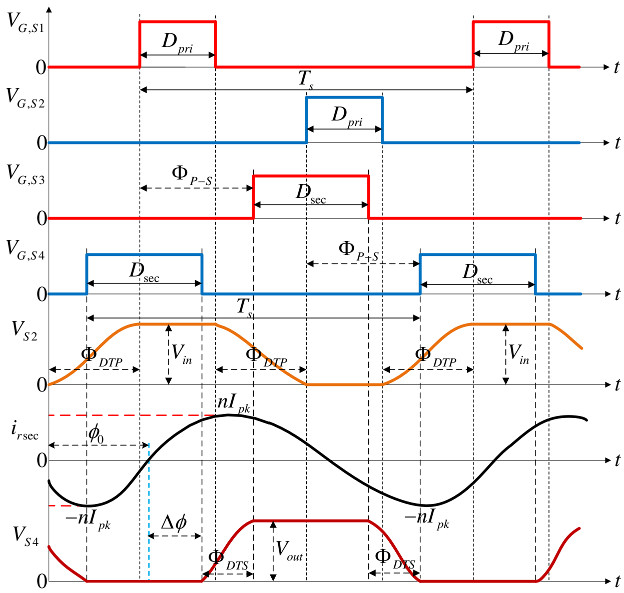

Fig. 3. Steady-state waveforms of the proposed resonant DC-DC converter.

The series component Z_1 (in Fig. 2) of the resonant circuit performs multiple functions: It provides dc blocking, and also forms an impedance divider that controls the AC power delivered to the resistive load. Z_1 is calculated using the similar concept provided in [15] with an assumption that the AC power is delivered to the load only at the fundamental of the switching frequency.

The impedances Z_1 and Z_2 are given by

$$Z_1 = Z_2\sqrt{\left(\frac{V_{A,RMS}}{V_{P,RMS}}\right)^2 - 1}\ , \tag{4}$$

$$Z_2 = \frac{\omega L_m R_{ac}}{\omega L_m + R_{ac}}\ . \tag{5}$$

where L_m is the primary magnetizing inductance of the transformer.

The resonant tank inductance L_r for a given tank capacitance C_r is calculated as [16]

$$L_r = \frac{C_r Z_1 \omega + 1}{C_r \omega^2}\ . \tag{6}$$

The quality factor Q of the resonant tank is given by

$$Q = \frac{1}{R_{ac}}\sqrt{\frac{L_r}{C_r}}\ . \tag{7}$$

Based on the FHA, the fundamental components of the input and output voltages of the resonant tank (by approximating the trapezoidal switch-node waveforms to square wave signals) are given by

$$V_A^F(t) = \frac{V_{in}}{\pi}\left[1 - \cos\left(2\pi D_{pri}\right)\right]\sin\left(\omega t\right), \tag{8}$$

$$V_P^F(t) = \frac{nV_{out}}{\pi}\left[1 - \cos\left(2\pi D_{sec}\right)\right]\sin\left(\omega t\right). \tag{9}$$

The voltage gain of the resonant tank is given as follows:

$$M = \frac{V_P^F(t)}{V_A^F(t)} = \frac{nV_{out}}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}\ , \tag{10}$$

The resonant tank gain M in terms of all circuit variables is given by [17]

$$M = \frac{k}{\sqrt{\left(1 + k - \frac{1}{f_n^2}\right)^2 + Q^2 k^2\left(f_n - \frac{1}{f_n}\right)^2}}\ . \tag{11}$$

where k is the inductance factor, f_r is the resonant frequency, and f_n is the normalized frequency $k = \frac{L_m}{L_r}$, $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, $f_n = \frac{f_{sw}}{f_r}$.

The steady state waveforms of the proposed DC-DC converter are shown in Fig. 3. The gate drive waveforms of the four primary and secondary GaNFETs, the voltages across the GaNFETs S_2 and S_4, and the secondary resonant tank current are clearly shown in Fig. 3. The switching frequency of the converter is fixed at 10 MHz.

The output power of the converter is defined as [10], [18]

$$P_{out} = \left(\frac{nI_{pk}\cos\left(\Delta\phi\right)}{\pi + \omega R_L C_{oss,sec}}\right)^2 R_L\ . \tag{12}$$

The output current is given by the following expression

$$I_o = \frac{nI_{pk}\cos\left(\Delta\phi\right)}{\pi + \omega R_L C_{oss,sec}}\ . \tag{13}$$

The phase shift $\Delta\phi$ is given by

$$\Delta\phi = \left(\Phi_{P-S} - \Phi_{DTS}\right) - \left(\phi_0 - \Phi_{DTP}\right)\ , \tag{14}$$

where I_{pk} is the peak value of primary resonant tank current, Φ_{P-S} is the phase-shift between primary GaNFET S_1 (or S_2) and secondary GaNFET S_3 (or S_4), Φ_{DTS} is the phase corresponding to the dead-time of the secondary side, Φ_{DTP} is the phase corresponding to the dead-time of the primary side, and ϕ_0 is the phase-shift of the resonant current. The output power and voltage can be controlled by varying the phase-shift angle Φ_{P-S} between the primary and secondary GaNFETs.

B. Power stage design

The power stage design of a 200-300 V input and 0-28 V output DC-DC converter switching at 10 MHz frequency is not that straight-forward due to several design variables and high frequency of operation. Hence, an iterative approach is followed to design the proposed isolated step-down converter.

The first step in the design process is to select the transformer turns ratio n. As the turns ratio n increases, the circulating energy reduces and the ZVS of primary GaNFETs is lost. However, the converter achieves soft-switching with a lower turns ratio at the expense of high circulating energy. A turns ratio of n=2.5 is selected to ensure both ZVS of the primary GaNFETs as well as low circulating energy of the resonant tank. Due to the high input voltage and low output voltage requirements, on the primary and secondary sides, 650 V GaNFETs (GS66502B) from GaN Systems and 40 V GaNFETs (EPC2014C) from EPC are chosen, respectively.

The duty cycles of primary and secondary GaNFETs are chosen as D_{pri}=18% and D_{sec}=40%, to ensure enough dead-time for soft-switching the primary and secondary GaNFETs. From equations (4)-(6), it is clear that the resonant tank inductance L_r is a function of the primary magnetizing inductance L_m. That means if one variable is fixed, the other can be calculated. After investigating suitable magnetics for operating at 10 MHz, an EIQ-13 core with Fair-rite 67 material is selected for transformer with a magnetizing inductance of L_m=2.2 μH. The calculated L_r value from equation (6) for C_r=1 nF is L_r=2.35 μH. An EEQ-20 core (using Fair-rite 67 material) with 5 turns is chosen for the inductor, which has in an inductance of L_r=2.7 μH. The details of magnetics will be discussed in Section III. The design of

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the converter at 10 MHz for 300 V input and 28 V output at 20 W is summarized in Table I.

TABLE I: POWER STAGE DESIGN

Variable		Value
n		2.5
R_{ac}		46 Ω
L_m		2.2 µH
Z_2		34.5 Ω
Z_1		131.4 Ω
C_r		1 nF
L_r	Calculation	2.35 µH
	Practical	2.7 µH
Q	Calculation	1.05
	Practical	1.13

An LTSpice simulation of the Class-DE converter is performed using the GaNFET models from the manufacturers. The simulation results showing key waveforms are provided in Fig. 4. The turn-on and turn-off drive voltages for the primary GaNFETs from GaN Systems and the secondary GaNFETs from EPC are 6 V and -2 V, and 5 V and -2 V, respectively.

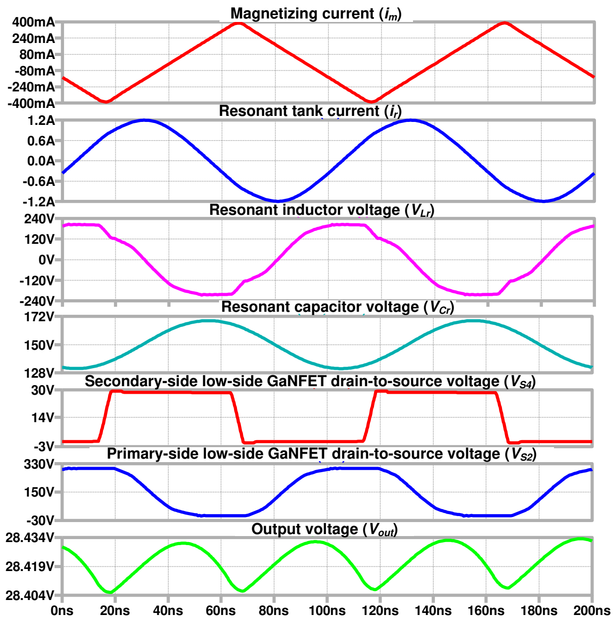

Fig. 4. LTSpice simulation results for V_{in}=300 V at D_{pri}=18% and D_{sec}=40%. The output power P_{out}=20 W. Power stage design parameters given in Table I are used in the simulation.

The voltage gain of the resonant tank M is plotted in Fig. 5 with respect to the normalized frequency f_n and the quality factor Q for a given k. Similarly, the voltage gain of the resonant tank M is plotted with respect to the normalized frequency f_n and k, for a given quality factor Q, as shown in the Fig. 6. For the converter design specifications described above, k =0.82, f_r=3 MHz, and f_n=3.33.

C. Design choices

1) The converter is operating well above the resonance frequency with f_n=3.33. Choosing a large f_n provides a large step-down while giving enough lagging current to achieve ZVS of the primary GaNFET within the dead-time selected.
2) The reactive power is considerably large compared to the active power sent to the load. Hence volt-ampere (VA) rating of the transformer is lower compared to the VA processed by the tank.
3) Since, the transformer size is small, its L_m will also be small for an efficient transformer design. Values of k<1 can have a sizable effect on the gain as seen in Fig. 6.
4) In the design process k is not a design parameter, and it is not dependent on L_m for resonant operation. Achieving high values of k will lead to efficient transformer designs at this high frequency of operation.
5) The quality factor Q does not affect the gain or operating point of the system significantly at high f_n as can be seen in Fig. 5. A range of quality factor Q is possible for the design. However, to limit the voltage stress on the resonant capacitor C_r to a reasonable value a single capacitor can be used, a Q close to 1 is chosen.

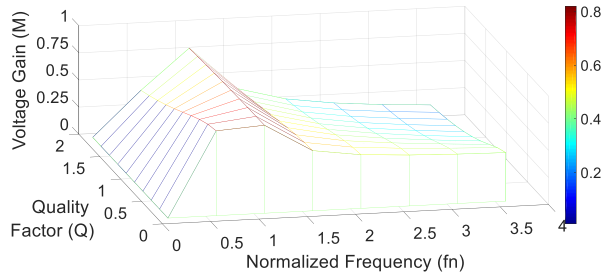

Fig. 5. Voltage gain vs. Loaded quality factor vs. Normalized switching frequency for k =0.82.

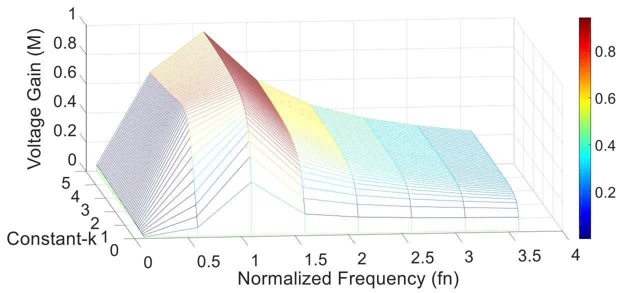

Fig. 6. Voltage gain vs. Constant k vs. Normalized switching frequency for Q =1.13.

The variations of output voltage and output power with respect to the phase-shift Φ_{P-S} are provided in Figs. 7(a), 8(a) and 7(b), 8(b) respectively for various input voltages. The LTSpice simulated, calculated and experimental V_{out} and P_{out} are compared in Fig. 7(a), 7(b) for V_{in}=254 V.

The maximum output voltage and output power for both V_{in} =300 V, 254 V and 200 V occurs at a phase-shift of 54° (15 ns) as shown in Figs. 7 and 8. For 300 V input voltage, the output voltage (from 28 V to 0 V) and output power (from 20 W to 0 W) can be controlled by changing the phase-shift Φ_{P-S} from 82° to 180°. Between this operating phase range, the inductor current will have enough energy for soft-switching. Hence, operation above peak power phase-shift (54° here for V_{in} =254 V) is used to control output power.

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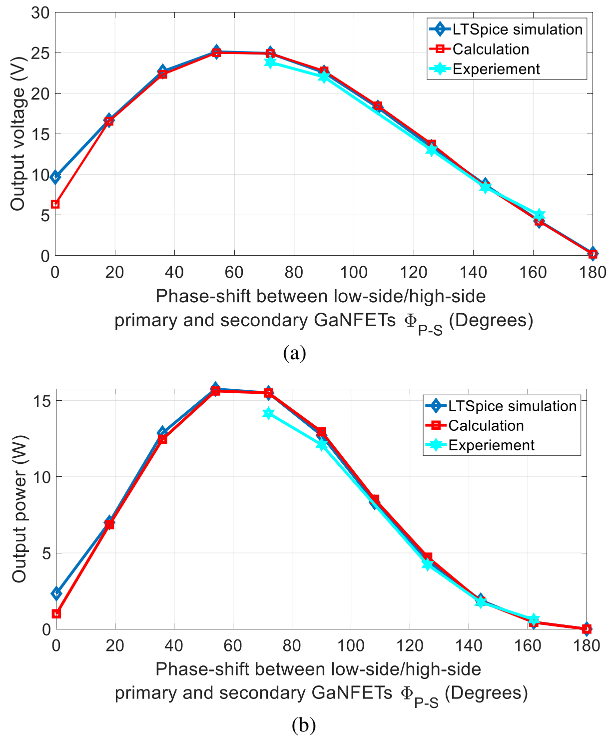

Fig. 7. (a). The variation of output voltage; (b) output power with respect to the phase-shift Φ_{P-S} for V_{in}=254 V, R_L=40 Ω.

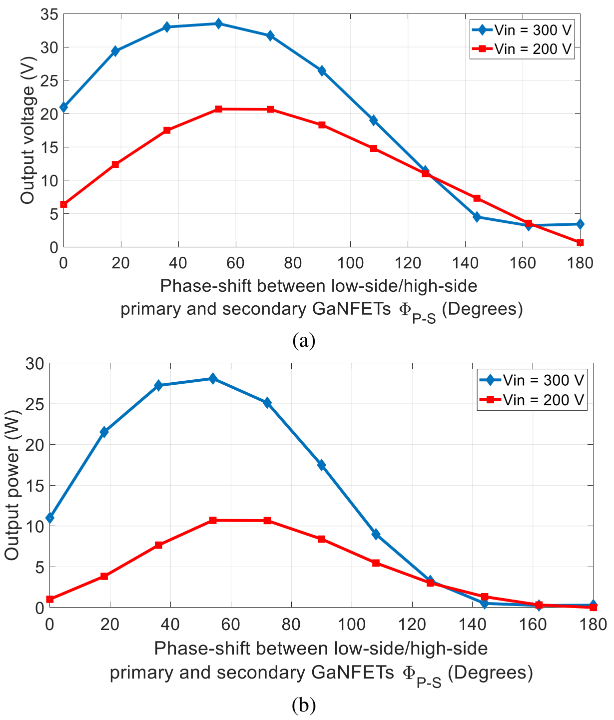

Fig. 8. (a). The variation of output voltage; (b) output power with respect to the phase-shift Φ_{P-S} for V_{in}=300 V and 200 V, R_L=40 Ω.

III. Design and FEM Simulations of Magnetics

A. Inductor and Transformer designs

With the emergence of GaN and SiC devices, there has been a significant advancement in semiconductor device switching speed, but magnetics has become a primary limitation constraining miniaturization. By increasing the switching frequency of the converter, the absolute value of capacitance and inductance can be reduced but the actual size reduction at very high frequencies depends on the allowable loss power density. Appropriate core material and winding structure have to be selected for these high frequencies to reduce the loss and realize the achievable miniaturization. Emerging thin-film magnetic materials are a good choice for frequencies greater than 10 MHz. These materials are typically alloys with Fe, Co and Ni. But these are not commercially available at economical costs [19], [20]. Another limitation is the conductor technology. Usually Litz wire is the choice for high-frequency power applications, however for frequencies higher than 1 MHz, the required strand diameter is around 40 μm which can be expensive and difficult to handle. For these operating frequencies considered here, foil winding structure can be simple and effective solution because they have higher packing factor, better thermal performance compared to Litz wire, and are more cost effective.

There is limited data available on the design of high frequency (HF) and very high frequency (VHF) power magnetics. Power magnetics have high flux drive. For most of the materials, large signal loss data are not available at above a few MHz. Among the commercially available materials, Ni-Zn ferrites and metal-powder materials, which are developed for RF applications, have very high resistivity and are suitable for the present application. The performance factor for these RF materials in range of 1 MHz to 100 MHz are reported in [21] based on the method proposed in [22]. Performance factor is the product of amplitude of AC flux density (B_{ac}) and frequency (f) and is a measure of power handling capability per unit volume for a given core loss density and is a relevant performance metric when core loss is the major design constraint (usually true for transformers and resonant inductors), neglecting AC winding loss. Among the above reported materials, Ferroxcube 4F1 [23] and Fair-Rite 67 [24] material were available in planar structures and rest were available in rods and toroidal shapes meant for RF applications. The 67 material also has the highest performance factor at 10 MHz [20].

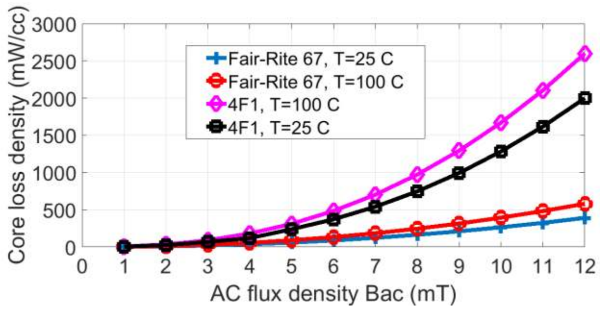

Fig. 9. 4F1 and 67 material core loss density comparison at 10 MHz for different operating temperatures.

For both Ferroxcube 4F1 and Fair-Rite 67 materials, core loss density at 10 MHz for temperatures 25° C and 100° C (sinusoidal flux assumed) is plotted in Fig. 9 from the raw data provided by the manufacturers. The core loss density of 67 material is 390 mW/cm^3 at 10 MHz for

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B_{ac} of 10 mT and is nearly a third of what it is for 4F1 material. Because of the relatively high thermal coefficient of the 4F1, it is not a good option for fabricating a resonant inductor with low air-gap designs. For the initial prototype, 67 material was chosen as the core option for the above reasons. However, a drawback of the 67 material is that when it is exposed to B_{ac} of greater than 20 mT the material properties irreversibly change and have higher losses than the initial characteristics. Permeability of both the material at 25° C and 100° C is given in Table II. The PCB windings for inductor and transformer prototypes are shown in Fig. 10. The inductor and transformer designs are summarized in Tables III and IV, respectively.

A 4-layer PCB (thickness=1.575 mm) with 1 oz. copper thickness is used for practical implementation of the power circuit. To maintain the ease of manufacturing and also high repeatability, multi-layered PCBs are used to realize the magnetic winding structures, 6-layer PCB for the inductor and 8-layer PCB for the transformer. For the inductor, the copper thickness in all layers is 35 µm, and the 3rd and 4th layers are parallel connected. This is done to achieve even number of layers for PCB. Since no air-gap was used in the core for inductor, the field intensity is symmetrical across the middle turn, so paralleling the middle turn ensures equal current sharing between the paralleled layers.

In the transformer, the 5 primary turns are placed in the first 5 layers, the 6th layer in the PCB is kept empty, and the 2 secondary turns are placed in 7th and 8th layers, respectively. Providing an empty 6th layer not only increases the isolation between the primary and secondary windings, but it also minimizes the interwinding capacitance. In Tables III and IV, the measured AC resistance values are used to calculate the AC winding loss.

Based on the one-dimensional field approximation [25], analytical calculations are performed to estimate the AC resistance in the planar PCB windings. This analysis helped to choose an initial optimal thickness for the PCB windings. However, a more detailed FEM analysis is required for operation at 10 MHz to improve the design due to the importance of parasitic effects from aspects such as PCB traces and vias.

TABLE II: 4F1 AND 67 PERMEABILITY WITH TEMPERATURE

Material	Permeability @ T=25° C	Permeability @ T=100° C
4F1	80	140
67	40	45

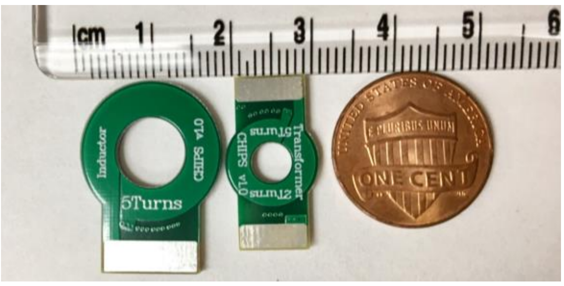

Fig. 10. A photo of inductor and transformer PCB winding prototypes.

TABLE III: INDUCTOR DESIGN SUMMARY

Parameter		Value
Inductance		2.8 µH
Core		EEQ-20, 67 material, Volume=2.01 cm^3, Area=0.6 cm^2
Overall core height		12.7 mm
Effective core length		3.33 cm
Turns, Air-gap		5 turns, No Air-gap
Core loss	@ 20 W	0.68 W (@B_{ac}=11.2 mT)
	@ 12 W	0.46 W (@B_{ac}=9.3 mT)
Copper loss	@ 20 W	0.13 W (for I_{rms}=0.831 A)
	@ 12 W	0.09 W (for I_{rms}=0.683 A)
AC resistance @ 10 MHz		190 mΩ
Copper thickness		35 µm (in all layers)
PCB		6 layer (layers 3 and 4 are paralleled) Total PCB thickness=1.75 mm
PCB thickness between layers {1-2, 3-4, and 5-6}		0.254 mm
PCB thickness between layers {2-3 and 4-5}		0.38 mm

TABLE IV: TRANSFORMER DESIGN SUMMARY

Parameter		Value
Transformation ratio n		2.5
Primary magnetizing inductance		2.18 µH
Core		EIQ-13, 67 material, Volume=0.28 cm^3, Area =0.2 cm^2
Overall core height		3.95 mm
Effective core length		1.39 cm
Turns Non-interleaved: PPPPPSS		5 turns primary, 2 turns secondary
Core loss	@ 20 W	0.055 W (@ B_{ac}=8.7 mT)
	@ 12 W	0.038 W (@ B_{ac}=7.3 mT)
Copper loss	@ 20 W	0.265 W (for I_{rms}=0.831 A)
	@ 12 W	0.18 W (for I_{rms}=0.683 A)
AC resistance referred to primary @ 10 MHz		385 mΩ
Copper thickness		35 µm (in top and bottom layers) 17.5 µm (in all middle layers)
PCB		8 layers, layer 6 is not used Total PCB thickness=2 mm
PCB thickness between layers {1-2, 3-4, 5-6, and 7-8}		0.254 mm
PCB thickness between layers {2-3, 4-5, and 6-7}		0.257 mm

B. FEM simulations

Maxwell 3D simulations have been performed to estimate the AC resistance and leakage inductance of magnetics at 10 MHz. The finite element modelling (FEM) simulation results of the transformer current density and flux density at 10 MHz are shown in Figs. 11(a) and 11(b). The skin depth of copper at 10 MHz is 20.6 µm. A fine mesh based on inside length selection is used to simulate the eddy current effects in the winding. In the primary and secondary windings, the layer to layer connections are made through the vias with an outer diameter of 0.45 mm and the diameter of the via hole is 0.2 mm. In the transformer 3D simulation model, the vias are placed between 2 layers (layer-to-layer).

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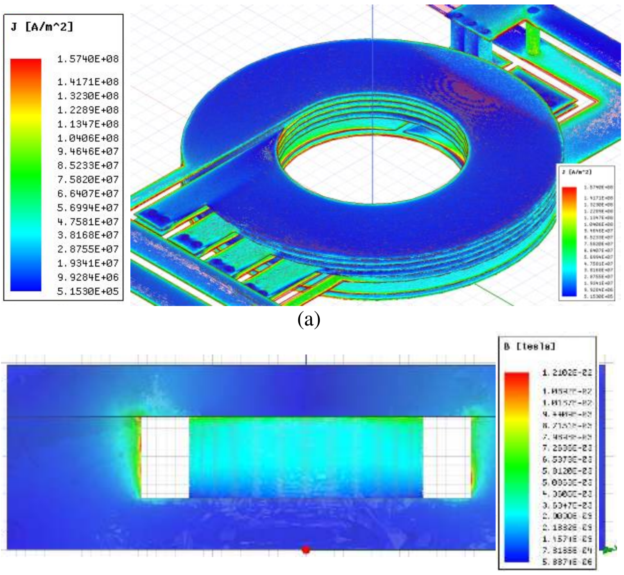

Fig. 11. Plots from the 3D Maxwell simulations of the EIQ-13 transformer (a) Current density at 10 MHz; (b) Magnetic flux density at 10 MHz. Secondary winding is shorted to obtain the AC resistance and leakage inductance.

Design of the magnetics has been a major part of the converter design. The core material selection and PCB windings structure are part of the design challenges that enabled the operation of the converter at high switching frequency of 10 MHz. The parameters of the transformer are measured using the Agilent 4294A Impedance Analyzer. The measurement results are shown in Figs. 12-15.

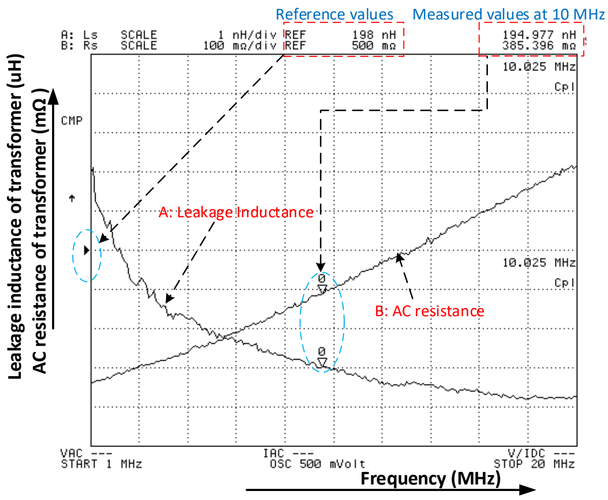

Fig. 12. Measured AC resistance and leakage inductance of the EIQ-13 transformer using Agilent 4294A analyzer.

From Fig. 13, the resonance frequency of the transformer is 48.5 MHz, and the primary magnetizing inductance of the transformer at 10 MHz is 2.18 µH as shown in Fig. 14, which results in a primary transformer self-capacitance of 4.95 pF. The measured interwinding capacitance of the transformer as shown in Fig. 15 is 8.99 pF at 10 MHz. It is obtained by shorting the primary and secondary windings, and measuring the capacitance across the shorted primary and secondary windings. A comparison of the simulated and measured parameters of the transformer is provided in Table V. The simulated and measured transformer parameters show a close match, with the largest error in the AC resistance.

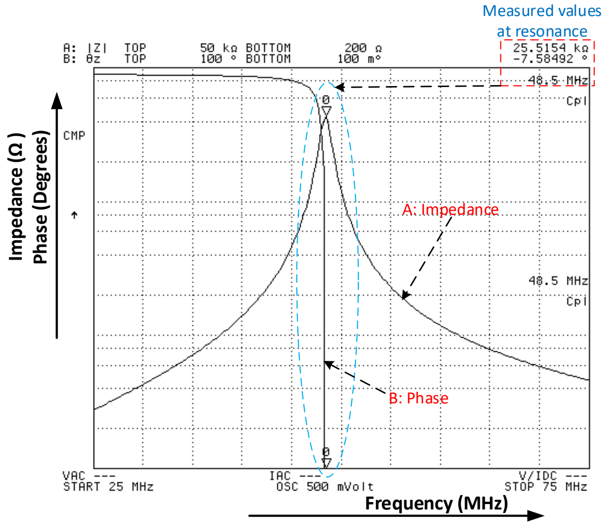

Fig. 13. Measured primary impedance of the EIQ-13 transformer.

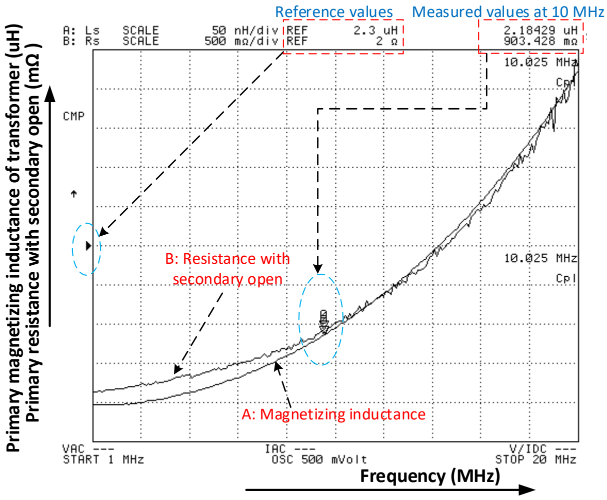

Fig. 14. Measured primary magnetizing inductance of the EIQ-13 transformer.

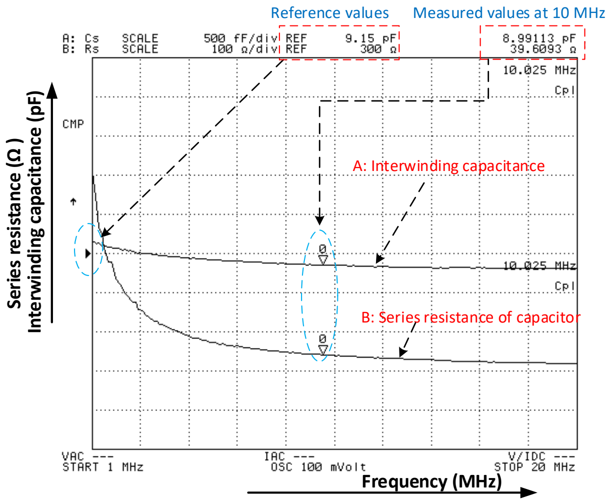

Fig. 15. Measured interwinding capacitance of the EIQ-13 transformer between primary and secondary windings.

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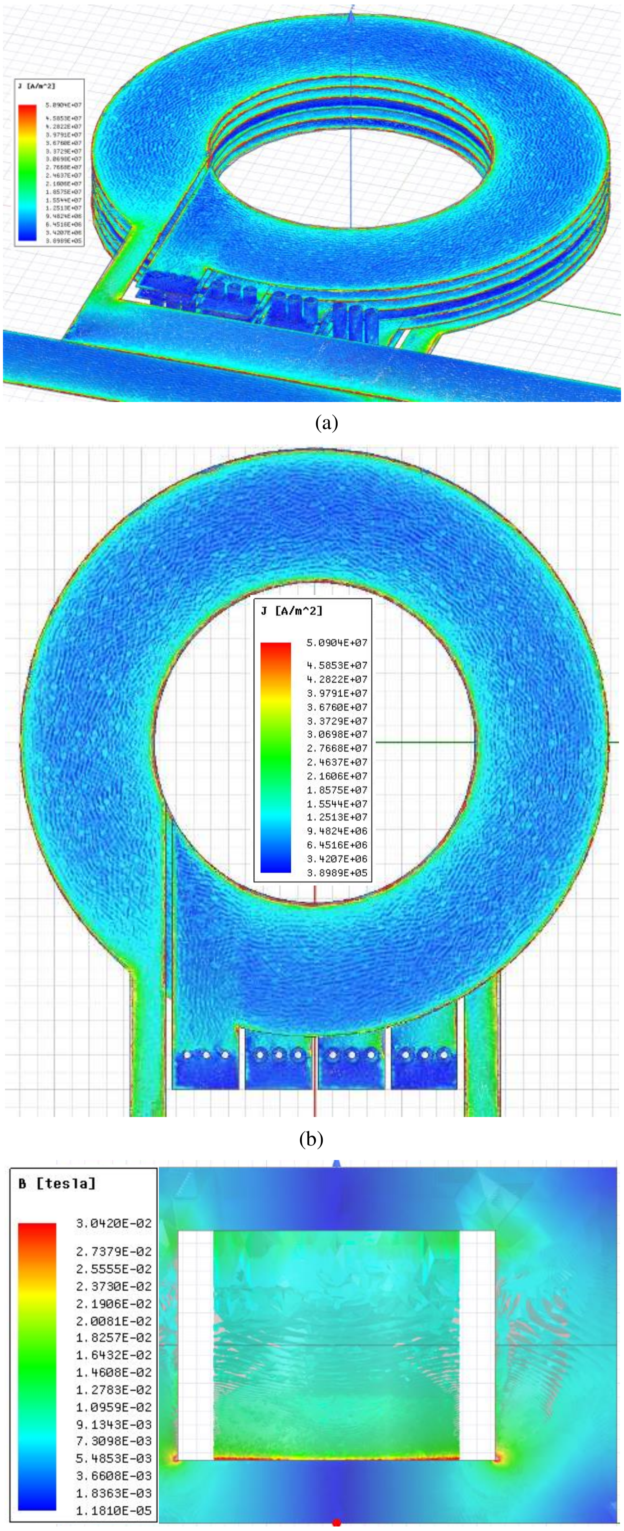
TABLE V: COMPARISON OF SIMULATED AND MEASURED TRANSFORMER PARAMETERS AT 10 MHZ

Variable	Simulation	Measurement
Primary magnetizing inductance	2.17 μH	2.18 μH
AC resistance	300 mΩ	385 mΩ
Leakage inductance	188 nH	194 nH
DC resistance	40 mΩ	45 mΩ



(a)

(b)

(c)

Fig. 16. Plots from the 3D simulations of the EEQ-20 inductor (a) Current density at 10 MHz; (a) Current density top view at 10 MHz; (c) Magnetic flux density at 10 MHz.

The FEA simulation results of the inductor current density and flux density at 10 MHz are shown in Figs. 16(a), 16(b) and 16(c), respectively. As shown in Fig. 16(b), the current is pushed towards the edges of the winding. In the inductor 3D simulation model, the vias pass through all layers (top-layer to bottom-layer). The measured parameters and impedance of the inductor using the Impedance Analyzer are shown in Fig. 17 and 18.

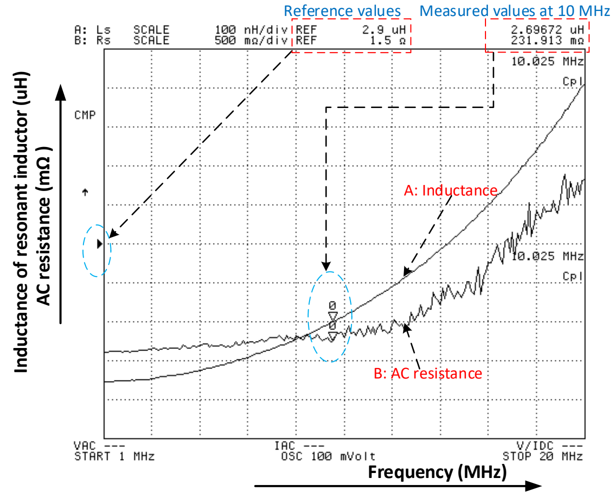


Fig. 17. Measured AC resistance and inductance of the EEQ-20 inductor.

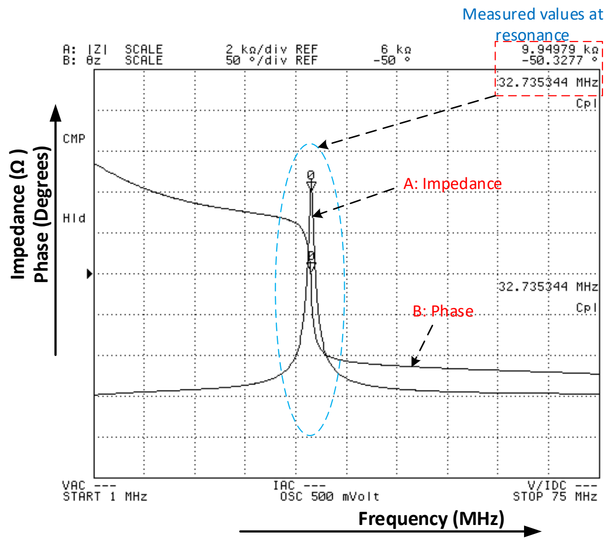


Fig. 18. Measured impedance of the EEQ-20 inductor.

The inductance and resistance parameters shown in Fig. 17 are given by the Impedance Analyzer for an equivalent circuit of series connected inductor and resistor. A series resistance of 231.9 mΩ is measured at 10 MHz. Analytically estimated series resistance of the inductor at 10 MHz is only 117 mΩ and FEM simulations estimate 131 mΩ. This larger error in the measured value is expected due to the parasitic capacitance of the winding. From the impedance plot in Fig. 18, it can be seen that the resonant frequency is 32.7 MHz. Since the resonant frequency is close to the measurement frequency of 10 MHz, the effect of parasitic capacitance can't be neglected. The winding capacitance is estimated to be 9 pF from the resonant frequency. This

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capacitance creates a significant change in the magnitude and phase of the current measured by the Impedance Analyzer which leads to large error in the measured AC resistance. The measured AC resistance is corrected and estimated to be around 190 mΩ after compensating for the winding capacitance.

A comparison of the simulated and measured inductance, DC and AC resistances of the inductor is provided in Table VI. Again, a close match is achieved with the largest error in the AC resistance. The error in AC resistance for both transformer and inductance might be due to the tolerances in PCB layer and via copper thickness. The copper plating thickness of via is usually not a parameter that can be specified. PCB manufacturers usually guarantee a minimum plating thickness and for the current PCBs 18 µm was guaranteed by the manufacturer.

TABLE VI: COMPARISON OF SIMULATED AND MEASURED INDUCTOR PARAMETERS AT 10 MHZ

Variable	Simulation	Measurement
Inductance	2.89 µH	2.69 µH
AC resistance	131 mΩ	190 mΩ
DC resistance	37.5 mΩ	40 mΩ

IV. EXPERIMENTAL RESULTS

An experimental prototype of the Class-DE based converter is shown in Fig. 19. The resonant converter is operated along a narrow optimized trajectory to guarantee ZVS and ZCS. The inductance and noise coupling in gate drive loop are very critical for operation of converter at 10 MHz and at high input voltages. For the practical implementation, primary 650 V, 220 mΩ GS66502B GaNFETs with low output capacitance (17 pF) and gate charge (1.7 nC) are used. For synchronous rectification, 40 V, 60 mΩ EPC2014C GaNFETs (C_{oss}=150 pF, Q_g=2 nC) are used in the secondary side. A HF diode PMEG6010CEH is used for D_3 and D_4. The experimental results are provided in Figs. 20, 21 and 22. The primary switch-node voltage, gate-drive signal for GaNFET S_2, and the output voltage for phase-shifts 90° and 126° are shown in Figs. 20 and 22, respectively. The output powers in Figs. 20 and 22 are 12 W and 5 W, respectively.

High-frequency resonant capacitors from ATC are used for C_r, C_1 and C_2. A 1000 V, 1 nF capacitor (100C102JW) is used for C_r [26]. A 100 V, 684 nF capacitor (900C684MP) is used for C_1 and C_2 [27]. A digital isolator ADuM210N with common mode transient immunity (CMTI) ≥ 100 V/µs is used for isolation. Due to non-availability of commercially available half-bridge gate drivers for 300 V input and 10 MHz operation, and to quickly evaluate the power stage design, a battery powered isolated low-side gate driver LM5114 [28] is used for driving each GaNFET. All gate-drivers for switches S_1-S_4 have been designed with a negative-bias supply to prevent false turn-on. A negative bias of -2 V is used for both primary side/GaN system devices and secondary side/EPC devices. Negative bias voltage in switch S_2 can be seen from Fig. 20. Independent turn-on and turn-off gate drive resistors $R_{g,ON}$=20 Ω and $R_{g,OFF}$=3.3 Ω are used to counter Miller effect on primary side. A Virtex-5 FPGA development board is used to generate the required 10 MHz driving signals on both primary and secondary sides.

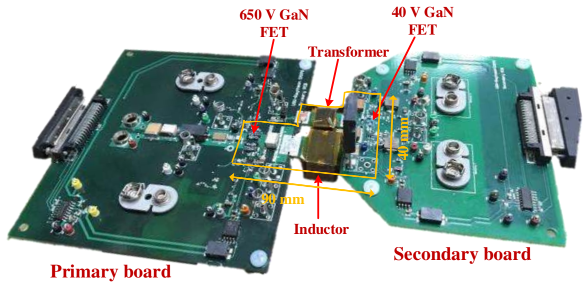

Fig. 19. An experimental prototype of the Class-DE based converter. The 10 MHz switching power stage is outlined in yellow. The rest of the PCB has connectors to the FPGA board, digital isolators, test points and auxiliary supplies for gate drivers.

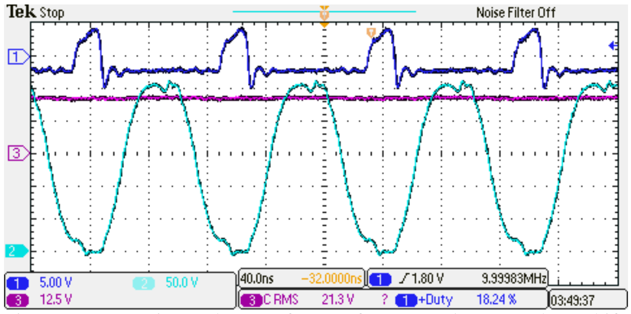

Fig. 20. Experimental waveforms for V_{in}=254 V, Phase-shift Φ_{P-S} =25 ns (90°), D_{pri}=18%. CH1: Gate-to-source signal of S_2 [5 V/div]; CH2: Drain-to-source waveform of S_2 [50 V/div]; CH3: Output voltage across 40 Ω load [12.5 V/div].

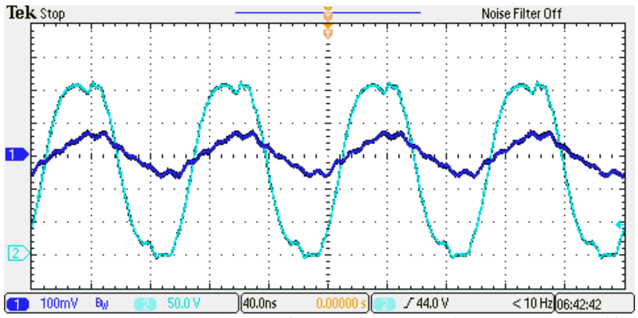

Fig. 21. Experimental waveforms for V_{in}=254 V, Phase-shift Φ_{P-S} =25 ns (90°), D_{pri}=18%. CH1: Resonant tank current [2 A/div] (dark blue); CH2: Resonant tank voltage [50 V/div] (light blue).

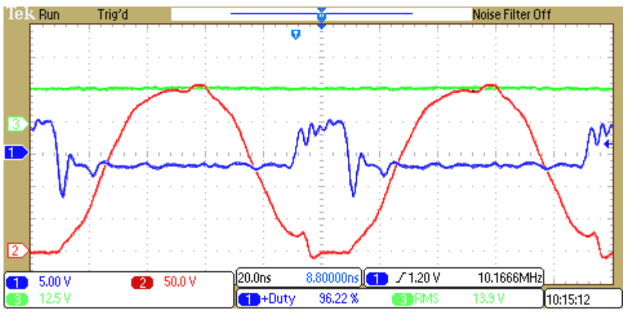

Fig. 22. Experimental waveforms for V_{in}=254 V, Phase-shift Φ_{P-S} =35 ns (126°), D_{pri}=18%. CH1: Gate-to-source signal of S_2 [5 V/div]; CH2: Drain-to-source waveform of S_2 [50 V/div]; CH3: Output voltage across 40 Ω load [12.5 V/div].

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V. Power Loss Breakdown

A. Loss-breakdown

The total loss breakdown for the proposed DC-DC converter for V_{in}=300 V, at rated power is shown in Fig. 23. The measured efficiency of the prototype converter is provided in Fig. 24. The inductor and transformer losses include both winding loss and core loss. The driving loss is the total gate drive loss for both primary and secondary GaNFETs. The GaNFET device losses include the total forward and reverse conduction losses, and switching loss due to all primary and secondary GaNFETs. This device loss is very low when all the GaNFETs are soft-switching. In other words when the dead-time is optimum (for both primary and secondary) the total device loss will be very low. The loss due to the power consumption in the auxiliary power supply is estimated to be 1 W, the loss due to the ESR of the capacitors, and PCB traces are considered as additional conduction losses. The total power loss is 3.46 W. The calculated efficiency of the converter at an output power of 20.2 W is 85.38%. Optimizing the magnetics and auxiliary power supply (for powering the gate drivers) designs could further increase the efficiency of the converter. Integrating the transformer and inductor into a single magnetic structure will reduce the overall size of the magnetics. Winding resistance can be reduced by paralleling multiple layers in planar PCB windings. The power stage and magnetics designs could be further investigated and optimized by changing the inductance constant-*k* described in Section II, however it is out of scope of this paper.

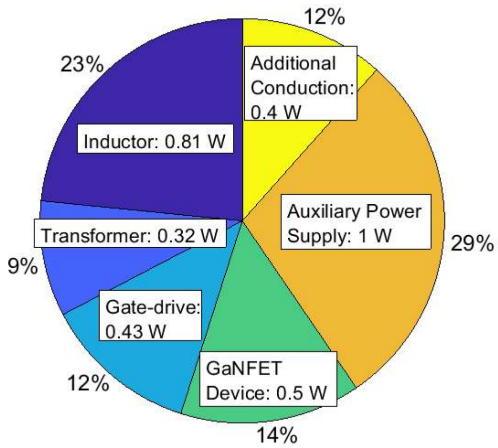

Fig. 23. Total loss breakdown for a 300 V to 28 V step-down for an output power P_{out}=20.2 W at 10 MHz switching frequency.

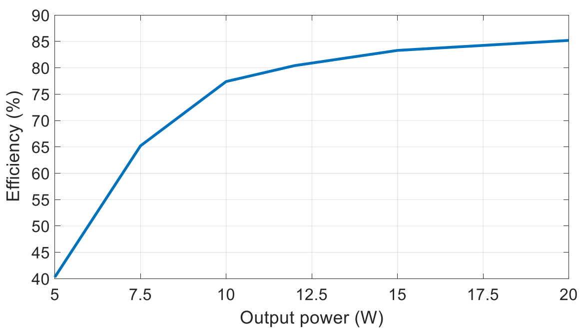

Fig. 24. Measured efficiency as a function of output power.

B. Control of the HF DC-DC converter

Envelop tracking capability helps to reduce heat and power consumption of the power amplifier (PA). Precise control is not a requirement for this application [29], [30]. The PA is linear (Class A or Class AB for instance) and has very high bandwidth. The envelope tracking converter can be slower and less accurate because the only requirement is to supply the PA with a voltage higher than the envelope to avoid the saturation of the output stage of the PA. But the bandwidth required (close to 1 MHz) is still very high for a switching converter. To achieve this high bandwidth a feed-forward control can be implemented. The PA load can be effectively represented by a resistor. For a given PA, the phase-shifts Φ_{P-S} can be pre-calculated and stored in a look-up table over the output voltage range. The recommended control block diagram is illustrated in Fig. 25. This suggested control has not been validated as a part of this paper.

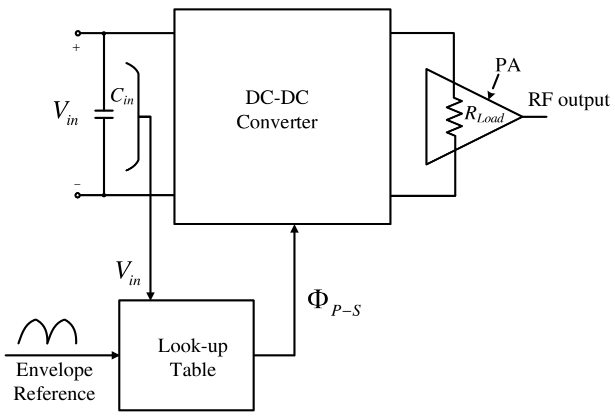

Fig. 25. Recommended control block diagram.

VI. Conclusions

In this paper, a high-frequency, high-step down isolated DC-DC converter equipped with the GaN devices is analyzed and designed. The proposed resonant design shapes waveforms to optimize magnetics and achieve high efficiency with high power density. A low-EMI is expected due to S-shaped transition of the switch-node voltage, and due to the smooth and sinusoidal high frequency resonant tank current waveform. Moreover, the following solutions help in minimizing the radiated EMI in HF DC-DC converters: by minimizing the power supply path for high frequencies, by designing the PCB to minimize the loop areas, by selecting the correct HF capacitors, and by adding an electromagnetic shielding.

The inductor and transformer are designed using commercially available magnetic materials to minimize the physical size and core and copper losses when operating at a switching frequency of 10 MHz. The core material Fair-Rite 67 was chosen from many of the commercially available magnetic materials because of its better performance factors and its availability in low-profile planar structures. Maxwell 3D simulations were performed to estimate the parameters of the inductor and transformer to aid the design process. A phase shift angle between the primary and secondary GaNFETs was used to regulate the output voltage and power of the DC-DC converter. Phase-shift angle range between peak power angle and 180° is used to ensure that there is enough reactive energy to soft-switch at low loads. A 20 W, 300 V to 28 V laboratory prototype operating at 10 MHz converter achieved an efficiency of 85.2%.

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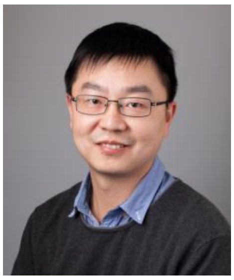

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