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# A 100-Channel 1-mW Implantable Neural Recording IC

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**Abstract**—This paper presents a fully implantable 100-channel neural interface IC for neural activity monitoring. It contains 100-channel analog recording front-ends, 10 multiplexing successive approximation register ADCs, digital control modules and power management circuits. A dual sample-and-hold architecture is proposed, which extends the sampling time of the ADC and reduces the average power per channel by more than 50% compared to the conventional multiplexing neural recording system. A neural amplifier (NA) with current-reuse technique and weak inversion operation is demonstrated, consuming 800 nA under 1-V supply while achieving an input-referred noise of  $4.0 \mu\text{V}_{\text{rms}}$  in a 8-kHz bandwidth and a NEF of 1.9 for the whole analog recording chain. The measured frequency response of the analog front-end has a high-pass cutoff frequency from sub-1 Hz to 248 Hz and a low-pass cutoff frequency from 432 Hz to 5.1 kHz, which can be configured to record neural spikes and local field potentials simultaneously or separately. The whole system was fabricated in a  $0.18\text{-}\mu\text{m}$  standard CMOS process and operates under 1 V for analog blocks and ADC, and 1.8 V for digital modules. The number of active recording channels is programmable and the digital output data rate changes accordingly, leading to high system power efficiency. The overall 100-channel interface IC consumes 1.16-mW total power, making it the optimum solution for multi-channel neural recording systems.

**Index Terms**—Multi-channel neural recording system, biomedical application, high power efficiency, power and area trade-off, dual S/H, low-noise neural amplifier, current reuse, NEF, SAR ADC, capacitor-less LDO

## I. INTRODUCTION

Simultaneous recording of neuropotentials from the brain over a large number of electrodes provides an effective

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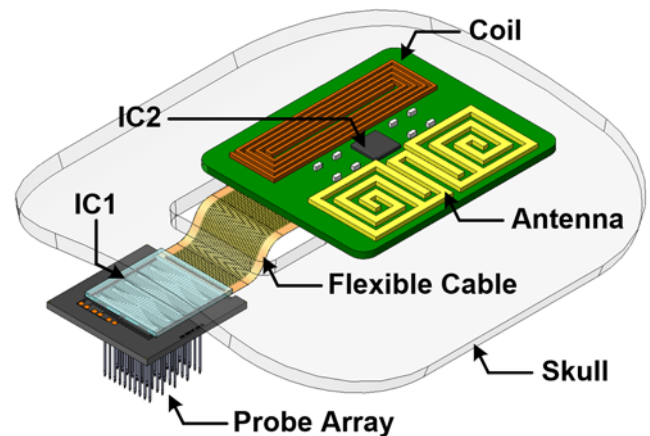


Fig. 1. Fully implantable wireless neural recording microsystem (not drawn to scale).

way for neuroscientists and clinicians to study the brain state dynamics and understand the nature of various neurophysiological behaviors. It has a wide range of applications, where the most exciting one currently is the development of brain-controlled neural prostheses. Recent clinical trials with paralyzed human volunteers have shown that it is possible to restore limb movement by such neuroprosthetic devices [1]–[3]. This calls for the development of an ultra-low-power implantable neural recording microsystem, like the one shown in Fig. 1. It consists of a  $10 \times 10$  neural probe array, a multi-channel neural recording interface IC (IC1), a wireless power and data link IC (IC2), and a flexible cable to exchange recorded data, extracted DC power, and digital control and clock signals between IC1 and IC2. In this paper, the system and circuit design of the IC1 is presented.

Effective and reliable neurological researches and diagnoses rely on multi-channel recordings from a large population of neurons. High-density recording systems with 100 channels to as many as 256 channels have been recently reported [4]–[7]. Since any amount of excessive heat dissipation by the recording microsystem induces damage to the surrounding tissue when it is implanted in the brain, the power consumption of the high-density recording electronics should be strictly restrained. In addition, implantable devices are usually powered through wireless power transfer links to obviate the need of large-capacity batteries or skin-piercing wires. The specific absorption rate of living tissue sets a stringent limit on power budget of the implant. Meanwhile, chip area is also an important constraint for implantable

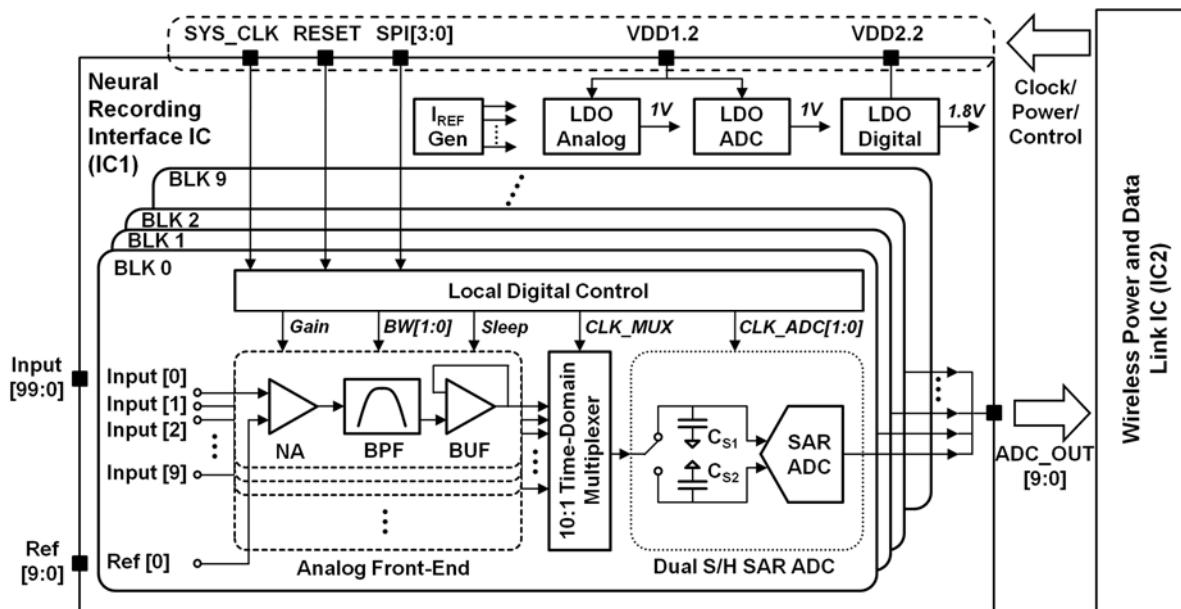


Fig. 2. System architecture of the neural interface IC.

devices to minimize surgical damage. The simultaneous requirements of low power consumption, minimum chip area, and a large number of recording sites impose a critical challenge to IC designers.

A conventional multi-channel neural recording interface IC requires signal conditioning and digitization blocks, which are usually realized by low-noise preamplifiers and ADCs. A successive approximation register (SAR) ADC is widely adopted in biomedical recording systems due to its high energy efficiency, while providing moderate resolution and conversion speed. Due to chip area restraint, one ADC is usually shared among multiple recording channels by employing a time-domain multiplexer [7]–[9]. Recently reported sensor interface ICs have put much effort into reducing the power consumption of individual functional blocks, such as the low-noise neural amplifier and the ADC, which can be realized with the power consumption of a few  $\mu\text{W}$  [7], [10]. However, little has been done in optimizing the overall system architecture to minimize the total system power. For example, a buffer preceding the ADC can draw tens of  $\mu\text{W}$  due to the shortened sampling time of the ADC in the conventional multi-channel system architecture, which simply overrides the consumption by the preamplifier and ADC and results in a high consumption of the total system power [7]. In [11], a design methodology for the optimized multi-channel neural recording IC was proposed to provide a systematic way to determine key system-level design parameters. It helps designers to achieve the minimum power-area product for the entire IC within the limit of the conventional architecture.

Some reported designs adopt data compression algorithm to reduce the transmitted data rate to minimize the power consumption [6]. However, this approach may lose some useful information and lead to inaccurate outcome. The complete raw recording data is preferred for the following

neural activity processing and analysis. An alternative solution to reduce the system power is implementing one ADC for each analog recording channel [12]. By doing so, the sampling time of the ADC is greatly extended and the power consumption of the system is minimized. However, this approach will significantly increase the total chip area due to the large area occupied by a large number of SAR ADCs.

In this paper, we present a 100-channel power- and area-efficient neural interface IC for a fully implantable wireless neural recording microsystem. The IC contains 10 recording blocks and power management circuits. Each of the 10 recording blocks consists of 10 analog recording chains, one SAR ADC and one digital control module. A power- and area-efficient multi-channel system structure is proposed with dual sample-and-hold (S/H) circuits, leading to more than 10 times of power saving in the ADC buffer compared to that in the conventional multi-channel recording system. Meanwhile, the increment of the chip area is kept to a minimum. The neural amplifier employs current-reuse technique, achieving an input-referred noise of  $4.0 \mu\text{V}_{\text{rms}}$  in 8-kHz bandwidth and a Noise Efficiency Factor (NEF) of 1.9. A 9-bit ADC with one redundant bit is implemented for every 10 analog recording chains. Three low-dropout regulators (LDOs) are integrated to provide separate regulated DC supplies to the analog recording chains, ADCs and digital control blocks. The overall system was fabricated using  $0.18\text{-}\mu\text{m}$  standard CMOS process and consumes  $1.16\text{-mW}$  total power.

The paper is organized as follows. Section II describes the system architecture of the multi-channel neural interface IC. The detailed circuit designs of the analog recording chains, ADCs and LDOs are presented in Sections III, IV and V, respectively. Section VI reports the measurement results and Section VII concludes the paper.

## II. SYSTEM ARCHITECTURE

Fig. 2 shows the overall system architecture of the 100-channel neural interface IC. There are 10 neural recording blocks for conditioning and digitizing the captured neural signals. Each recording block contains 10 analog recording chains. After multiplexed by a time-domain multiplexer, the conditioned analog signals are then digitized by the following 9-bit SAR ADC. A digital control unit in each recording block provides all the clock sequences and control signals. Note that the overall configuration and timing control is managed by the central digital controller residing in the IC2. The local control unit in each recording block of the IC1 communicates with the central controller through the serial peripheral interface (SPI). LDOs and a current reference generator provide stable DC power and necessary current biases to the whole neural interface IC. The DC supply voltages of 1.2 V and 2.2 V are extracted from wireless RF power in IC2 and sent to IC1 via the flexible cable, as illustrated in Fig. 1. Two LDOs (LDO Analog and LDO ADC in Fig. 2) generate 1-V regulated DC voltage from the 1.2-V supply, and the other LDO (LDO Digital) provides 1.8-V voltage from the 2.2-V DC input.

As shown in Fig. 2, each analog recording channel consists of a low-noise neural amplifier, a BPF, and a unity-gain buffer. Usually, the bandwidth of the biomedical recording system is defined by the 3-dB cutoff frequency  $f_{3dB}$  of the low-noise preamplifier according to the equation,

$$f_{3dB} = \frac{g_m}{C_C \cdot A_V} \quad (1)$$

where  $g_m$  is the transconductance,  $C_C$  is the compensation capacitor, and  $A_V$  is the mid-band gain of the neural amplifier. Low input referred noise requires a large  $g_m$ , leading to a large  $C_C$  of tens of pF, and consequently a large chip area [13]. In order to solve this problem, the system bandwidth in this design is determined by the second stage BPF, where its input-referred noise is not critical and hence its  $g_m$  can be set much smaller than that of the preamplifier. By doing so, a smaller  $C_C$  of a few pF is enough to meet the system bandwidth requirement [14].

Local field potentials (LFPs) and neural spikes are two types of neuropotential signals that are commonly studied to understand cortical activities. The LFPs have relatively large amplitudes of 100  $\mu V_{pp}$  to 1 mV<sub>pp</sub> and occupy a low frequency range from sub-1 Hz to about 100 Hz. For the neural spikes, they are usually observed with amplitudes of tens or hundreds of  $\mu V_{pp}$  and frequencies ranging from 300 Hz to 5 kHz. A versatile recording system should be able to record either the LFPs or neural spikes separately, or both simultaneously. In the proposed system, both high-pass and low-pass cutoff frequencies of the BPF can be programmed to support different recording modes. In order to enhance the system dynamic range, a programmable gain function should be implemented. One method to adjust the system gain is changing the feedback capacitance of the BPF. However, this approach also changes the BPF bandwidth and hence the system bandwidth accordingly. In this design, the system gain is controlled by the neural amplifier, as its bandwidth variation

will not affect the system performance because its bandwidth is much larger than the system bandwidth. Since the BPF bandwidth is set to match the neural signal frequency, an dedicated buffer is implemented to drive the multiplexer and the sample-and-hold (S/H) circuit of the ADC. By partitioning the different functions of system gain adjustment, bandwidth control, and ADC drive as described, the design focus for each individual block is explicit and design requirements become relaxed. This effectively helps to achieve optimal system performance and power consumption.

Most of the recently reported works have focused on the power optimization of individual circuit blocks, such as the neural preamplifier and ADC, which are implemented with the power consumption of sub- $\mu W$  to a few  $\mu W$ . However, without a carefully designed system architecture, some auxiliary circuits may easily draw excessive current and override the low consumption of key building blocks, resulting in high total power consumption. In conventional multi-channel biomedical recording system, the ADC is usually shared by multiple analog recording channels to save chip area, as illustrated in Fig. 3(a). A typical timing diagram of one S/H circuit shared by 10 channels is shown in Fig. 3(b). According to Nyquist criterion, the effective sampling rate of the ADC for each channel needs to be at least  $2f_{signal}$ , where  $f_{signal}$  is the maximum frequency of the input neural signal. As a result, the time period for ADC to finish digitization of one analog channel is  $T_{ch} = 1 / (2f_{signal} \times 10)$ . Taking a 9-bit ADC for example, the sampling time of the traditional SAR ADC is  $T_{ch}/10$ , which is only 1  $\mu s$  for 5-kHz input signal. This sampling time will decrease further if higher oversampling ratio or higher-resolution ADC is needed. As a result, large driving capability is required for the preceding buffer. As reported in [7] with the conventional multiplexing structure, the buffer draws 20.3- $\mu A$  current while the preamplifier consumes only 2  $\mu A$ . It is obvious that the buffer is a dominant power consumer in the system and more effort is needed to minimize the buffer current. One approach to extend the sampling time and reduce the system power is employing one dedicated ADC for each channel [12]. However, this will result in large chip area, which is not desirable for implantable high-density recording devices.

In order to achieve low power and small chip area, a dual S/H scheme for multi-channel system is proposed, as illustrated in Fig. 2. There are two S/H circuits connected to each ADC, and they work in an alternate manner. That is, when one S/H is holding the output of one recording channel for conversion, the other S/H is sampling the output of the next channel. By adopting the dual S/H architecture, the sampling time of the ADC is extended from  $T_{ch}/10$  to  $T_{ch}$ , as the S/H actions are conducted in parallel mode instead of serial mode in the conventional multi-channel system. The timing diagram of the proposed dual S/H ADC is shown in Fig. 3(c). Compared to Fig. 3(b), the extension of the sampling period of the proposed structure is clearly demonstrated. As the power consumption of the buffer dominates in the conventional multi-channel system with single S/H, the system power reduction with the dual S/H approach is

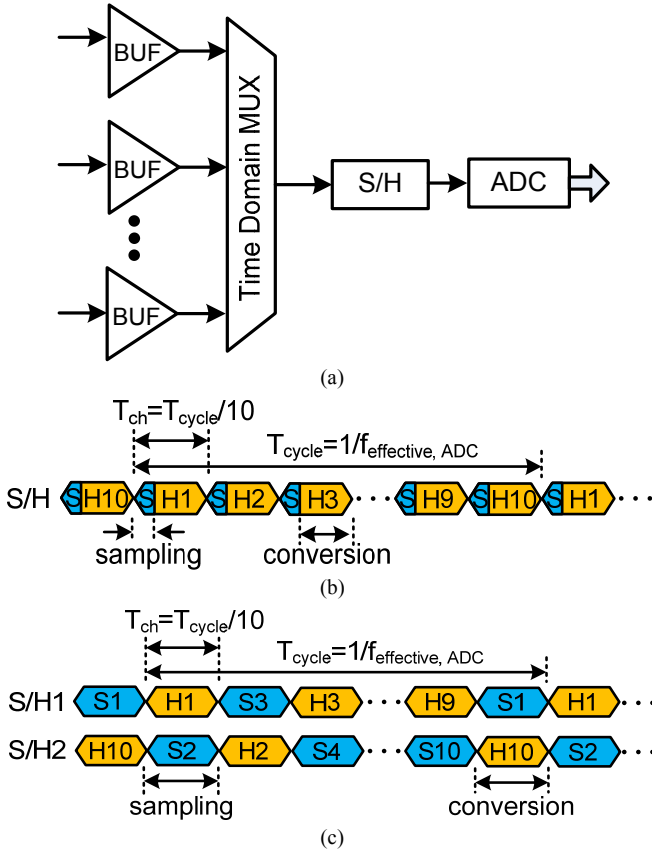


Fig. 3. (a) Conventional multi-channel recording system with a shared ADC. (b) S/H timing diagram of the conventional system. (c) Timing diagram of the proposed dual S/H system architecture.

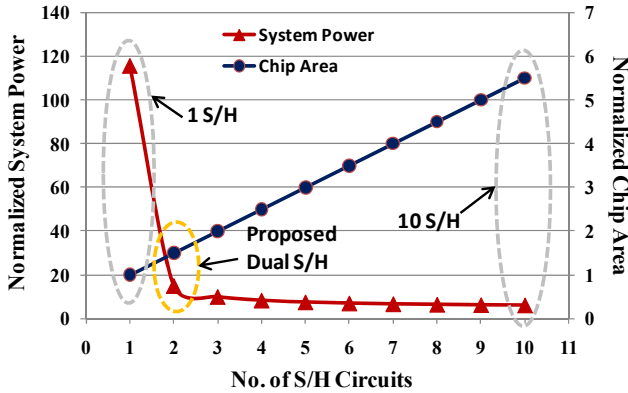


Fig. 4. System power and chip area vs. number of S/H circuits. The chip area is normalized to the system area with a single S/H circuit. The system power is normalized to the ADC buffer power consumption in the dual S/H system.

prominent. Using the proposed system architecture, a buffer with 1.2- $\mu$ A current fulfills the sampling time requirement, leading to a less than 5  $\mu$ W average power for each channel including the ADC.

To further demonstrate the high power and area efficiency of the proposed architecture, we estimate the system power and chip area when one ADC is shared by 10-channel, with varying number of S/H circuits, and plot the results in Fig. 4. It shows that chip area increment is linear with the number of S/H circuits. However, the system power is strongly nonlinear.

When the number of S/H circuits increases from 1 to 2, the system power decreases dramatically. Fig. 4 clearly emphasizes the optimal power-area trade-off of the proposed dual S/H structure.

Besides the full-throughput operation mode with all the 100-recording channels turned on, the neural interface IC can be also configured with 10, 20 or 50 active channels, while the rest are in sleep mode. One way to realize the partial-throughput operation mode is to select 1, 2 or 5 ADCs working in full load. However, this will limit the selection flexibility of the recording sites, as turning off one ADC means all the data from the 10 analog channels attached to it will be lost. In this design, the 10 ADCs are always activated and the partial-throughput operation mode is achieved by varying the number of active analog recording chains attached to the ADC. Since the ADC supports a smaller number of analog channels, the clock frequency of the ADC is reduced accordingly. This results in better performance and lower power consumption of the ADCs as they now operate at much lower frequency compared to the full-load mode. Note that the sampling frequency for each analog channel is kept constant despite the change of the ADC clock frequency. For the partial-throughput operation mode, any 1, 2 or 5 channels can be selected freely from the 10 channels attached to the ADC, while the other unselected channels stay in sleep mode and consume about 0.5  $\mu$ W per channel.

### III. ANALOG RECORDING CHAINS

#### A. Low-Noise Neural Amplifier

The neural amplifier is one of the most critical components in the neural recording system, and its schematic is shown in Fig. 5. A capacitive feedback topology with pseudo-resistors is chosen to achieve low power and low noise. The gain of the amplifier can be set at 34 dB and 40 dB by the switch associated with  $C_3$  ( $C_1=20$  pF,  $C_2=C_3=400$  fF). Since the low-pass cutoff frequency of the system is determined by the second-stage BPF, the bandwidth of the neural amplifier is set to be slightly larger than the signal bandwidth.

The design of the OTA in the neural amplifier is of particular importance, where power consumption and input-referred noise are the two most important factors. The NEF is introduced to measure the trade-off between these two factors, and defined by the following equation [15],

$$NEF = V_{rms,in} \sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (2)$$

where  $V_{rms,in}$  is the root-mean-square (RMS) value of the input-referred noise,  $I_{tot}$  is the total supply current of the amplifier,  $U_T$  is the thermal voltage,  $k$  is the Boltzman constant,  $T$  is the absolute temperature, and  $BW$  is the amplifier bandwidth in hertz. The lower NEF means the better power-noise trade-off. To achieve a good noise performance with limited power budget, current-reuse technique is an attractive choice, where both NMOS and PMOS transistors are stacked in the same current branch to obtain double  $g_m$  [16], as shown in Fig. 6.

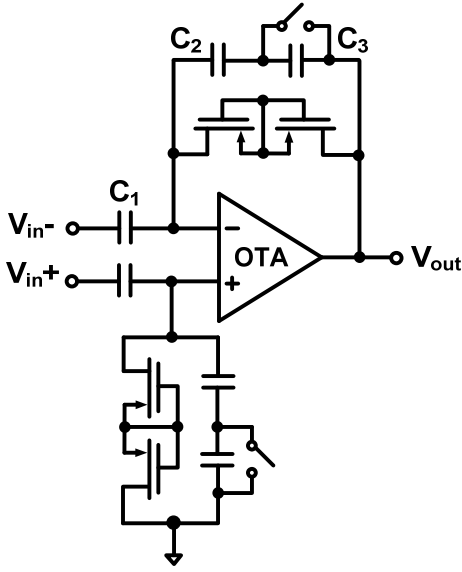


Fig. 5. Schematic of the low-noise neural amplifier.

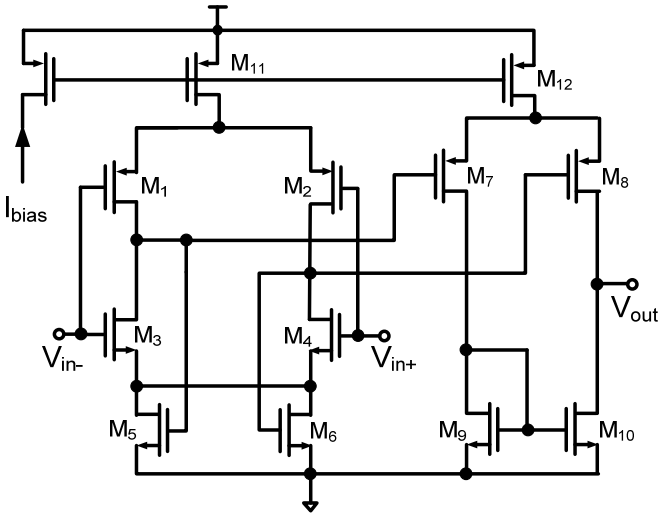


Fig. 6. Schematic of the low-noise OTA used in the neural amplifier.

Meanwhile, a subthreshold operation provides high  $g_m$  efficiency, and has been widely adopted in biomedical recording systems.

Using the EKV model [17] which is valid in all operation regions, the  $g_m$  of a MOS transistor in deep subthreshold region is approximated as

$$g_m \cong \frac{I_D}{nU_T} \quad (3)$$

where  $n$  is the slope factor with a typical value of 1.5 and  $I_D$  is the drain current. The current noise power spectral density of MOSFETs operating in subthreshold region [18] is modeled as

$$\overline{i_n^2} = 4kT\gamma g_m = 4kT\gamma \frac{I_D}{nU_T}. \quad (4)$$

$\gamma$  is the thermal noise coefficient, which is 2/3 for transistor in strong inversion region and 1/2 in weak inversion region. The input-referred voltage noise of an ideal differential pair in subthreshold region without current-reuse technique can be

derived as

$$\overline{v_{ni,no-reuse}^2} = \frac{2\overline{i_{ni}^2}}{(g_m)^2} = 8kT\gamma \frac{nU_T}{I_D}. \quad (5)$$

When the current-reuse technique is applied, assuming that all the four input transistors have the same  $g_m$  value and all the other conditions remain the same, the input-referred noise becomes

$$\overline{v_{ni,reuse}^2} = \frac{4\overline{i_{ni}^2}}{(2g_m)^2} = 4kT\gamma \frac{nU_T}{I_D}. \quad (6)$$

It shows that the input-referred noise power is reduced by half when the current-reuse scheme is applied, compared to the circuit without it.

In this design, a fully differential current-reuse OTA is employed as shown in Fig. 6. The current-reuse technique is employed at the input stage to achieve required noise performance with minimum current. The four input transistors are biased in weak inversion region to maximize  $g_m/I_D$  and further enhance the current efficiency. Large gate areas ( $W/L = 300 \mu\text{m}/2 \mu\text{m}$  for NMOS and  $200 \mu\text{m}/1 \mu\text{m}$  for PMOS) are chosen to suppress the  $1/f$  noise.  $M_5$  and  $M_6$  provide a common-mode feedback and fix the output DC level of the first stage. In the second stage, PMOS transistors are chosen as the input pair to reduce the  $1/f$  noise. The input-referred thermal noise of this OTA is given by

$$\overline{v_{n,thermal}^2} \approx 2 \times \frac{4kT}{(g_{m1,2} + g_{m3,4})} \times \left[ \gamma_{wi} + \frac{\gamma_{si}g_{m5,6} + \gamma_{wi}g_{m7,8}}{g_{m1,2} + g_{m3,4}} + \frac{\gamma_{wi}g_{m9,10}^2}{(g_{m1,2} + g_{m3,4})g_{m7,8}} \right] \times \Delta f \quad (7)$$

where  $\Delta f$  is the bandwidth of the amplifier. It is clear that the large  $g_{m1,2} + g_{m3,4}$  will minimize the noise contributions from  $M_5$ – $M_{10}$ . Hence, 80% of the total amplifier current is allocated to the input stage.  $M_1$ – $M_4$  and  $M_7$ – $M_8$  are biased in weak inversion region to maximize the  $g_m$  efficiency, while  $M_5$ ,  $M_6$ ,  $M_9$  and  $M_{10}$  are biased in strong inversion region to minimize their thermal noise contribution.

When the neural amplifier is in sleep mode, its quiescent current is reduced from 800 nA to 160 nA. This non-zero sleep current maintains the DC level at each node of the OTA near the normal operation voltage and helps to achieve fast recovery when the amplifier is activated. In addition, the neural amplifier operating in the sleep mode has a minimum bandwidth of 300 Hz, which can be also used for LFP signal recording.

### B. Band-Pass Filter and Unity-Gain Buffer

As discussed in Section II, the BPF determines the system bandwidth. At the same time, it provides an additional gain of 10 to enhance the system dynamic range. Fig. 7(a) shows the schematic of the BPF, which has the AC-coupled input and closed-loop configuration. Both low-pass and high-pass cutoff frequencies of the BPF are programmable. The low-pass cutoff frequency is determined by the 3-dB roll-off frequency

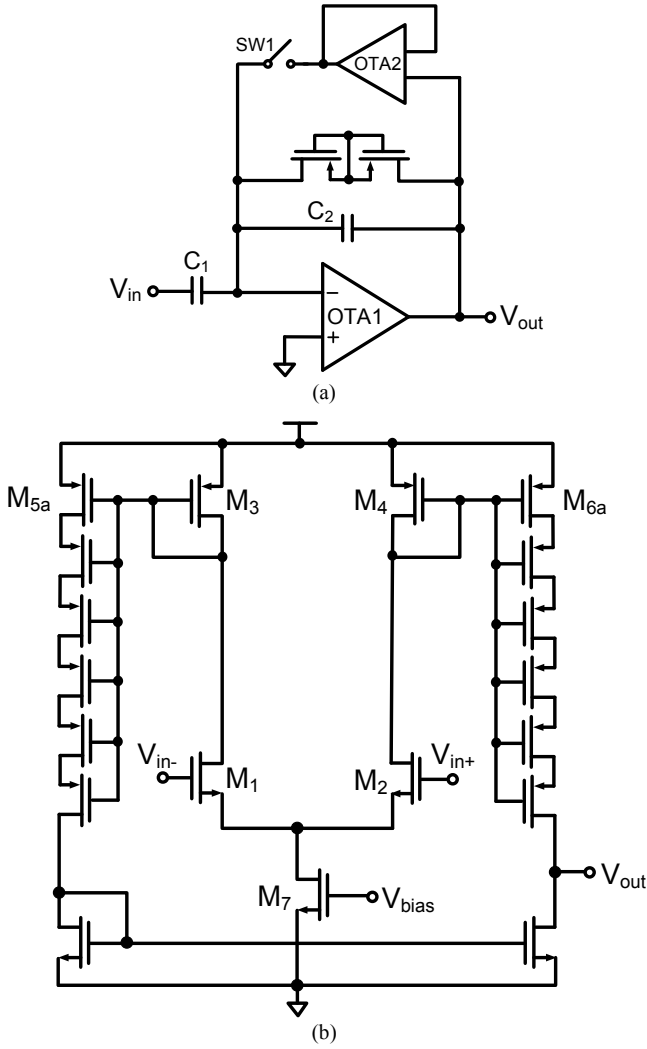


Fig. 7. (a) Schematic of the BPF. (b) Schematic of the OTA2.

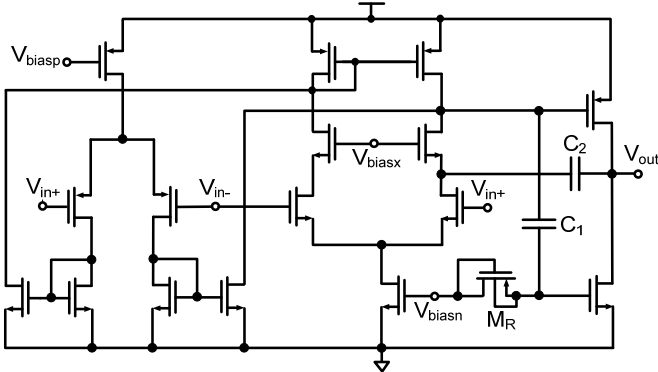


Fig. 8. Schematic of the OTA used in the unity gain buffer.

of the OTA1, and is programmed by the DC bias current of OTA1. The low-pass cutoff frequency can be set at 300 Hz for LFP recording or at 5 kHz to include the neural spikes within the system bandwidth.

The desired high-pass cutoff frequencies for the BPF are sub-1 Hz and 300 Hz to fit the recording bandwidth of LFP and neural spikes respectively. While it is easy to achieve an ultra-low high-pass cut-off frequency by employing the widely

used pseudo-resistors, it is difficult to obtain well controlled 300-Hz cut-off frequency as the resistance generated by the pseudo-resistor is highly susceptible to process variations. In order to solve this problem, an ultra-small- $g_m$  OTA is implemented in the feedback path of the BPF [19] as shown in Fig. 7(a). The OTA2 is connected in unity-gain configuration and designed with very narrow unity-gain bandwidth, such that the signal within the bandwidth of the OTA2 is fed back to the negative input node of the OTA1 and eventually rejected by the BPF. The bandwidth of the OTA2 is determined by its quiescent current, and can be controlled with much higher accuracy than the resistance of the pseudo-resistors. When the switch in series with the OTA2 is disconnected, the high-pass cutoff frequency of the BPF is set to sub-1Hz, which is determined by the pseudo-resistors.

The schematic of the OTA2 is shown in Fig. 7(b). A series-parallel current division structure is used to achieve ultra-low  $g_m$  [20]. The DC current in  $M_7$  is about 2 nA and the  $W/L$  ratio of  $M_3$  and  $M_4$  is 7 times of the  $W/L$  ratio of  $M_{5a}$  and  $M_{6a}$ , and the 6 serially connected PMOS transistors have all identical sizes. This results in a current of about 30 pA in the right and left branches. By using this ultra-low- $g_m$  OTA2, the BPF is designed to have a simulated high-pass cutoff frequency at 300 Hz.

Following the BPF is a unity-gain buffer and its OTA schematic is shown in Fig. 8. Both NMOS and PMOS transistors are adopted for the input pair to achieve rail-to-rail input swing. A class-AB output stage [21] is implemented by using a pseudo-resistor  $M_R$  and a capacitor  $C_1$ . This output topology achieves very large slew rate with small DC current, as the charging or discharging current to the load is not limited by the quiescent current of the output stage. By using the proposed OTA for the unity-gain buffer, combined with the dual S/H structure, only 1.2- $\mu$ A current is sufficient to fulfill the settling time requirement of the ADC. When the recording chain is put into sleep mode, the unity-gain buffer is fully turned off to conserve power.

#### IV. SAR ADC DESIGN

The architecture of the 9-bit alternating SAR ADC is shown in Fig. 9 (a). The ADC mainly consists of four building blocks: a time domain (TD) comparator, a capacitor array, a switch array, and a logic circuit. This 9-bit alternating ADC digitizes ten analog input signals and generates one serial digital output. Based on the proposed dual S/H structure, two S/H channels are implemented. It is achieved using two sets of sampling switches, TD comparators, and capacitor arrays. Only one set of SAR logic is implemented. The ADC first samples the input  $V_{in1}$  from the channel 1 through the switch  $S_1$  onto the capacitor array  $C_{S1}$  while the channel 2 capacitor array  $C_{S2}$  undergoes the bit conversion of  $V_{in2}$ . During the next cycle, the channel 1 will enter the conversion phase and the channel 2 will go into sampling of the next analog input channel according to the timing diagram in Fig. 9(b).

A non-binary redundant algorithm is utilized in the SAR ADC design to improve the accuracy and noise rejection

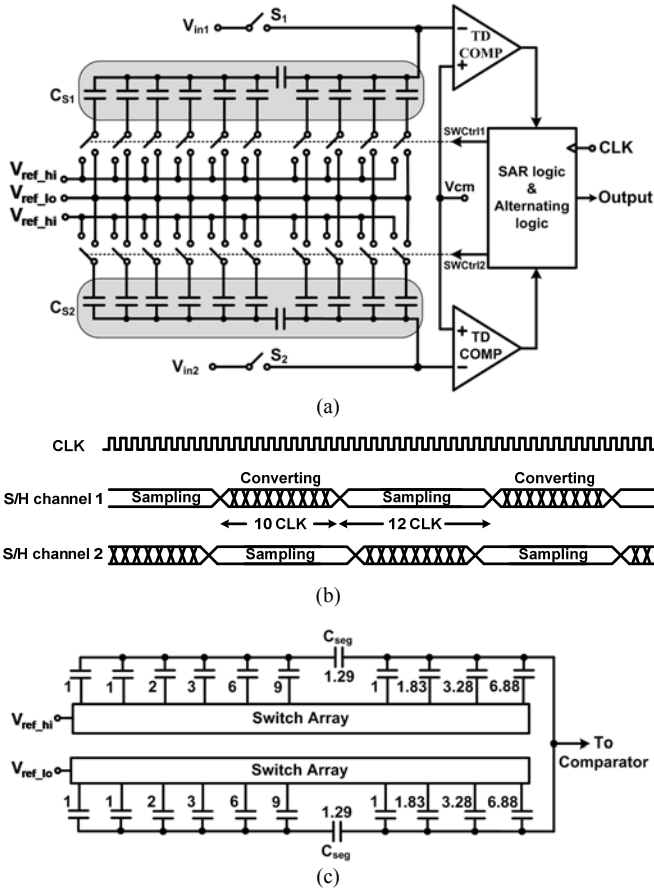


Fig. 9. (a) Architecture of the 9-bit alternating SAR ADC. (b) Timing diagram of the alternating SAR ADC. (c) Architecture of the segmented capacitor array.

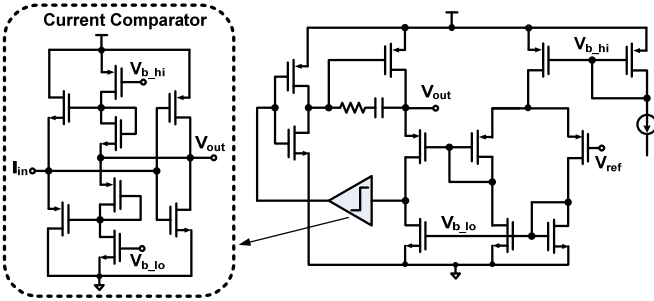


Fig. 10. Schematic of the output-capacitor-less LDO with high-loop-gain current-mode feedback.

performance [22], [23]. One redundant bit is introduced in this design. The capacitors in the array are sized based on the optimum non-binary redundant bit weights obtained through extensive simulation [24]. To reduce the total size of capacitors, the segmented capacitor array is introduced. The unit capacitance used is 0.24 pF occupying the area of 12  $\mu\text{m}$  by 12  $\mu\text{m}$  when implemented by the MIM capacitor. This value was determined considering the noise requirement as well as the parasitic capacitance effect. A time-domain comparator reported in [25] is used to further reduce the power consumption. The reference voltages  $V_{ref\_hi}$  and  $V_{ref\_lo}$  are generated from the 1-V supply using a resistive voltage divider and buffered using a self-regulated voltage reference

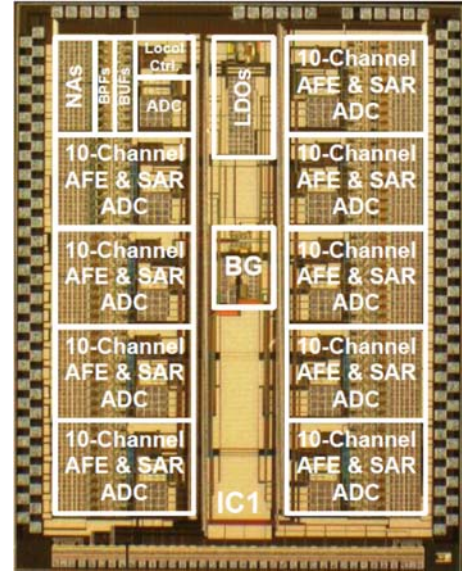


Fig. 11. Die micrograph of the neural interface IC.

buffer [26].

## V. POWER MANAGEMENT

The overall system power is provided by the IC2 via flexible cable, as described in Section I. The rectifiers in IC2 output two levels of DC voltage, which are then regulated by the low-power capacitor-less LDOs in the IC1. As shown in Fig. 10, the LDO has two gain stages in its current feedback loop to increase the loop gain which stabilizes the LDO under low-output-power condition, and non-linear circuits are used to reduce the power consumption. A flipped voltage follower (FVF) structure is utilized to achieve low output impedance and hence loop stability without the need of an off-chip capacitor [27]. However, such a structure has limitation in its loop gain which in turn limits the load regulation performance of the LDO and stability when the load current is very small (e.g.  $< 50 \mu\text{A}$ ). In order to improve the loop gain, a two-stage current-mode feedback loop is introduced. The output voltage variation is converted to current by the FVF and compared with a current reference using a current comparator [28]. The output of the current comparator controls the switching of a thick-gate charge pump to charge/discharge the gate voltage of the output driver MOSFET. The two-stage current-mode feedback improves the loop gain of the LDO to 50 dB.

The current comparator [29] utilizes a source follower as the input stage and a CMOS inverter as the positive feedback to have lower input resistance and short response time. However, there exists a deadband region in which the two input transistors are both turned off and the input resistance is high. In this LDO, the current comparator utilizes the structure in [28] which solves this problem by biasing the input transistors to be always on.

As the input impedance of the current comparator is low, it does not introduce additional low-frequency poles to the circuit. As a result, the LDO remains stable without an off-chip capacitor even at no load current. Since the LDO consists

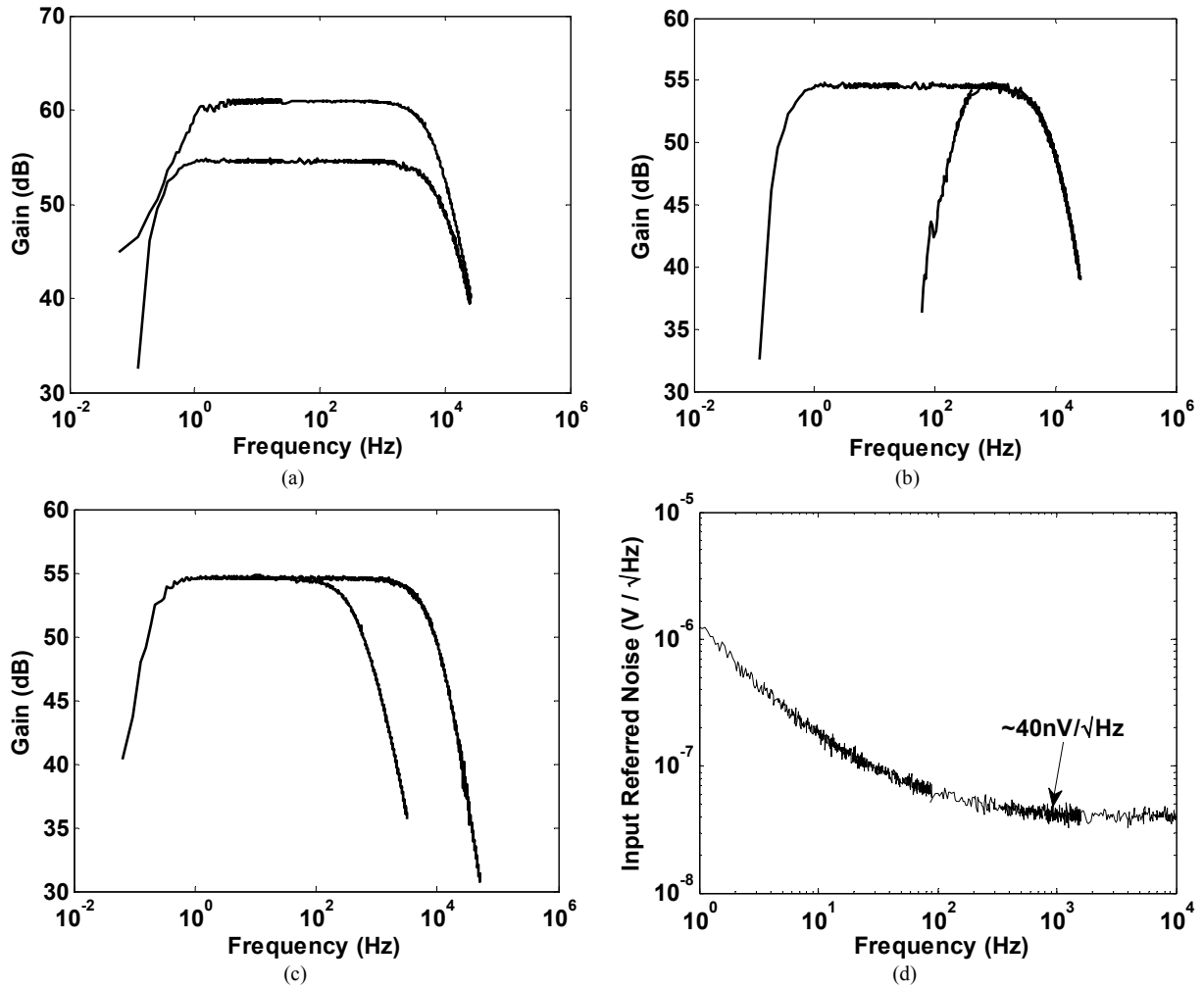


Fig. 12. (a) Frequency response of the full analog recording chain showing programmable gain. (b) Frequency response with programmable high-pass cutoff frequency. (c) Frequency response with programmable low-pass cutoff frequency. (d) Input-referred noise of the full analog recording chain.

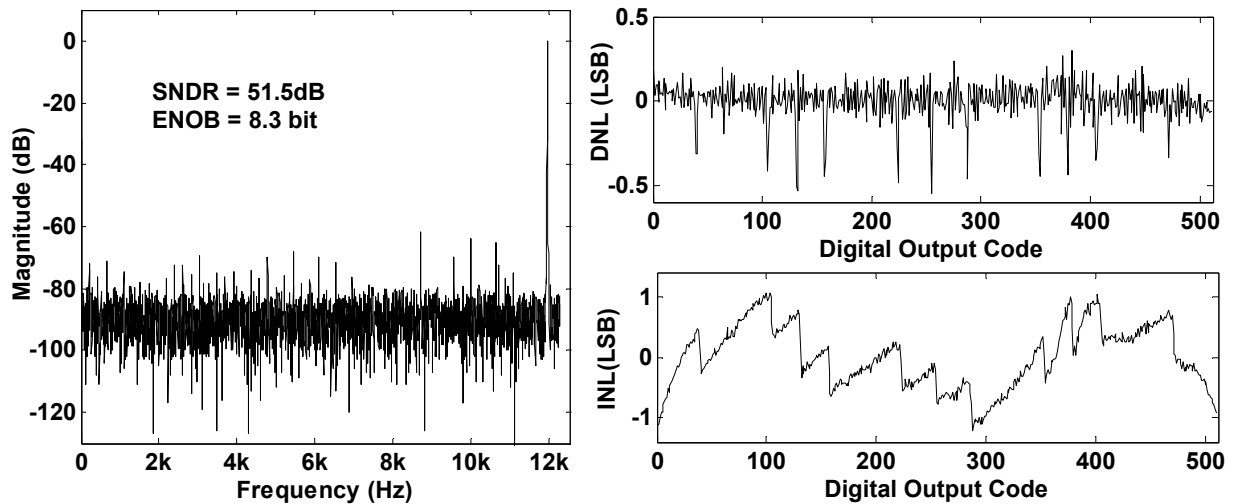


Fig. 13. Measured ADC performance. Output spectrum (SNDR and ENOB) and nonlinearity (DNL and INL).

of non-linear circuit blocks such as the current comparator and charge pump, it consumes very low power and achieves high power efficiency even under low-load condition.

## VI. MEASUREMENT RESULTS

The 100-channel neural recording interface IC has been fabricated using a standard 0.18- $\mu\text{m}$  CMOS process and the

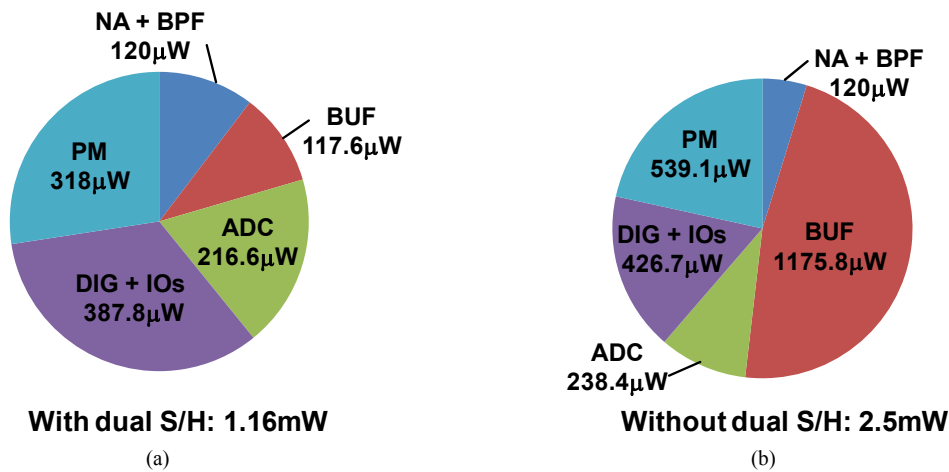


Fig. 14. Power breakdown of the overall neural interface IC with and without dual S/H scheme.

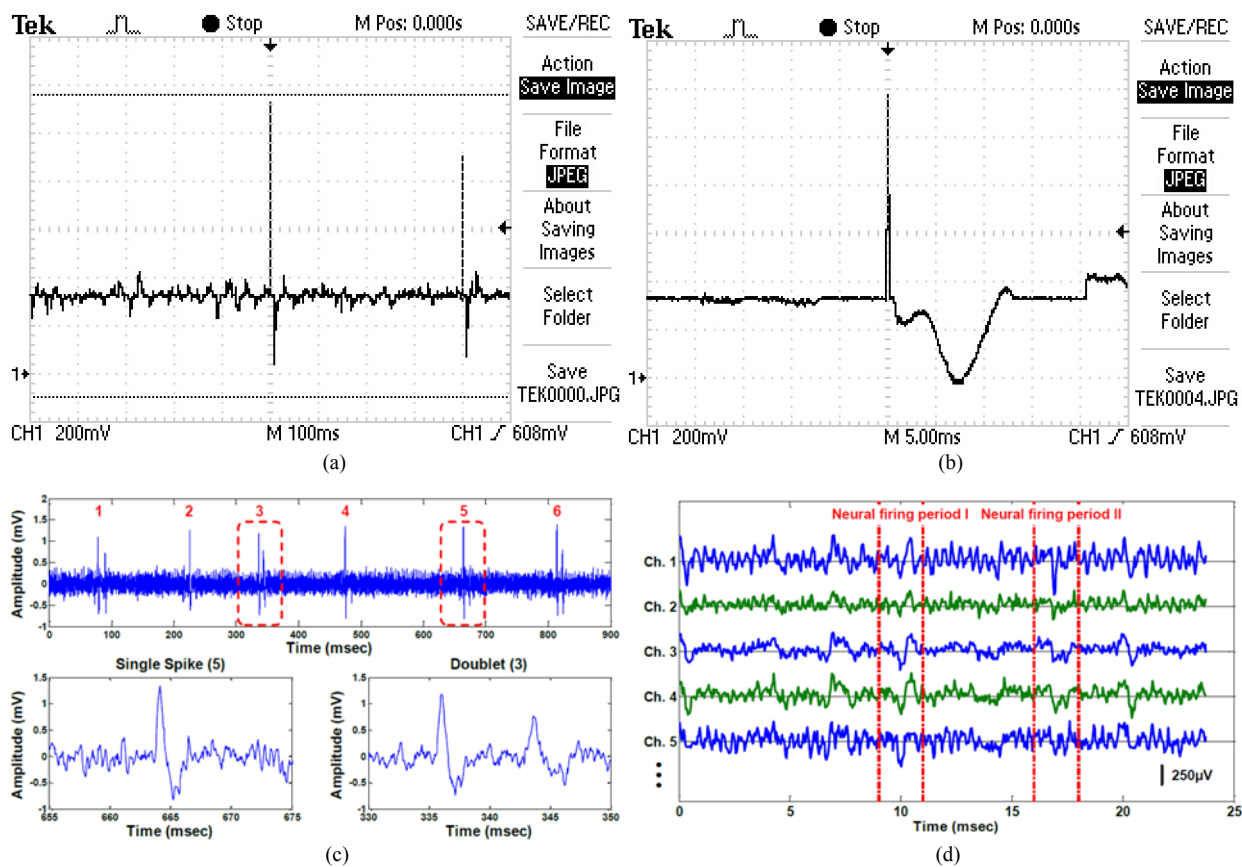


Fig. 15. in vivo testing results of the overall interface IC. (a) Stimulation artifacts and their responses. (b) Zoomed-in stimulation artifact and neural response. (c) Spontaneous neural signal acquisition with a glass electrode from an anesthetized rat. (d) Multi-channel neural signal recording with a NeuroNexus electrode from a freely behaving rat.

die micrograph is shown in Fig. 11. The dimension of the fabricated IC is 4.7 mm by 6 mm, including pads. The system is tested under 1 V for the analog channels and ADC, and 1.8 V for the digital control module. The measurement results of the overall neural interface IC are described in detail in the following sections.

#### A. Analog Recording Chains

The mid-band gain of the system can be set at either 54.6 dB or 60.6 dB as plotted in Fig. 12(a). The measured high-pass cutoff frequency is 0.38 Hz if only the pseudo-resistor presents in the feedback path of the BPF, and it can be altered to 248 Hz when OTA2 is connected. By programming the high-pass cutoff frequency, the LFP signal can be either recorded or removed. The low-pass cutoff frequency of the

TABLE 1. MEASURED PERFORMANCE SUMMARY AND COMPARISON OF THE PROPOSED NEURAL INTERFACE IC WITH STATE-OF-THE-ART DESIGNS.

	Harrison [5]	Chae [7]	Lee [32]	Rabaey [30]	Walker [33]	Chang [34]	This work
Supply voltage (V)	3.3	±1.65	±1.5	0.5	1.2	0.5 / 1	1 / 1.8
Process	0.5 μm	0.35 μm	0.5 μm	65 nm	0.13 μm	0.25 μm	0.18 μm
System gain (dB)	60	57 – 60	67.8 / 78	--	40 / 55	37.5 – 57.5	54.8 / 60.9
High-pass cutoff (Hz)	30 – 1k	0.1 – 200	0.1 – 1k	DC / 300	0.3	0.5 (tunable)	0.38 / 248
Low-pass cutoff (Hz)	5k	2k – 20k	8k	300 / 10k	10k	18k (tunable)	432 / 5.1k
Noise (μV)	5.1	4.9	4.32	4.9	2.2	4.26 / 5.62	4.0 (whole chain)
NEF	--	--	--	5.99	5	5.2 / 1.69*	1.9 (whole chain)
NEF <sup>2</sup> VDD	--	--	--	17.96	30	27 / 2.86*	3.6 (whole chain)
THD	--	--	--	--	--	--	1% @ 0.9-V output
CMRR (dB)	--	90	134	75	--	35	> 60
PSRR (dB)	--	80	62.7	64	--	48	> 70
Sampling rate (ks/s)	15	640	58 – 709	20	31.25	31.25	24.5 – 245
SNDR (dB)	--	--	--	--	60.3	45.14	51.5
No. of bits	10	6 – 9	--	8	10	--	9.5
ENOB	--	--	8.3	7.15	--	7.2	8.3
INL/DNL	0.6 / 0.6	--	--	--	--	0.75 / 0.5	1.2 / 0.55
No. of channels	100	128	32	1	96	16	100
Total power (mW)	4.3 (one ADC)	3	1.2 (without ADC)	0.005	6.5	0.2	1.16 (including loss in power management)
Chip area (mm <sup>2</sup> )	27.7 (one ADC)	51.8	16.2	0.013	25	2.88	28.2

\*The numbers are for the preamplifier only, while the numbers in the proposed design are for the whole analog recording chain.

system is determined by the  $g_m$  value of the OTA1 in the BPF, and can be set at 432 Hz or 5.1 kHz as shown in Fig. 12(c). As a result, the neural spikes and the LFP can be recorded either separately or simultaneously by choosing different bandwidth configurations.

The input-referred noise spectrum of the overall neural recording channel is depicted in Fig. 12(d). The noise floor is about 40 nV/√Hz measured at 1 kHz, and the RMS value of the input-referred noise is 4.0 μV<sub>rms</sub>, when integrated from 1 Hz to 8 kHz. The measured NEF of the whole analog chain is 1.9, which is the lowest to the best of our knowledge. The NEF of the stand-alone neural amplifier will be even lower than this value if the noise from the BFP and the unity-gain buffer is not counted in.

Considering the constantly decreasing operation voltage of the preamplifier, the popular NEF metric has been modified to the following equation [30] [31],

$$NEF^2 \cdot VDD = V_{rms,in}^2 \left( \frac{2 \cdot P_{total}}{\pi \cdot kT / q \cdot 4kT \cdot BW} \right) \quad (8)$$

which is dependent on the power consumption rather than the current. The  $NEF^2 VDD$  of this design is only 3.6, which is much lower or comparable to other state-of-the-art designs, indicating an optimal noise-power trade-off.

### B. ADC

The measurement results of the SAR ADC are shown in Fig. 13. The input dynamic range of the ADC is from 250 mV to 750 mV.  $V_{ref\_lo}$ ,  $V_{cm}$  and  $V_{ref\_hi}$  (Fig. 9(a)) are set to 250 mV, 500 mV and 750 mV, respectively and the clock

frequency for the ADC is set to 540 kHz. Fig. 13 shows the measured signal-to-noise-and-distortion ratio (SNDR), differential nonlinearity (DNL), and integral nonlinearity (INL) performances of the dual S/H SAR ADC for a 12-kHz sinusoidal input. The ADC achieves 51.5 dB of SNDR which corresponds to 8.3 bits of the effective number of bits (ENOB). The DNL and INL of the ADC are ±0.55 LSB and ±1.2 LSB, respectively. The total power consumption of the ADC is 8.39 μW when it supports two analog recording channels. When all of the 10 analog recording channels are activated, the ADC clock frequency is 2.7 MHz and the ADC total power is 21.66 μW.

### C. System Performance

Table I summarizes the performance of the overall 100-channel neural interface IC and makes a comparison with other state-of-the-art designs. All the listed numbers for analog modules of this design in Table I are obtained from the output of the unity-gain buffer. The total power consumption of the overall 100-channel interface IC is only 1.16 mW including the loss in the power management module. The system power allocation with dual S/H scheme is displayed in Fig. 14(a). The power management module takes about 30% of the total power with 70% efficiency. Fig. 16 shows the line and load regulation of the LDO. The LDO achieves a line regulation of 3%/V and a load regulation of 0.6 mV/mA. The 100 analog recording chains consume about 20% of the total power, and the ADCs take about 19%. The rest of power is dissipated by the digital modules, including the digital control blocks, digital buffers and I/O pads. On the other hand, if without the

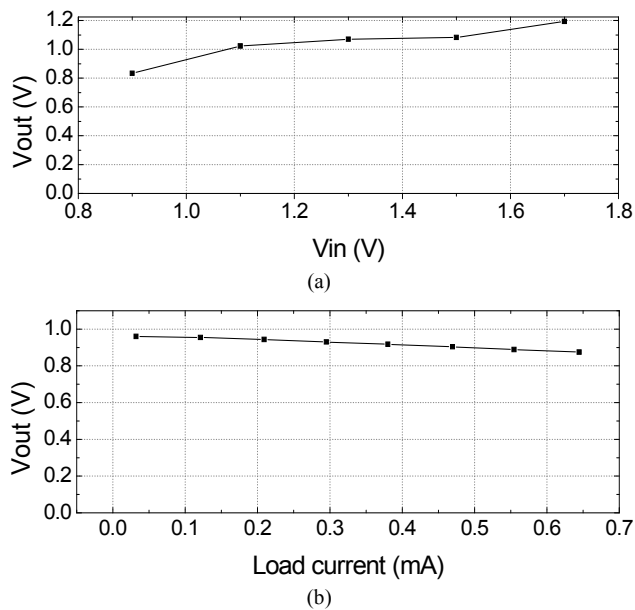


Fig. 16. (a) Line regulation and (b) load regulation measurement results of LDO.

dual S/H structure, the system power can raise up to 2.5 mW as shown in Fig. 14(b), with about 50% of consumption is taken by the unity-gain buffer. This is due to the significantly shortened sampling time of the ADC, which necessitates high driving capability of the buffer. The numbers in Fig. 14(b) are estimated based on theoretical analysis. Compared to the conventional single S/H structure, the proposed dual S/H system architecture reduces the total system power by more than 50% and improves the system power efficiency significantly.

#### D. In vivo testing

To further verify the functionality of the fabricated neural recording system, *in vivo* neural signal acquisitions have been performed. First, field evoked potential recording was carried out and Fig. 15(a) shows the sample recordings from the medial perforant path-dentate gyrus monosynaptic pathway [35]. Two stimulus artifacts with 400-ms interval and the paired pulse inhibition of the negative waveform (characteristic of the dendritic recording in the aforesaid pathway) were illustrated in Fig. 15(a), and the neural response was observed as shown in the zoomed-in picture, Fig. 15(b). Second, spontaneous neural activities were also captured using a glass electrode from dorsal raphe nucleus (DRN), as shown in Fig. 15(c). The biphasic waveform and occurrence of doublets confirms the recording electrode position in the DRN [36]. The above-mentioned experiments were conducted in unconscious rats. Further, multi-channel neural signals were also recorded successfully from nucleus incertus (NI), in a freely moving rat chronically implanted with a NeuroNexus probe. The acquired neural signals are depicted in Fig. 15(d), where neural spikes from the NI [37] are clearly observed.

## VII. CONCLUSION

This paper has demonstrated a mili-watt 100-channel neural recording interface IC. A dual S/H system architecture is proposed which extends the sampling time of the ADC by 10 times and effectively reduces the system power by more than 50% compared to the conventional multi-channel neural recording system. A three-stage analog recording chain was implemented, which helps to achieve optimal system performance. The system was designed with programmable gain and bandwidth so that neural spikes and LFP can be recorded simultaneously or separately. The current-reuse technique and weak-inversion operation are employed to achieve high power efficiency for the neural amplifier, resulting in a system NEF of 1.9, which is one of the lowest among state-of-the-art designs. A low-power ADC with a redundant bit was implemented and a capacitor-less LDO was integrated to complete the functionality of the interface IC. *in vivo* neural signals were successfully acquired using the developed prototype. The optimal system power and small chip area make the developed interface IC especially suitable for fully implantable multi-channel neural recording microsystems [38].

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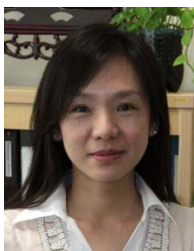
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