# A 100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure

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*Abstract*—**A 100-MHz bipolar operational amplifier has a gain of 100 dB. The op amp owes its high unity-gain bandwidth and high gain to an all-n-p-n signal path and multipath nested Miller compensation (MNMC). The phase margin with a 100-pF load is 40° at 100 MHz and the amplifier settles in 60 ns to 0.1% on a 1-V step. For comparison, a similar op amp without the multipath technique has been realized. The unity-gain bandwidth of this nested Miller compensation (NMC) op amp is 60 MHz and the settling time is 70 ns. Theory and measurements confirm that the multipath technique almost doubles the bandwidth of nested Miller compensated amplifiers.**

## I. Introduction

SPEED or bandwidth demands are generally in conflict with demands on low-frequency accuracy or gain in an operational amplifier (op amp). Op amps consisting of three gain stages to obtain an acceptable dc gain cannot be frequency compensated by conventional means. A widespread compensation method like simple pole splitting is only capable of handling the two dominant poles that occur in two-stage amplifiers.

For this reason, high-frequency bypass techniques are extensively used in high-frequency high-gain amplifiers [1]. In these amplifiers one gain stage is bypassed by a capacitor, short circuiting the stage for high frequencies. This compensation method greatly worsens the settling time of the operational amplifier because of the strong and inevitable pole–zero doublet the feedforward capacitor introduces [2].

A more effective way to compensate an amplifier containing three gain stages or more is by nested Miller compensation (NMC) [3]. This compensation technique nests Miller feedback loops, as shown in Fig. 1. The structure starts off with an output device with a Miller capacitor connected across it. For every gain stage added to the circuit, an additional Miller capacitor is introduced, closing a wider feedback loop.

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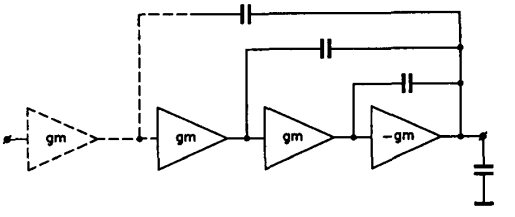



Fig. 1. Principle of nested Miller compensation.

Unfortunately, NMC causes a bandwidth reduction compared to simple pole splitting. The bandwidth halves, for example, when stepping from a two-stage simple Miller compensated amplifier to a three-stage amplifier with nested Miller compensation.

The multipath nested Miller compensation (MNMC) structure proposed in this paper overcomes the bandwidth reduction typical of conventional NMC by introducing an *independent* path for high frequencies. The MNMC structure consists of NMC with a multipath input stage connected in parallel with the regular input stage of the op amp. The multipath stage directly drives the output transistor, bypassing the intermediate stage for high frequencies.

In the ideal case no pole–zero doublets occur, because the multipath input stage can be independently configured from the remainder of the amplifier. In practice, the matching depends on the ratio of transconductances and the ratio of capacitors, both being among the best controlled parameters in a standard IC process.

To take full benefit of the MNMC, the operational amplifier presented is based on an all-n-p-n topology, allowing an extremely high unity-gain bandwidth. Combined with an effective class-AB control, the result represents the state of the art in high-bandwidth precision operational amplifiers.

For comparison, two operational amplifiers have been realized. The first is compensated using NMC and displays a unity-gain bandwidth of 60 MHz with a 100-pF load. The second op amp has an additional multipath input stage, which raises the bandwidth to 100 MHz under the same conditions.

The organization of the paper is as follows. The next section addresses the principle of operation of the nested and the multipath nested Miller compensation structures.

In Section III the two realized op amps are discussed, including the all-n-p-n topology and class-AB control. Section IV gives the experimental results. The paper finishes with the conclusions and references.

## II. Principle of Operation

### A. Nested Miller Compensation

Fig. 2 shows the simplified schematic of a three-stage amplifier with NMC. Fig. 3 is the corresponding Bode plot. It shows the frequency characteristic of the output stage, resulting from $C_{m1}$ and $C_{m2}$.

The output stage has two dominant poles $p_1$ and $p_2$, represented in Fig. 2 by the corresponding resistors and capacitors. Inserting $C_{m1}$ splits the poles, such that $p_1$ shifts to a higher frequency $p_1'$ and $p_2$ to a lower frequency $p_2'$. This is the effect of normal pole splitting, resulting in a well-behaved combination of the intermediate and output stage.

Miller capacitor $C_{m2}$, which closes the second loop, acts on the newly placed pole $p_1'$ and the additional pole $p_3$, the latter being introduced by the input stage. Splitting these two poles results in a straight 20-dB/decade rolloff from the dominating pole frequency $p_2''$ up to the unity-gain frequency $\omega_0$. The Miller capacitors also help reduce distortion by applying all internal gain across the output stage.

The process of pole splitting is further clarified by Fig. 4(a) and (b). These figures show the root loci for $C_{m1}$ and $C_{m2}$, respectively. Pole $p_1'$, positioned by the inner Miller capacitor $C_{m1}$, limits the bandwidth of the op amp. To first order $p_1'$ depends on the ratio of the transconductance of the output stage and the load capacitor $C_l$:

$$p_1' = \frac{g_{m1}}{C_l}. \tag{1}$$

The design criteria for the NMC follow from requiring a Butterworth frequency response from the amplifier with unity-gain feedback:

$$\frac{g_{m2}}{C_{m1}} = \frac{1}{2} p_1' \tag{2}$$

$$\frac{g_{m3}}{C_{m2}} = \frac{1}{4} p_1' = \omega_0 \tag{3}$$

where $g_{m2}$ is the transconductance of the intermediate stage and $g_{m3}$ is the transconductance of the first stage. Expression (2) gives a hint about the dimensioning of a NMC amplifier. The unity-gain frequency of the inner loop, set by the transconductance of the intermediate stage $g_{m2}$ and the inner Miller capacitor $C_{m1}$, has to equal half the limiting pole frequency $p_1'$.

As (3) reveals, the unity-gain bandwidth of the NMC op amp $\omega_0$ is one-fourth of the limiting pole frequency $p_1'$. This is half the value that could be obtained in a two-stage amplifier with simple Miller compensation.

The bandwidth reduction is due to the downward shift of pole $p_1'$ when the outer Miller loop with capacitor $C_{m2}$ is closed. At approximately half its frequency pole $p_1'$ collides with $p_3$. Fig. 4(b) illustrates this effect. Pole frequency $|p_1''|$ obeys

$$|p_1''| = \tfrac{1}{2}\sqrt{2}p_1'. \tag{4}$$

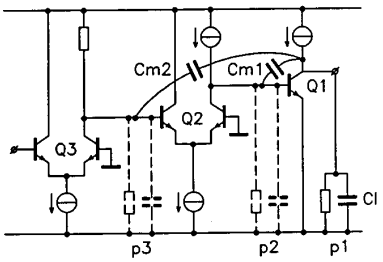



Fig. 2. Three-stage NMC.

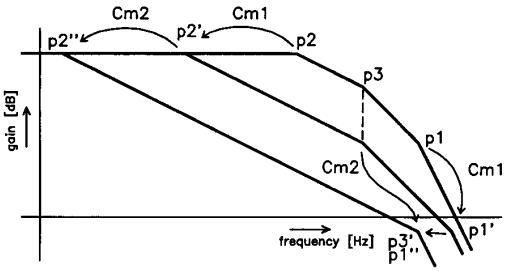



Fig. 3. Bode plot of the NMC structure.

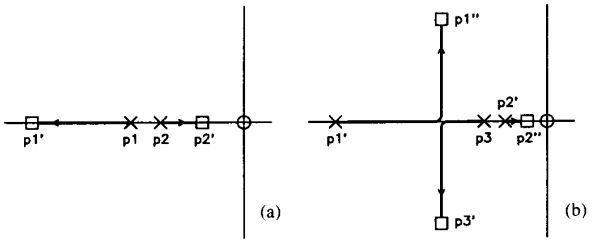



Fig. 4. Root locus of the NMC structure with effects of (a) $C_{m1}$ and (b) $C_{m2}$.

### B. Multipath Nested Miller Compensation

Fig. 5 demonstrates how adding an independent parallel input stage transforms the NMC structure into the MNMC structure. Transistors $Q_1$ through $Q_3$ together with the two capacitors $C_{m1}$ and $C_{m2}$ build up the conventional NMC structure. The multipath input stage is transistor pair $Q_4$. This differential pair directly drives the output transistor, overruling $Q_2$ for high frequencies.

In Fig. 6 the Bode plot of the MNMC amplifier is shown. Drawn as a dashed line is the high-gain low-frequency part established by the three-stage NMC amplifier. The solid line represents the high-frequency part created by the two transistors $Q_4$ and $Q_1$ and Miller capacitor $C_{m1}$. Since this HF part is solely determined by a two-stage amplifier with simple Miller compensation, no

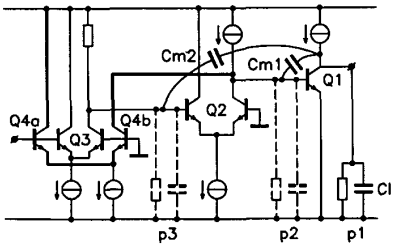



Fig. 5. Multipath NMC.

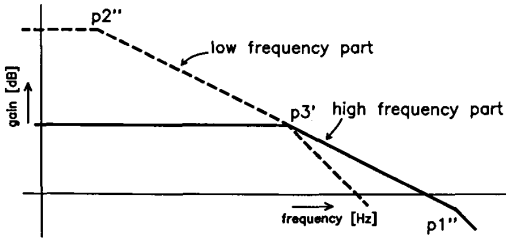



Fig. 6. Bode plot of the MNMC structure.

bandwidth reduction takes place. Matching of the high- and low-frequency parts is easy, as the following analysis confirms.

It is important to note that the multipath input stage adds a zero to the transfer function. The positions of the poles do not change compared to NMC. This makes clear that the dimensioning of the MNMC circuit should be different from the NMC circuit, otherwise the second pole $p_1''$ will stay at its place and no bandwidth improvement is to be expected. The position of pole $p_1''$ with respect to its original position $p_1'$ before closing the second Miller loop is given by

$$p_1'' = \frac{p_1'}{2} + \frac{p_1'}{2}\sqrt{1 - \frac{4\, g_{m2}}{p_1'\, C_{m1}}}. \tag{5}$$

From (5) it follows that the greater ratio $g_{m2}/C_{m1}$ (the unity-gain frequency of the inner Miller loop) compared to the limiting pole frequency $p_1'$, the lower the bandwidth of the circuit. Setting $g_{m2}$ to zero leads to $p_1'' = p_1'$. Obviously, in this case there is no bandwidth reduction, since only two stages are active. A better choice is

$$\frac{g_{m2}}{C_{m1}} \approx 0.1 p_1'. \tag{6}$$

With this ratio, the bandwidth reduction is only about 10% and still three stages contribute to the low-frequency gain.

Putting the multipath zero on top of pole $p_3'$ requires

$$\frac{g_{m3}}{C_{m2}} = \frac{g_{m4}}{C_{m1}} \quad \text{if} \quad \frac{g_{m2}}{C_{m1}} \ll p_1' \tag{7}$$

The condition in (7) is satisfied by (6). As (7) reveals, the matching of the pole and the zero only depends on the matching of transconductances and capacitors.

The position of the doublet is

$$\omega_{pz} = \frac{g_{m2}}{C_{m1}}. \tag{8}$$

Or, with (6)

$$\omega_{pz} \approx 0.1 p_1' \approx 0.2\omega_0 \tag{9}$$

since for a phase margin of 60° the unity-gain frequency $\omega_0$ of the op amp should be half $p_1'$ ($\approx p_1''$).

The root locus in Fig. 7 shows the movement of the poles in the MNMC structure. In contrast to NMC, closing the outer Miller loop only moves the poles a fraction, because of the low value $g_{m2}/C_{m1}$. Pole $p_3'$ is eliminated by the multipath zero.

## III. Circuit Description

### A. All-n-p-n Topology

Fig. 8 is a simplified schematic of the op amp with NMC. To assure a high bandwidth, only n-p-n transistors are present in the signal path. As a consequence, in the push–pull output stage an emitter follower has to be used for the push and an inverting amplifier for the pull transistor. The emitter following $Q_{400}$ has a capacitor $C_{p1}$ connected from its base to ground and the inverting amplifier $Q_{500}$ a Miller capacitor from base to collector. Capacitors $C_{m1}$ and $C_{p1}$ have equal values.

Surprisingly, when driven by a current signal both transistor configurations behave symmetrically [4]. Not only do they have the same transimpedance $z_t$, but also their output impedances $z_{\text{out}}$ are equal.

$$z_t = \frac{1}{sC_{m1}} = \frac{1}{sC_{p1}} \tag{10}$$

$$z_{\text{out}} = \frac{1}{s\beta_f C_{m1}} = \frac{1}{s\beta_f C_{p1}} \tag{11}$$

Because of the differential second stage in Fig. 8, the circuit has a capacitor $C_{p2}$ added to it to balance out Miller capacitor $C_{m2}$.

The level-shift circuit, depicted as a voltage source in Fig. 8, has the characteristics of an all-pass current network [4]. In Fig. 9 the circuit is shown. For input currents there are two separate routes from input to output. For low frequencies the signal goes through the resistor and the p-n-p transistor. For high frequencies the path is through the capacitor and the n-p-n current follower. The crossover frequency $f_{np}$ is set by the $RC$ product. As long as $f_{np}$ is lower than the $f_t$ of the p-n-p transistor, no pole–zero doublets occur, because no current is lost in the all-pass network. The bandwidth of the level-shift circuit equals the n-p-n's $f_t$. The location of the level shift in the circuit is dictated by noise considerations. Situating the level shift directly following the input stage would have increased the noise, because this would mean abandoning the passive collector loads.

The MNMC op amp is largely similar to the NMC op

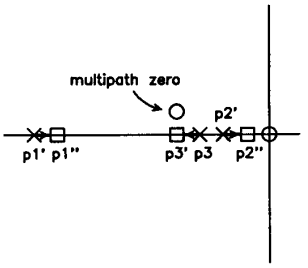



Fig. 7. Root locus of the MNMC structure.

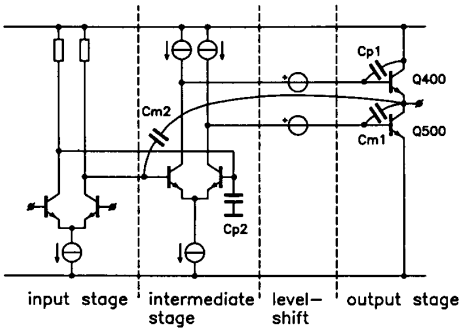



Fig. 8. Simplified schematic of the NMC op amp.

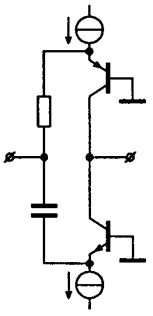


Fig. 9. All-pass level-shift circuit.

amp in Fig. 8. Added is the multipath input stage, as Fig. 10 points out.

### B. Class-AB Control

The feedback class-AB circuit controls the quiescent current of the output stage and prevents cutoff of the output devices by assuring a minimum quiescent current [5].

The control circuitry is independent from the signal path, as demonstrated in Fig. 11. The signal is applied to the output transistors as two differential currents, while the class-AB circuit controls the biasing by two common currents. Class-AB operation does not interfere with the output signal, because the common currents cancel in the output stage (i.e., when one of the transistors is controlled at its quiescent current due to a high output current, the

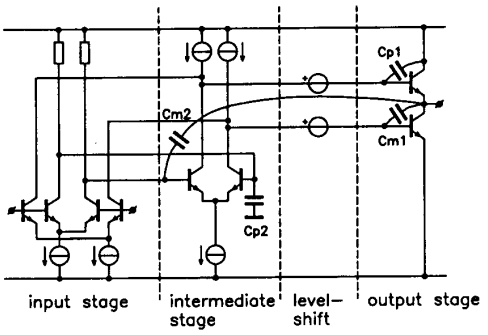



Fig. 10. Simplified schematic of the MNMC op amp.

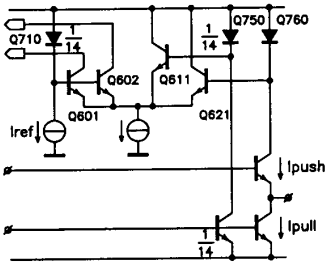



Fig. 11. Class-AB control.

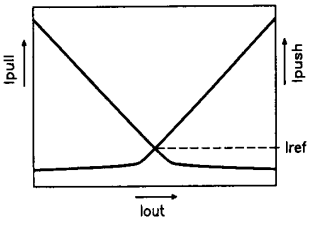



Fig. 12. Class-AB characteristic.

class-AB control doubles the driving of the other transistor).

The class-AB circuit incorporates a combined error amplifier and decision gate. The decision gate, comprising $Q_{611}$ and $Q_{621}$, selects the smaller of the two transistor currents in the output stage. Controlling this current keeps the output transistors from shutting off. The transistors $Q_{611}$ and $Q_{621}$ function as two emitter followers, but only the device corresponding to the lowest output current becomes properly biased. This active emitter follower transfers its input voltage to the common-emitter node of the error amplifier.

The error amplifier consists of the decision gate together with $Q_{601}$ and $Q_{602}$. The input voltages of the decision gate are derived from the push and pull transistor currents by diodes $Q_{750}$ and $Q_{760}$. The reference of the error amplifier is current $I_{ref}$ across diode $Q_{710}$. Fig. 12 shows the class-AB characteristic. The quiescent current is set by $I_{ref}$ and the emitter ratios of the transistors. The minimum value is limited to half the quiescent current.

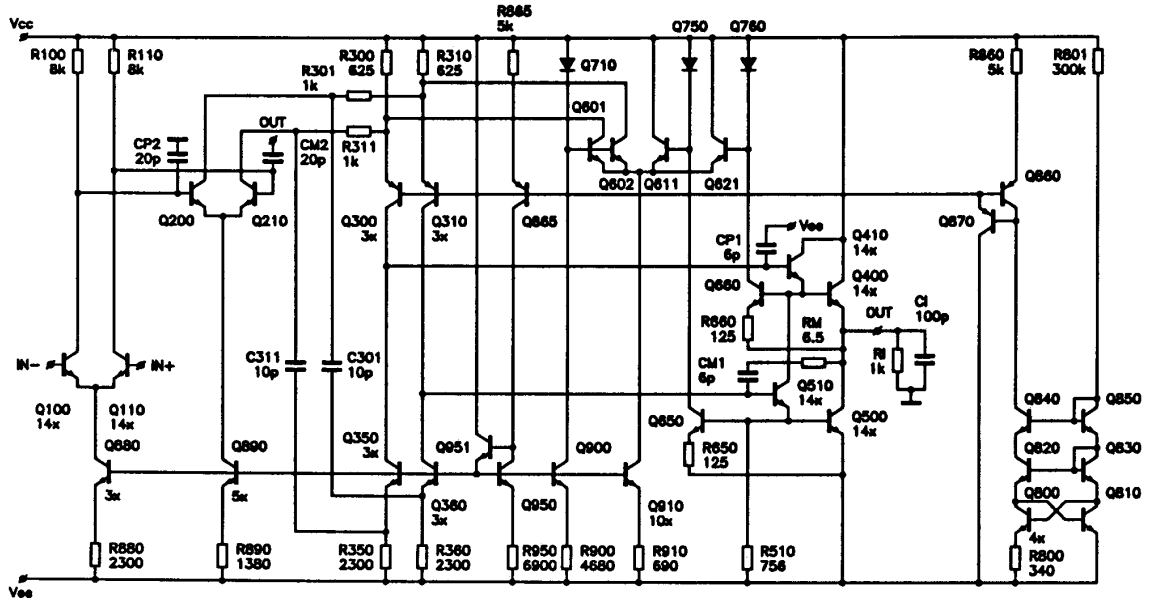



Fig. 13. Total schematic of the NMC op amp.

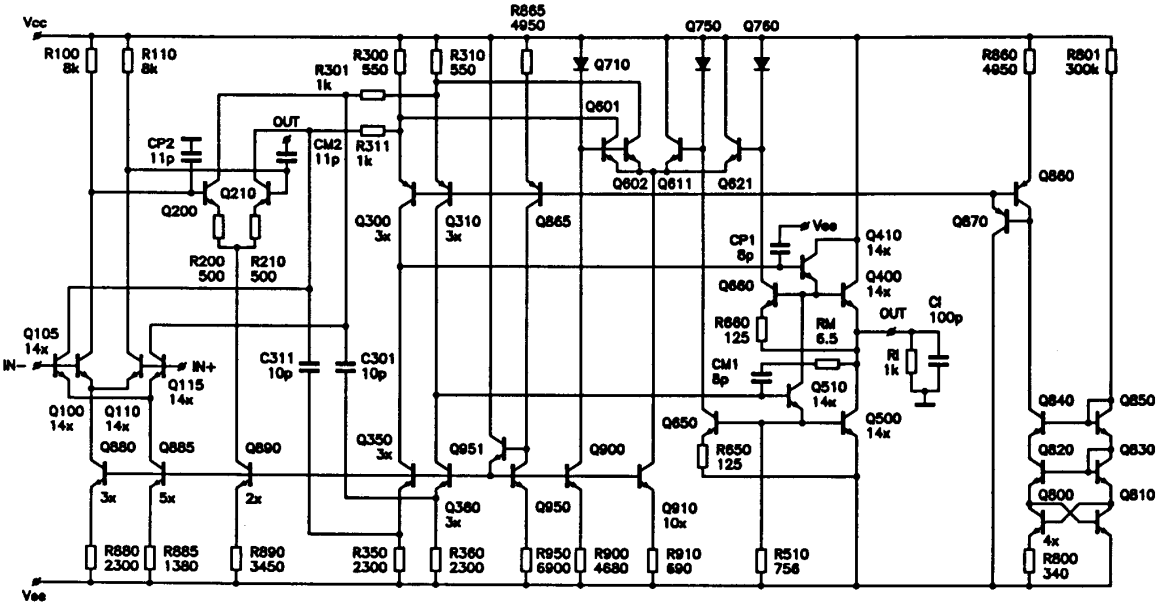



Fig. 14. Total schematic of the MNMC amplifier.

### C. Total Schematic

Fig. 13 shows the total schematic of the NMC operational amplifier. This circuit diagram includes the biasing and level-shift elements. The actual circuit uses Darlington transistors in the output stage to improve the gain. The bias current is generated in the PTAT current source consisting of $Q_{800}$–$Q_{850}$ [6]. Resistor $R_{801}$ initiates a small current in the right-hand branch. Because of the cross-coupled structure, the magnitude of the current is of no consequence to the PTAT output current and start-up is guaranteed. The PTAT current is 100 $\mu$A at room temperature. The quiescent current of the output transistors is set to 4.5 mA.

The MNMC op amp (Fig. 14) is, apart from the additional input stage with $Q_{105}$ and $Q_{115}$, largely comparable to the operational amplifier without the multipath technique. To limit the bandwidth reduction, indicated by (5), the transconductance of the intermediate stage is reduced

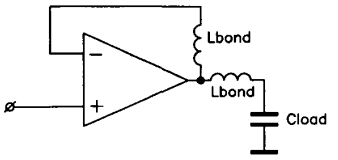
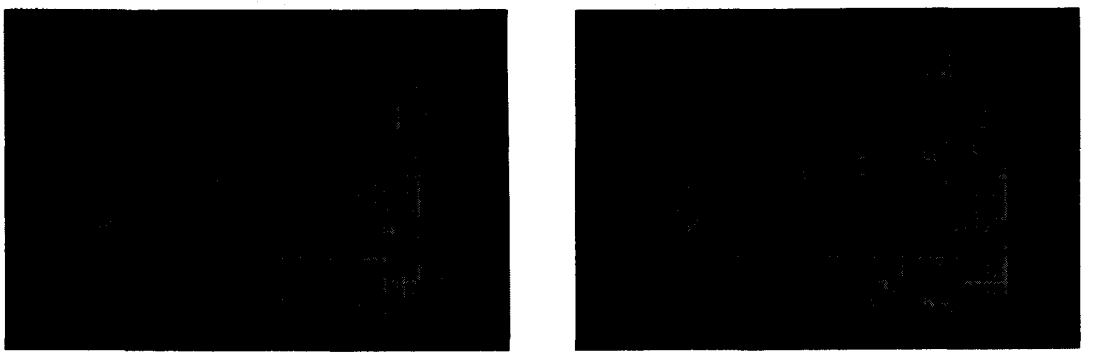



Fig. 15. Separate voltage and current terminals at the output.



(a) (b)

Fig. 16. Photomicrographs of the (a) NMC op amp and (b) MNMC op amp.

by lowering the tail current of $Q_{200}$ and $Q_{210}$ and inserting degeneration resistors $R_{200}$ and $R_{210}$. The doublet frequency, according to (8), is 15 MHz.

The lower tail current of the intermediate stage ensures that, despite the extra input stage of the MNMC op amp, the total supply currents of the two amplifiers are equal.

## IV. Realizations and Experimental Results

The chips were fabricated in a 3-GHz $f_t$ n-p-n bipolar IC process. To be able to drive a 100-pF load with a unity-gain bandwidth of 100 MHz, load and feedback are separated by two output pins and corresponding bond wires (Fig. 15). The pins act as current and voltage terminals and isolate the driving of the load from the feedback path. Without this measure the load capacitance and inductance of the bonding wires would introduce a pair of complex poles in the feedback loop, resulting in instability of the circuit.

Clearly the two output bonding wires can be seen in Fig. 16. Fig. 16(a) is a photomicrograph of the NMC and Fig. 16(b) of the MNMC op amp. The die area of both amplifiers is equal. The extra area needed on the MNMC chip for the multipath input stage is used in the NMC amplifier to accommodate the Miller capacitors. These capacitors are larger due to the lower bandwidth of the op amp. The die area of the chips is 1.2 mm $\times$ 1.5 mm.

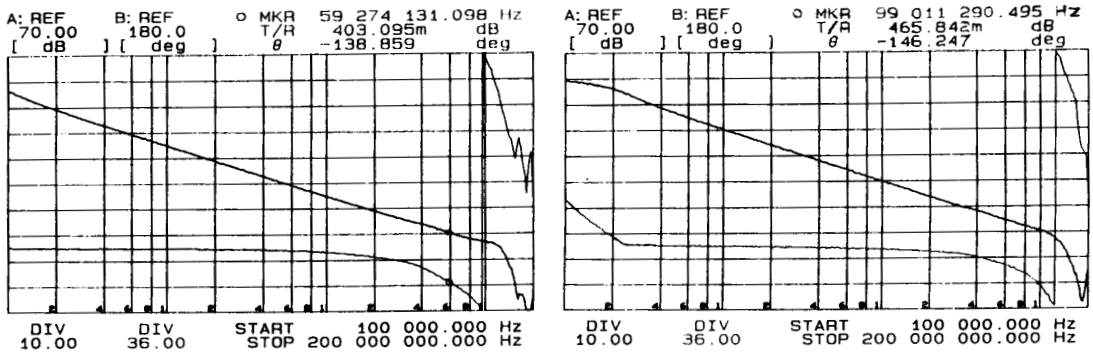
In Fig. 17 the Bode plots of the op amps are shown. The NMC op amp has a unity-gain bandwidth of 60 MHz with a phase margin of 40°C. The unity-gain bandwidth of the MNMC op amp is 100 MHz, with a phase margin of slightly less than 40°. Both op amps are loaded by a 100-pF capacitor in parallel with a 1-k$\Omega$ resistor, as is the case in the following measurements.

Fig. 18 gives the slew response of the op amps to an input step of 1 V. Since the input stages are not degenerated by emitter resistors, the slew rate is determined by the unity-gain bandwidth of the amplifiers. The slew rate of the NMC op amp (Fig. 18(a)) is 20 V/$\mu$s, and that of the MNMC op amp (Fig. 18(b)) is 35 V/$\mu$s.

Fig. 19 gives an impression of the small-signal settling of the amplifiers. The input step is 100 mV. The 0.1% settling time corresponding to the NMC (Fig. 19(a)) is 40 ns. The step response very much resembles the designed for Butterworth curve. As Fig. 19(b) indicates a slow settling component is detectable in the step response of the MNMC amplifier. The doublet spacing corresponding to the slow settling component is approximately 5%. The 0.1% settling time is 50 ns.

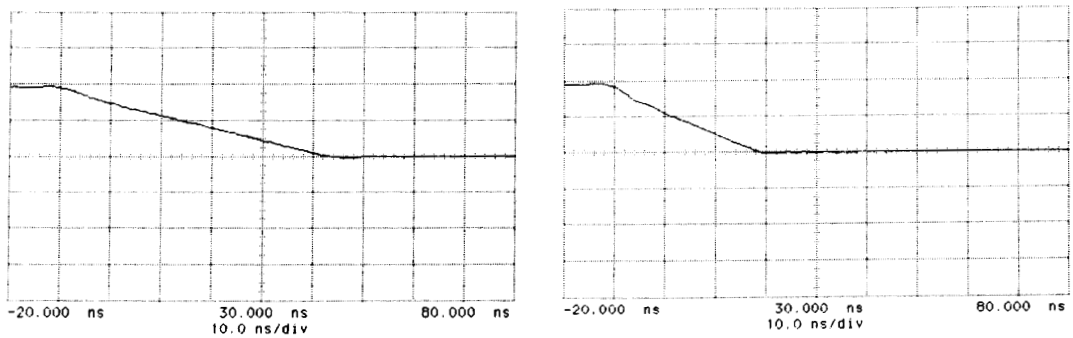
The contribution of the slow settling component to the total settling time becomes relatively less important for large input steps. Because most of the large-signal step response is governed by slewing of the op amp, the MNMC settles faster to 0.1% after a 1-V input step than its NMC counterpart. This is confirmed by the plots in Fig. 20. Settling times are 70 and 60 ns, respectively.

The last plot concerning the two op amps is shown in Fig. 21(a) and (b), which represents the input-referred voltage noise of the NMC and MNMC op amps, respectively. The voltage noise of the op amps is 2 nV/$\sqrt{\text{Hz}}$.



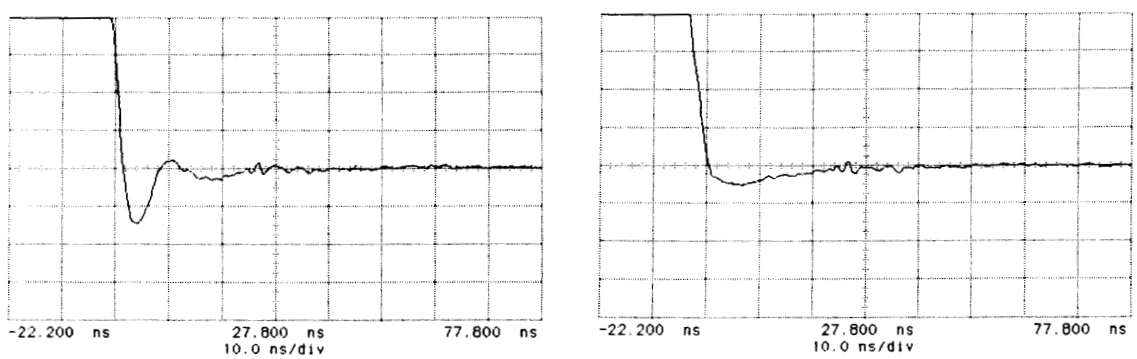

(a) (b)

Fig. 17. Bode plots of the (a) NMC op amp and (b) MNMC op amp.




(a) (b)

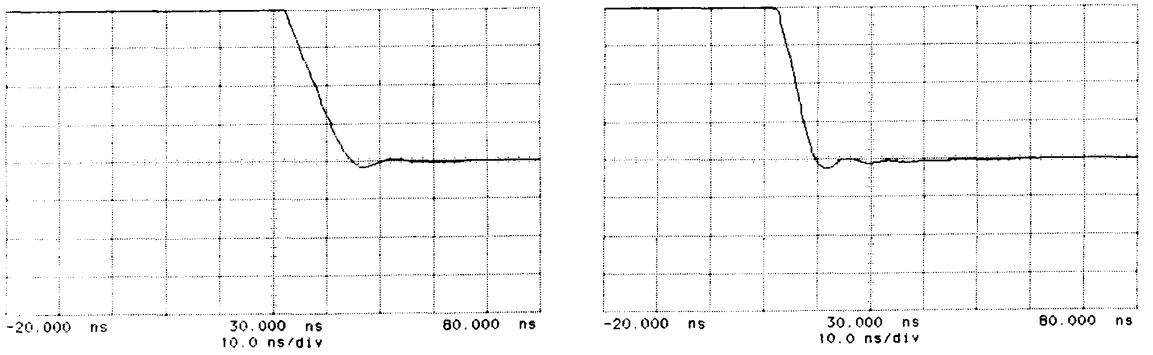
Fig. 18. Slew response of the (a) NMC op amp and (b) MNMC op amp (500 mV/div).




(a) (b)

Fig. 19. Small-signal settling of the (a) NMC op amp and (b) MNMC op amp (5 mV/div).

For frequencies above 15 MHz (the crossover frequency of the multipath input stage) the noise of the MNMC op amps goes up slightly. Because the intermediate stage is not active in this frequency region, noise of the level-shift circuits contributes to the input noise through the multipath input stage. The total input noise is limited to 4 nV/$\sqrt{\text{Hz}}$ over the bandwidth of the MNMC op amp. Table I summarizes the measurement results.




(a) (b)

Fig. 20. Large-signal settling of the (a) NMC op amp and (b) MNMC op amp (50 mV/div).

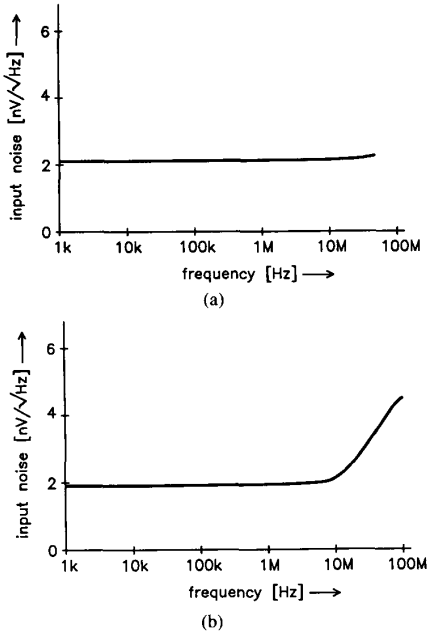



Fig. 21. Input-referred voltage noise of (a) the NMC op amp, and (b) the MNMC op amp.

TABLE I
MEASUREMENT RESULTS

| Parameter | NMC | MNMC |
|---|---|---|
| Unity-Gain Frequency | 60 MHz | 100 MHz |
| DC Gain | 100 dB | 100 dB |
| Settling Time (0.1%) ($V_s$ = 0.1 V) | 40 ns | 50 ns |
| Settling Time (0.1%) ($V_s$ = 1 V) | 70 ns | 60 ns |
| Input Noise Voltage (1 kHz) | 2 nV/$\sqrt{\text{Hz}}$ | 2 nV/$\sqrt{\text{Hz}}$ |
| (50 MHz, 100 MHz) | 2 nV/$\sqrt{\text{Hz}}$ | 4 nV/$\sqrt{\text{Hz}}$ |
| Output Impedance (50 MHz) | 10 Ω | 10 Ω |
| Maximum Output Current | ±50 mA | ±50 mA |
| Supply Current | 9.5 mA | 9.5 mA |

($T_A$ = 25°C, $V_{cc}$ = 8 V, $C_l$ = 100 pF, and $R_l$ = 1 kΩ except where indicated.)

## V. CONCLUSIONS

Nested Miller compensation and multipath nested Miller compensation open the door for a next generation of fast and accurate operational amplifiers. The MNMC amplifier presented drives a 100-pF load with a unity-gain bandwidth of 100 MHz. The multipath technique introduces a well-controlled pole-zero doublet, the matching of which depends on capacitor and current ratios only. In a test chip the doublet spacing was 5%. The unity-gain bandwidth of the NMC op amp is 60 MHz. Since feedforward components are absent in this amplifier, no pole-zero doublets occur. The gain of both op amps is 100 dB.

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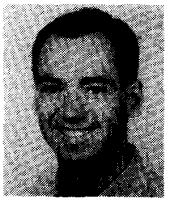

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