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A 1006 ELEMENT HYBRID SILICON PIXEL DETECTOR WITH STROBED BINARY OUTPUT

CERN Detector R&D Collaboration RD19, presented by Erik H.M. Heijne

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Abstract

An asynchronous version of a binary pixel readout circuit has been implemented in an array with 16 columns at 500 μm pitch and 63 rows at 75 μm pitch. This readout chip has been bonded with solder bumps to a silicon detector with matching pixel elements. Event information in a pixel can be strobed into a local memory by a trigger signal and subsequently read out. Without a strobe the information is continuously cleared. The complete hybrid detector has been successfully tested with ionizing particles from a radioactive source. Three such devices have been put in the CERN heavy ion experiment WA94 in the Omega spectrometer where they recorded particle tracks from high multiplicity ^{32}S interactions.

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1. INTRODUCTION

Vertex detection and particle tracking in the inner region of detectors at the hadron colliders SSC and LHC need a precision of ~ 10 μm on coordinate measurements and time-tagging in accordance with the event repetition rate of ~ 70 MHz, i.e. jitter should be < 10 ns. Existing approaches using silicon microstrip detectors with projective geometry can, in principle, satisfy such requirements. However, the occupancy of the detector elements as well as the global pattern recognition problem may be reduced by the use of true 2–dimensional silicon pixel detectors for several additional measurement planes. The average track multiplicity over 4 π in a single interaction (~ 100 for p–p) and the possible occurrence of simultaneous interactions (maybe up to 40 in LHC) do not lead to global occupancy problems. Locally, however, in high P_T jets, related e.g. to charm or bottom production the average core multiplicity is 12 tracks/cm^2 in a plane, at a perpendicular distance of 10 cm from the interaction, with possible rates up to 30 tracks/cm^2. In the forward direction the rates can still be higher [1]. Also in heavy ion interactions a locally very high track density can be expected. One may further note that curling "low" energy particles and conversions from neutrals add considerable confusion in the pattern recognition and increase the number of ambiguities.

From the technical point of view, finer segmentation of detector and electronics offers much lower noise for the same speed, which can be traded against lower power consumption [2–4] or a smaller charge signal. This might eventually allow a thinner sensitive layer for detection, so that the use of cheaper, standard silicon wafers of 150 mm or 200 mm in diameter could be envisaged. The penalty for smaller segmentation consists mainly in increased sophistication of the on-chip information processing electronics, but not in higher production cost.

The gain in time and computation effort for event reconstruction which can be achieved by the use of pixel detectors is hard to quantify at this stage. Previous experience with the CCD pixel detectors in NA32 and with the Si pad detectors in UA2 shows that the importance for pattern recognition of such detectors varies from "very helpful" to "essential" in complementing projective detectors.

Silicon pixel detectors with adequate readout speed, specifically for the hadron collider environment, have not been announced as yet, but earlier development efforts in the framework of the CERN-LAA detector Research and Development (R&D) program already resulted in a small prototype array of pixel elements with 10 MHz, synchronous binary direct readout circuits for a hybrid device [5]. As a continuation to this experience the development program RD19 [6] has been approved by the CERN Detector R&D Committee (DRDC). Besides working on hybrid detectors, the authors collaborate with IMEC Leuven, Belgium, on a monolithic device using Silicon-On-Insulator (SOI) technology.

Improvements to the original binary readout cell [5] have been studied and now an engineering batch of 17 wafers of 4" in diameter has been produced, using the 3 μm p–well SACMOS3 process(*). The complete reticle is shown in fig. 1. It contains again the previous LAA array [5] with a wider edge region to allow ultrasonic wire bonding after the active detector chip has been bump-bonded on top of the readout chip. Another small matrix to test sparse readout is placed alongside. These two arrays will not be further considered here.

The largest silicon area, 8.3 mm × 6.6 mm, is taken by the new prototype array of 16 × 63 active pixels with asynchronous, strobed binary output. An extra row of pixels is added at the top for electrical testing. Another extra row at the bottom is used to sense the typical pixel leakage current in each column, which can be compensated for if needed. In order to allow realistic testing of a complete device, the circuit has been designed to suit the needs of a fixed-target experiment. It has recorded tracks for the first time on 20 October 1991 in the heavy ion experiment WA94 using the ^{32}S beam in the Omega spectrometer.

Several other development efforts in view of high speed pixel detectors for particle physics are in progress, for monolithic solutions notably by the Stanford-SLAC-Hawaii group [7, 8], at Lawrence Berkeley Laboratory [9], and at the Max Planck Institut in Munich [10]. Hybrid devices are under development by an SSC collaboration involving Hughes Aircraft Corp. [11] and at the Rutherford Appleton Laboratory.

(*) The Self-Aligned Contact Metal Oxide Silicon (SACMOS) process is a proprietary process of Faselec AG, Zürich, a subsidiary company of Philips NV, Netherlands.

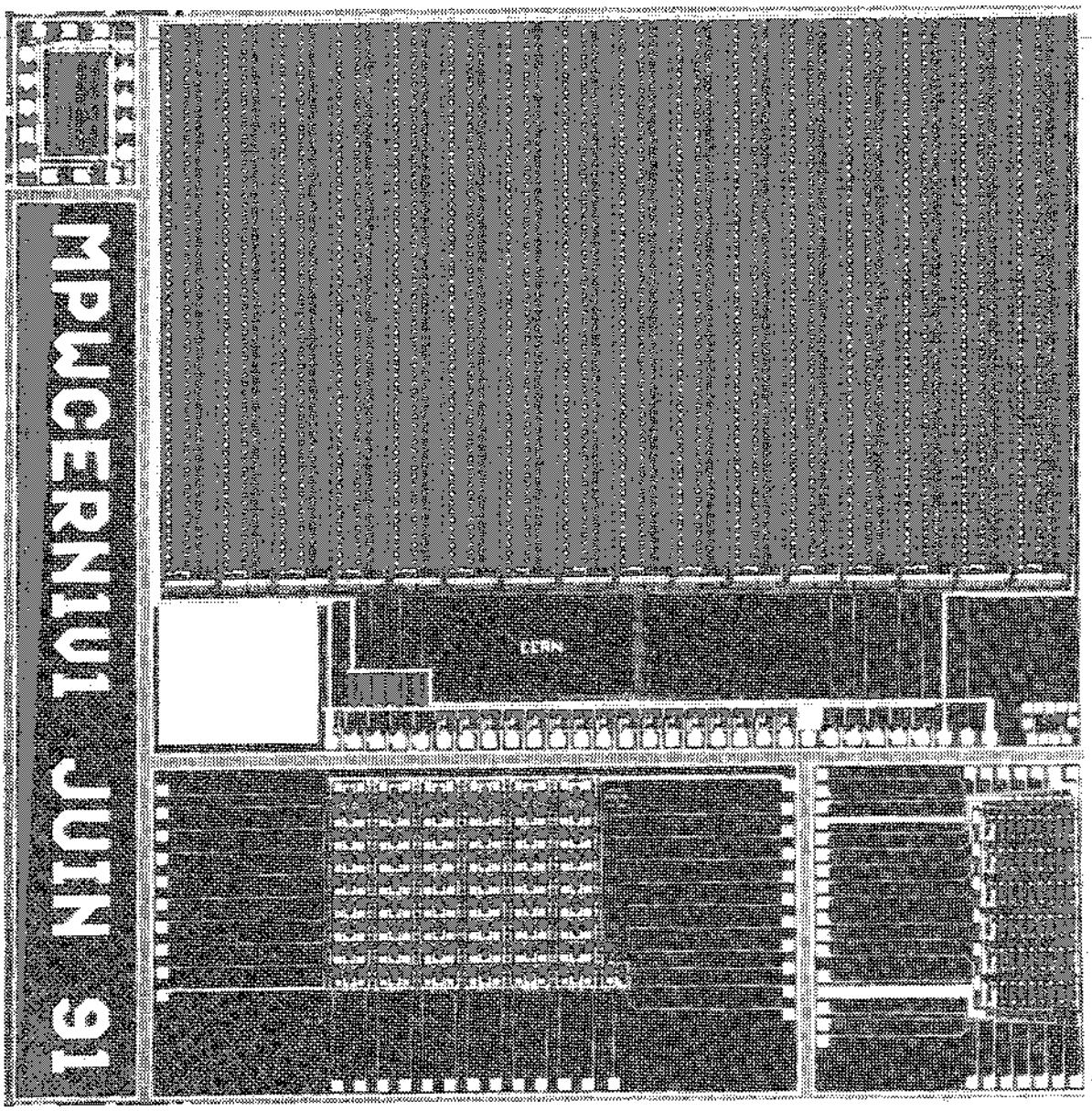

Fig. 1 Picture of the reticle of 9.5 mm × 9.6 mm. The "D Omega-Ion" readout chip takes most of the upper part, the 1988 LAA pixel readout chip is at the bottom left and an array to test sparse readout, made at the Collège de France is at the right.

2. CIRCUIT DESCRIPTION

The layout of a single pixel cell of 75 μm × 500 μm (0.037 mm^2) is illustrated in fig. 2. In comparison with the 0.040 mm^2 cell of the previous LAA design [5] a number of improvements and additions have been made. The signal processing functions contained in each cell are shown in the block diagram of fig. 3. The cell has become more compact through design changes and by the use of a much smaller bonding pad. The array is organized in 16 columns and 64 rows. The binary data from the rows are sequentially clocked out as 16-bit words via parallel shift registers, into an external FIFO memory.

The front-end amplifier and the comparator have been designed according to ideas of Vittoz [3] and Krummenacher [4]. The preamplifier stage is a folded cascode circuit with a small (7 fF) feedback capacitor. Compared with the previous preamplifier design [5] the gain is increased by a factor of 6 to 125 mV/fC in order to diminish the influence of comparator threshold variations.

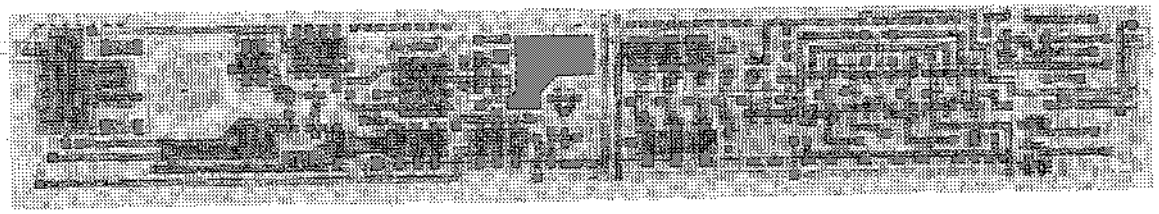

Fig. 2 Layout of a single pixel cell of 75 μm × 500 μm (0.037 mm^2). The bump pad is seen on the left. The digital delay and strobed multiplexer take the right half of the cell.

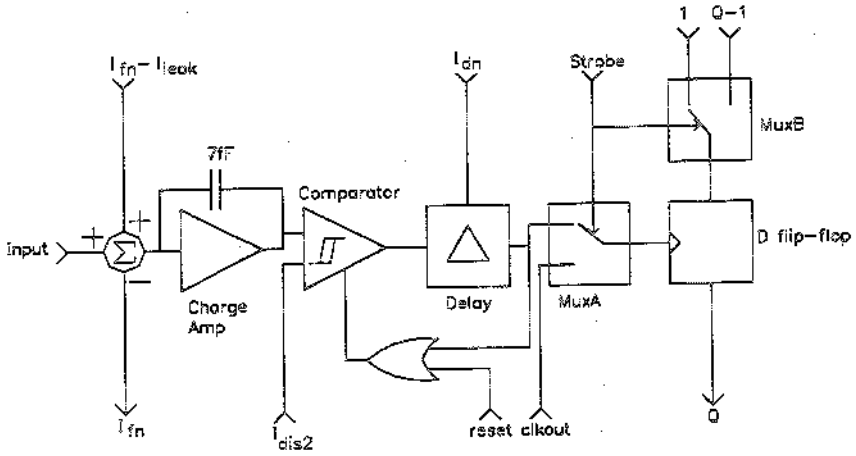

Fig. 3 Block diagram of the pixel readout circuit "D Omega-Ion" corresponding to the layout in fig. 2. The amplifier and comparator are followed by an adjustable digital delay element, a strobed multiplexer and a D flip-flop.

The detector leakage current I_{leak} flows via the DC connection into the preamplifier circuit. In order to compensate for an increase of I_{leak} an extra cell at the bottom of each column contains a circuit that senses the leakage current of a dummy pixel detector cell. This current I_{leak} is subtracted from an external reference current I_{fn} which is initially set at 2 nA. The difference is then used to cancel the effects of the leakage current in each pixel of the column. The reference current I_{fn} has to be adjusted if I_{leak} exceeds 2 nA per pixel, i.e. 2 μA for the detector or 5 μA cm^{-2}.

The 10 MHz synchronous regenerative comparator of the LAA design was replaced by a latched asynchronous comparator in view of testing the pixel array in a fixed-target experiment or with radioactive sources. The principle of operation of the comparator, illustrated in fig. 4, is similar to the previous version. A differential shaper amplifier has a non-linear load which is in turn connected to an output latch. The main difference in the new version is that after reset the comparator stays in the sensitive mode until a sufficiently large input signal causes it to switch. In the old version the comparator was only sensitive for a short time after reset. The threshold of the comparator is determined by the difference of the currents I_q and I_{dis2}. The latter is used to adjust the threshold for the whole readout array between 3000 e$^-$ and 10 000 e$^-$ equivalent input signal. The response time of the asynchronous comparator is simulated to be < 150 ns for the nominal input signal of 10 000 e$^-$. The timing characteristics of the comparator are illustrated in the diagram of fig. 5, together with the additional logical and readout operation.

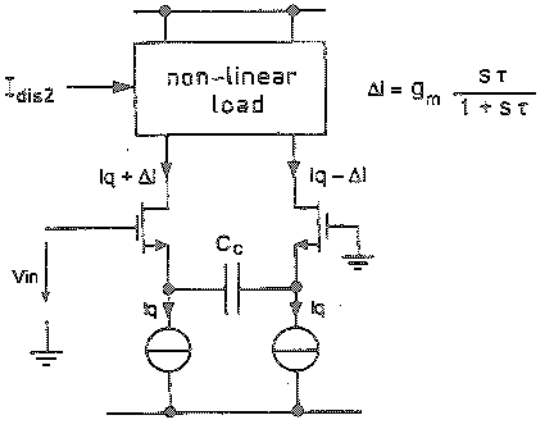

Fig. 4 Schematic diagram of the asynchronous comparator: ΔI represents the signal current, I_q is the standing current, and the threshold adjustment current I_{dis2} is injected in the non-linear load at the top. The coupling capacitor is 0.6 pF.

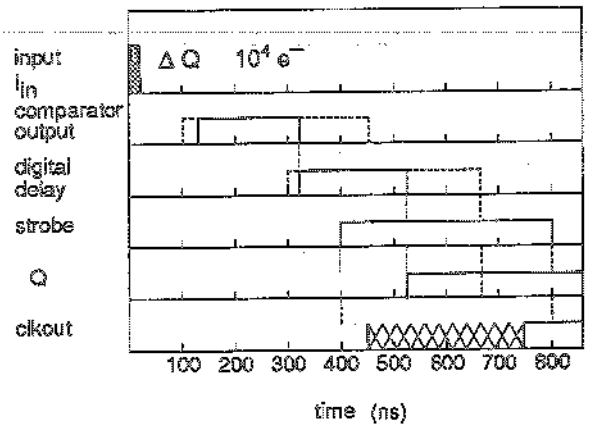

Fig. 5 Timing diagram of the signal processing in the "D Omega-Ion" chip. The uncertainty on the comparator output, found in the first preliminary measurements, is indicated by blocks of dashed lines. The duration of the comparator output and of the digital delay, here 200 ns, are externally adjustable.

To enable the use of this pixel electronics with an external, delayed trigger, some coincidence and readout logic is added to each cell. A digital signal delay is implemented by 3 inverters whose speed is controlled by current source loads. The bias of these current sources is controlled by the I_{dn} input current making the delay adjustable. After a hit is detected in a pixel, this pixel has a dead time of ~ 400 ns. Then it is reset and is sensitive again.

Multiplexer, MuxA, is used to ensure that the falling edge coming from the comparator output is only connected to the clock input of the D flip-flop when it coincides with an external strobe. When the strobe is low MuxB connects all of the D flip-flops of one column together so that by using the "clkout" signal the flip-flops behave as a single shift register.

The readout is controlled by a special CAMAC module, which uses a 1 MHz clock. The total readout time is therefore at present ~ 60 μs. This could be made shorter by using 5 or 10 MHz for the readout, resulting in readout times of 6–12 μs. Ultimately, the readout time will be much shorter by using sparse readout of hit pixels only.

The power consumption of a single pixel cell is designed to be 25 μW at ± 1.5 V power supply.

3. ELECTRICAL MEASUREMENTS

The input pads of the top row of pixel cells are AC coupled to a p-well implant which can be externally connected to a step function generator. The effective input capacitance is 20 fF, so that an electrical pulse of 1 mV corresponds to an injected charge of 125 e^-. This test input can be used also during operation in the experiment to verify the functioning of the complete data acquisition channel for each column. This row of pixel cells cannot be connected to the cells on the detector chip.

Measurements have been made of the threshold characteristics of the amplifier-comparator circuit of the test pixels by varying the input charge signal in small steps. A typical response curve is illustrated in fig. 6. The transition between 2% and 98% response (4 σ) for a single cell takes place over an equivalent charge variation of 240 e^-. Supposing a Gaussian distribution one finds an Equivalent Noise Charge (ENC) at the input of 60 e^-. For detector-connected pixels the input capacitance is higher and so is the noise. The actual value will have to be established by precision measurements with photon sources as described earlier [5]. In this earlier study the noise in the electrical test was higher than in the photon test, in spite of abnormally large input capacitance due to external wire bonding. In the meantime it was found that the correct value for the LAA pixel circuit is 350 e^-, instead of 500 e^-, because of imprecise knowledge of the oxide capacitance. By analogy one could expect now a noise of < 100 e^- for the bonded pixels.

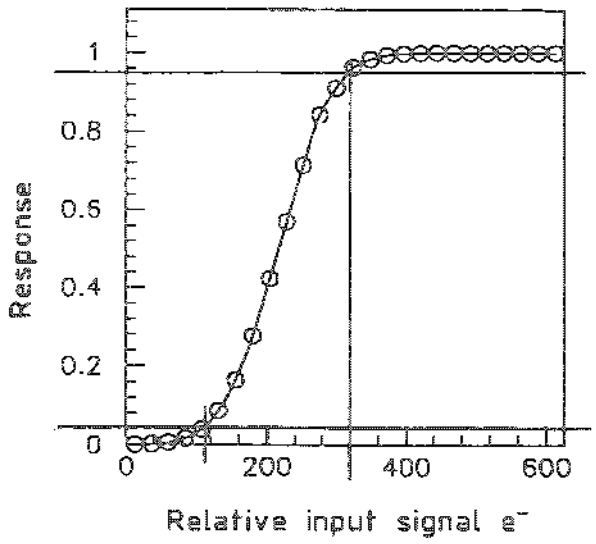

Fig. 6 Threshold curve of a single pixel. The horizontal axis shows the incremental input charge, not the absolute value. The transition from 2% to 98% response occurs over ~ 240 e^- which corresponds to a r.m.s. noise of 60 e^-.

The threshold distribution has been determined for the 16 test pixels for 3 values of the current I_{dis2} which serves to adjust the threshold setting for the entire chip. A minimal average threshold of 2800 e^- is found, with a

r.m.s. spread of 430 e^-, whereas the maximum threshold is situated around 8000 e^- with a spread of 700 e^-. The results are shown in fig. 7.

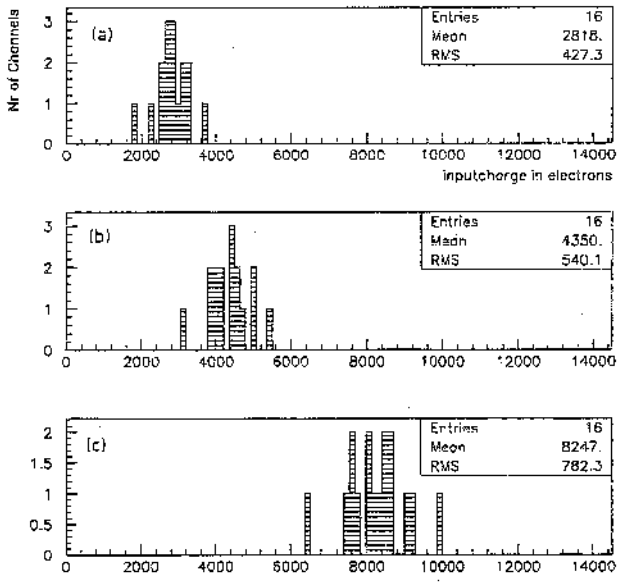

Fig. 7 The distribution of thresholds of the 16 pixels in the electrical test row for 3 values of the threshold adjustment current I_{dis2} and constant I_q. The 50% response point of fig. 6 is used as "threshold" value: (a) corresponds to the minimal threshold setting with 23 μA, (b) is 30 μA and (c) is 44 μA. The input charge is the calculated value in e^-.

The adjustable signal delay has been measured also using the test pixels. The current I_{dn} can be set to vary the delay from ~ 400 ns to ~ 1 μs. The distribution of the delays for the 16 pixels has a slight left-right asymmetry as shown in fig. 8. The cause of this is not understood at present. The r.m.s. variation on the delay times is 27 ns.

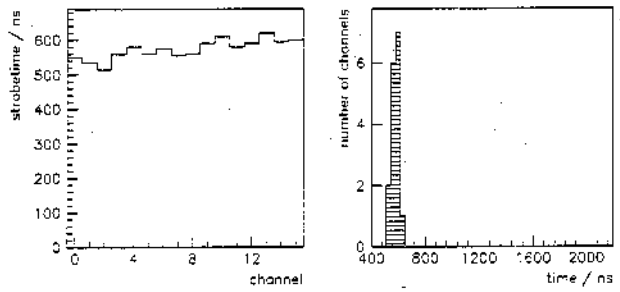

Fig. 8 Digital signal delay distribution for a setting of 9 μA of the adjustable parameter I_{dn} in the right-hand histogram. The mean value of the delay is 560 ns. The left histogram shows the geometrical distribution. There is a slight left-right asymmetry.

A first speed limitation of the comparator is the time slewing, i.e. the variation of the response as a function of the amplitude of the analog input signal. The value found in the first measurements is ~ 50 ns peak–peak for an input charge ranging between 5000 e^- and 20 000 e^-. A second limitation is the spread in propagation time in the comparator. Finally, the response time will also be subject to fluctuations in the propagation time in the digital signal delay. All these factors contribute to a spread in the arrival times of the digital signal in the externally strobed coincidence circuit. This spread was found to be ~ 100 ns for 16 channels tested. Preliminary measurements in the beam show 100% efficiency for the 1006 cell array, even for low signals (4000 e^-) with strobe duration of ~ 400 ns (fig. 5).

4. DETECTORS AND BUMP BONDING

The pixel size on the detector chip is basically determined by the space needed for the electronic functions, and in this project both cells were chosen to be conform in shape, 75 μm × 500 μm. The bottom row of cells on the detector chip is reserved to provide a continuous current signal for the leakage current compensation circuits, discussed in sect. 2. For correct operation of this row a guard ring has been added to the detector matrix. This guard ring is connected to the left and right active cells at the bottom, as shown in fig. 9.

Fig. 9 Bottom left corner of the silicon pixel diode array OD1 that matches the "D Omega-Ion" readout chip. The guard ring is connected to one of the diodes, and the bottom row of cells is used as current reference diodes.

These two cells consequently are not operational for particle detection due to the excessive input capacitance. The active array therefore consists of 63 × 16 – 2 = 1006 elements. Figure 9 is a microscopic picture of a corner of the 300 μm thick silicon detector that

matches the "D Omega-Ion" direct readout chip. The detector chip is passivated and small contact holes, hardly visible, are gold-plated in order to form a wettable solder contact.

The hybrid device is obtained by bonding all inputs of the amplifiers to the contacts on the detector pixels. A solder bump process [12] is used to make the contacts. After deposition of a wettable layer a thick layer of lead and tin is evaporated on the electronics wafer. Where the metal is undesirable, it is removed and the remaining solder is reflowed under eutectic conditions. An enlarged view of a reflowed solder bump is shown in fig. 10. Also on the detector wafer a wettable metal layer is deposited. After the wafers have been sawn and the individual chips have been optically inspected, they are aligned with a special tool, and heated until the solder wets both pads.

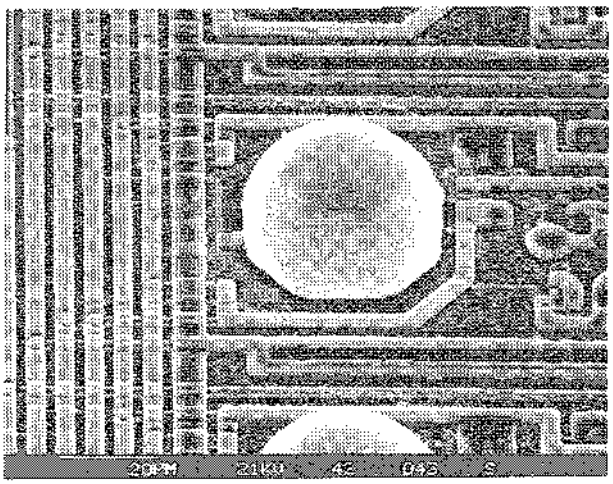

Fig. 10 Photograph taken with a Scanning Electron Microscope (SEM) of a 28 μm diameter solder bump on the input pad of the micropower amplifier.

A total number of 110 devices of various types are produced in this phase of the project, implying nearly half a million bumps to be made. Of the first 9 hybrid detectors which were tested electrically only one was not working. Two devices had a noisy column, but the other 6 were nearly perfect. Although this is rather low statistics, it is very encouraging because we neither tested the detector chips nor even the electronic chips prior to bonding.

The physics applications generally would require at least one dimension of the detector pixel to be as small as possible. The ultimate width that can be achieved will be determined by the size of the solder bumps. The pixel could then be stretched to achieve the total needed area, whereas the electronics cell could have a more convenient shape while covering several detector pixels. This geometry is an improved version to the "short strip" geometry and could, in principle, also be applied to the readout of more conventional microstrip detectors.

5. MEASUREMENTS WITH SOURCES

A first test of the finished hybrid pixel detectors has been performed with a ^{241}Am source, using only the emitted photons. In each case a single column of the device was read out at a time by clocking the shift register content of 64 bits into the sequential memory of a digital oscilloscope. Only pulse trains with at least one bit were accumulated during a certain period. In this way one obtains a hit distribution for the column, as illustrated in fig. 11. Because the spectrum contains besides the 59.5 keV line also photons of 13.9, 17.8, 20.8 and 26.35 keV, which are just situated around the threshold values of ~ 4000 e^-, the counting efficiency varies from pixel to pixel, depending on its actual threshold.

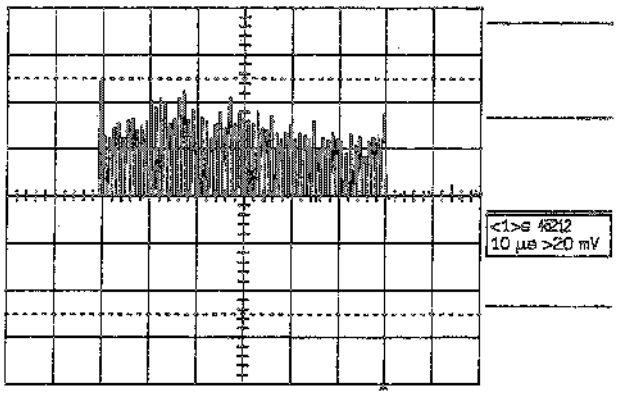

Fig. 11 Accumulation of 45 212 events which occurred in a column of pixels by irradiation with photons from a ^{241}Am source, using a digital oscilloscope. There are no dead pixels but the distribution is quite inhomogeneous due to threshold variation, which just occurs in the 10 keV equivalent energy region, where several X-ray peaks of ^{241}Am exist.

The performance of 6 hybrid detectors has been checked with this source test and apart from a noisy column in two of them, no dead channels have been found. Two more hybrid detectors have been tested in a similar way, but using a laser light spot instead of a source. Those two detectors were both completely functional. Afterwards, the three best hybrid pixel detectors were used for the beam test described in sect. 6. There, it was found that only two pixels were noisy out of the 3018 active cells. No dead pixels were found at all.

6. TEST IN A HEAVY ION EXPERIMENT

Data acquisition CAMAC cards and mother boards for mounting the detector devices in a particle beam had been prepared beforehand. This enabled a parasitic test in the region downstream of the target in the Omega spectrometer at CERN. The host experiment was the Omega-Ion experiment WA94 which is running with a ^{32}S beam of intensity ~ 5.10^5 per spill. The experimental set-up is sketched in fig. 12.

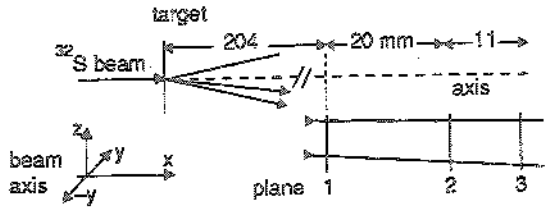

Fig. 12 Vertical view of the topology of the test set-up in the Omega spectrometer, used by the WA94 heavy-ion experiment. The distance between the target and the 3 detectors is not to scale.

Three pixel detector planes were positioned with their centre 11.5 mm below and 3 mm sideways of the beam axis. The distance of the first plane from the target was 204 mm, the other planes followed at 223 mm and 234 mm behind the target centre. Therefore, the detectors detected normally no beam particles but only interaction products coming at an angle from the target. This dip angle is clearly visible in the nice 2-particle event, illustrated in fig. 13.

A large number of events has been accumulated and will eventually be available for off-line analysis of the detector behaviour. On-line analysis was more limited in scope but it enabled scatter plots to be obtained like the ones illustrated in fig. 14, which show correlations in the coordinates. The values of the z-coordinates in the 3 planes are entered on abscis and ordinate for events with one, and only one, hit in each plane. Again the dip angle can be deduced from the shifts of the correlated values. The width of the distributions can be explained by the angular spread of the particles which emerge from interactions in various positions in the target. The width is larger for planes which are further apart. Some random particle positions are found if the "good" particle has a trajectory which must be outside the first or second plane, i.e. the top regions in (a) and (b). These plots reveal some fine structure which has to be studied further in the off-line work.

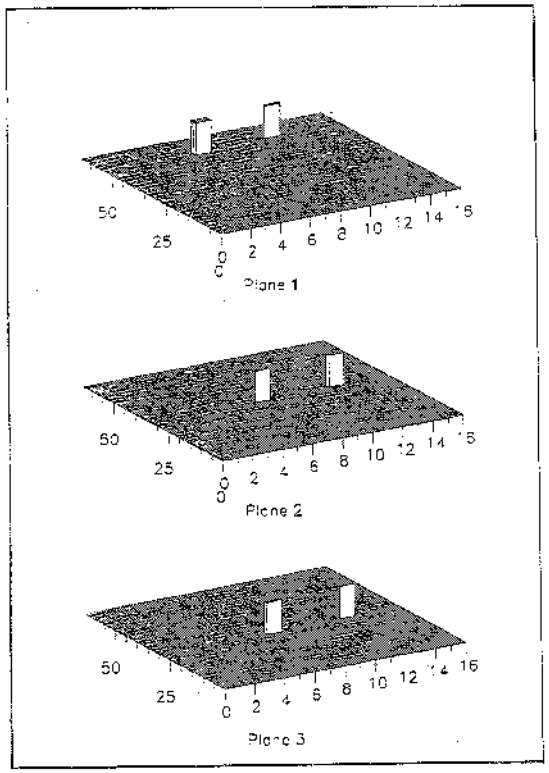

Fig. 13 A nice event seen in the 3 pixel planes. Note the dip angle of the tracks.

7. CONCLUSIONS

Hybrid silicon pixel detectors for Minimum-Ionizing Particles (MIPs) with fast binary response and direct readout for single pixel hits have been demonstrated for the first time in a high multiplicity particle beam. Preliminary data indicate a noise of ~ 60 e^- and a threshold spread of ~ 500 e^-. The timing characteristics are adequate for a fixed-target experiment. For use in future hadron colliders both speed and jitter have to be improved without increasing power significantly and sparse data readout has to be implemented. Such detectors not only could be used for particle detection, but they can also be coupled to scintillating fibres, using an image intensifier or some other mechanism to increase the light output.

The yield in manufacturing is promising so that in the following months composite detector ladders [6] will be mounted using the same type of direct readout chips. This should enable the construction of a module of ~ 4×5 cm^2.

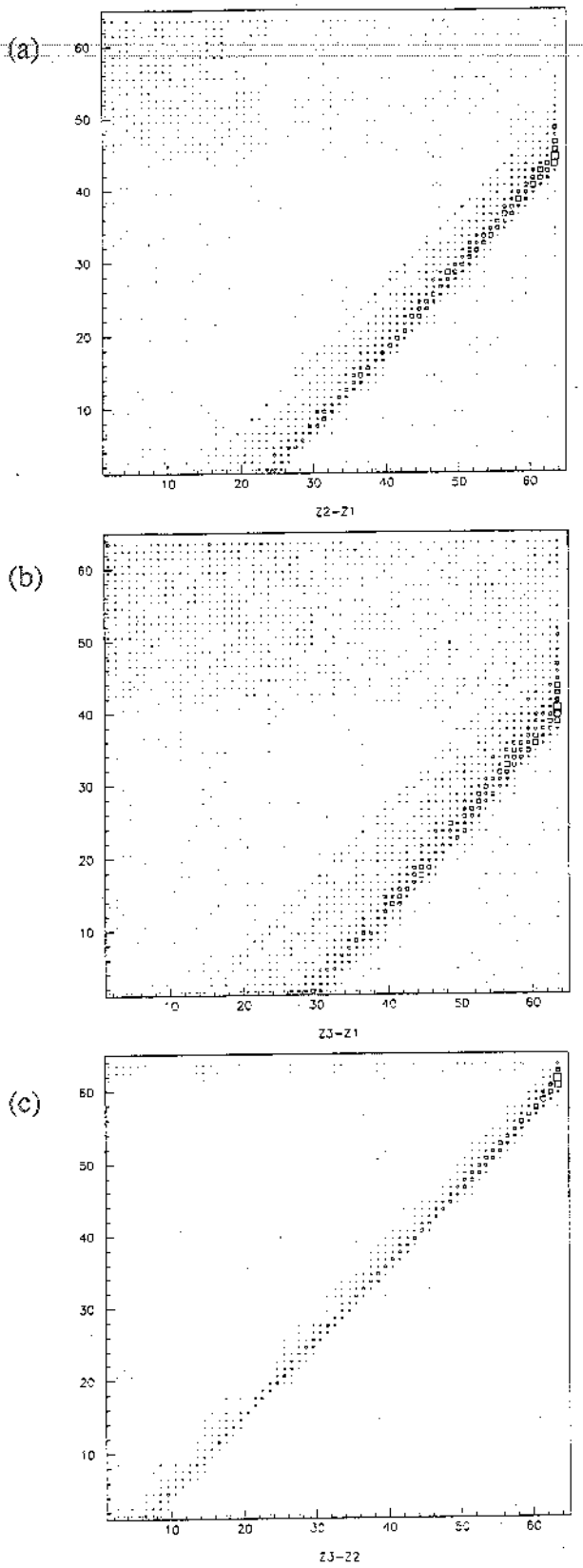

Fig. 14 Scatter plots made on-line for the z-coordinates of particle hits if there was only one hit in each of the 3 pixel planes. The width of the distribution and the background are discussed in the text.

The development of silicon pixel detectors with active low-noise circuitry in each pixel is expected to still take a considerable commitment before all the specifications for the use in LHC or SSC can be met, in particular, the radiation tolerance in the 1–100 kGy range. In the end, however, the complete system presents cost advantages due to easier pattern recognition, reliability, lower power dissipation and longer operational lifetime in comparison with micro-strip detectors with larger area segmentation.

Acknowledgements

It is a pleasure to acknowledge the enthusiastic and effective work of the participants in this project. In particular, should be mentioned the just-in-time contributions of the companies Canberra Semiconductor N.V. (Olen), Faselec AG (Zurich), GEC-Marconi (Caswell) and Smart Silicon Systems SA (Lausanne), and the contract-research institute CSEM (Neuchâtel). The encouragement by the project-referee Dr P. Sharp is much appreciated. The results reported here owe much to the initial effort in the CERN-LAA detector R&D project.

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