A 105-dB SNDR, 10 kSps Multi-Level Second-Order Incremental Converter with Smart-DEM Consuming 280 μW and 3.3-V Supply

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***Abstract*—This paper presents a second-order 3-bit incremental converter, which uses a novel Smart-DEM algorithm for mismatch compensation of multi-level DAC unity elements. The circuit, fabricated in a mixed 0.18-0.5-μm CMOS technology, achieves more than 17-bit resolution over a 5-kHz bandwidth using 256 clock periods. A single-step chopping of the input stage leads to a residual offset of 9.7 μV. The measured SFDR and power consumption are −90 dB and 280 μW, respectively. The achieved Figure of Merit is 177.5 dB.**

I. Introduction

Incremental converters are mostly used for low conversion rate and high resolution. Typical target applications are sensors and instrumentations that require low offset, good linearity and high dynamic range, [1]. An incremental converter has the same scheme of a ΣΔ modulator, but it resets the integrators periodically. The equivalent number of bit of an incremental converter depends on the used number of clock cycles, the order of the modulator, the number of bits used in the quantizer and the digital post processing. High resolution demands for high order modulator. However, when the order of the modulator is higher than two, the stability requirement can limit the effectiveness of the architecture.

An incremental converter can use a single or a multi-bit quantizer. Conventional solutions use a single-bit quantizer, [2]. In this case, the modulator does not suffer from non-linearity of the digital-to-analog converter (DAC). In such a case, however, the integrators experience a relatively large output swing. This may result in operational amplifiers (op-amps) working in slewing mode.

In the case of multi-bit DAC, its non-linearity can be compensated for with static or dynamic calibration methods. For ΣΔ modulators, the well-known dynamic-element-matching (DEM) methods such as DWA, [3], are possible solutions. However, these methods are not suitable for incremental converters. To our best knowledge, very few papers studied this problem. As an alternative solution, the work proposed in [4] is a second-order modulator achieving 18-bit resolution using a 3-bit DAC with inherent linearity.

This paper presents a second-order incremental converter that includes a 3-bit quantizer. The circuit, fabricated in a mixed 0.18-0.5-μm CMOS technology, uses 256 clock periods to achieve a signal-to-noise and distortion ratio (SNDR) of 105 dB. The mismatch of the multi-level DAC unity elements is compensated for by means of a novel Smart-DEM (SDEM) technique. The chosen second-order architecture enables low swing of the operational amplifier outputs and a nearly rail-to-rail input range. The nominal supply voltage is 3.3 V and the measured power consumption is 280 μW. The obtained figure of merit (FoM), applying the Schreier's definition, [5], is 177.5 dB.

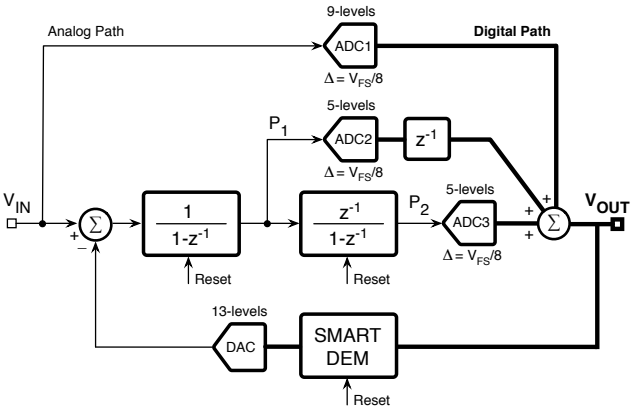

Fig. 1. Proposed incremental converter block diagram.

II. Architecture and Circuit Description

Fig. 1 shows the converter architecture. It is the cascade of two sampled-data integrators (one without delay, the other with delay) with three analog-to-digital converters (ADCs), which digitize the input signal and the outputs of the two integrators. The digital output is the addition of the three analog-to-digital conversions. The quantization step of each ADC is $V_{FS}/8$. For such a second-order modulator, the maximum achievable resolution is

$$R_{2^{nd}-ord} = log_2 \frac{N(N-1)}{2!} + b_q \quad (1)$$

where N is the number of conversion cycles and b_q is the resolution of the quantizer. With $N = 256$ and $b_q = 3$, $R_{2^{nd}-ord}$ is equal to 17.99-bit. The full scale value is 261,120. The used

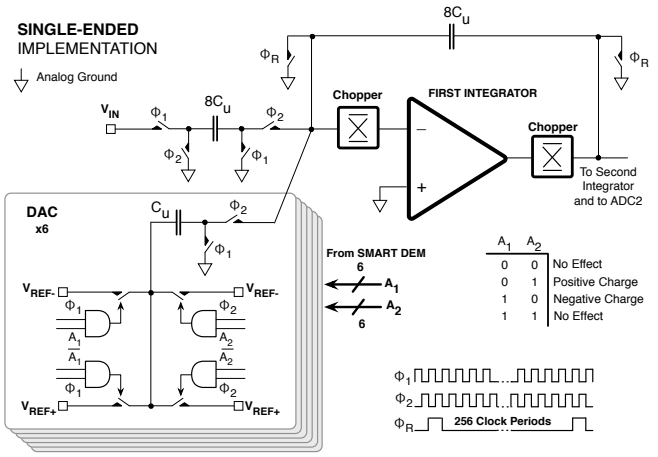

Fig. 2. Converter input stage schematic diagram.

digital feedforward limits the swing at the output of the op-amps. Thus, ADC2 and ADC3 use only 4 comparators. The Smart-DEM block processes the modulator output to properly select the unity elements to be used in the multi-level DAC. Notice that Fig. 1 mimics with digital paths the second order scheme proposed in [6]. The scheme ensures stability and limits the op-amp swings below 0.4-V_{REF}.

A. Chip Analog Section Design

Fig. 2 shows the single ended version of the critical part of the circuit: a chopper amplifier, a switched-capacitor (SC) input stage and the 13-level DAC. The use of a bipolar DAC, shown Fig. 2, enables the employ of only 6 unity elements. The left terminal of each DAC capacitors, C_u, can be connected to V_{REF+} or V_{REF-} either during phase 1 (Φ_1) or phase 2 (Φ_2). As specified by the Table in Fig. 2, controls A_1 and A_2 obtain positive, negative or null injection. Same capacitors and same references make exactly symmetric positive and negative injections. A unity capacitance of 450 fF makes the kT/C noise negligible.

The first op-amp scheme, shown in Fig. 3, is a fully differential recycling folded cascode amplifier, [7], with discrete-time common mode control (not shown in the figure). V_{B1} and V_{B2} are biasing voltages generated by a bias circuit not

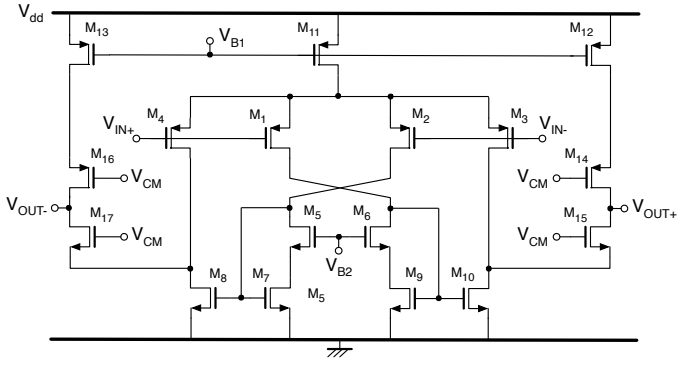

Fig. 3. First op-amp schematic diagram.

shown in the figure while V_{CM} is the common mode voltage. As explained in [7], this scheme, derived from conventional folded cascode implementation, can boost the gain, bandwidth and slew-rate without affecting noise performance or introducing additional offset. The simulated DC gain and GBW are 95 dB and 19 MHz, respectively. The second op-amp is a conventional fully differential folded cascode amplifier with 83-dB gain and 21-MHz bandwidth.

The offset of the first integrator is the main source of the output offset, but even other contributions affect the overall offset. This circuit compensates for all the sources by a single chopping of the input stage, [4]. If a single chopping occurs at the *K-th* cycle out of *N*, the offset of the first op-amp, V_{os1}, reverses while the remaining source, V_{os2}, referred to the input of the second op-amp is unchanged. The input referred offset becomes

$$V_{os,in} = \left[1 - \frac{2(K-1)(K-2)}{(N-1)(N-2)}\right] V_{os1} + \frac{2}{(N-2)} V_{os2} \\ = \alpha_1 V_{os1} + \alpha_2 V_{os2} \tag{2}$$

If $N = 256$ and $K = 181$, the offset of the first integrator is multiplied by a lower value $\alpha_1 = 5.1\text{x}10^{-3}$ while $\alpha_2 = 7.9\text{x}10^{-3}$. V_{os1} diminishes by a factor 196 while V_{os2} is naturally reduced by 127. By trimming the value of *K*, it is possible to obtain a value of α_1 which compensates for both offset sources.

Four-input preamplifiers followed by latches, [8], realize the 16 comparators used by the three ADCs.

B. Chip Digital Section Design

This design cancels the mismatch among elements of the multi-level DAC by using a Smart-DEM algorithm. Let us represent the mismatch for each unity element with ϵ_i ($i = 1, 2, ..., 6$). Since the mismatch sums to zero (otherwise it could be considered as a gain factor), we have:

$$\epsilon_1 + \epsilon_2 + ... + \epsilon_6 = 0 \tag{3}$$

For incremental converters, the error caused by mismatch of DAC depends on the injection time. If an error enters *m* periods before the end of conversion, then the first integrator stores it until the end of conversion. The second integrator accumulates it *m* times, thus leading to an amplification by *m*. Therefore, a given mismatch entered the input, multiplied by the amplifying factor, piles up at output. For negative inputs, error is added to the complementary elements. The total error ϵ_{tot} can be, hence, represented by the summation of the weighted mismatches, which can be expressed as

$$\epsilon_{tot} = W_1\epsilon_1 + W_2\epsilon_2 + ... + W_6\epsilon_6 \tag{4}$$

where W_i are the weights for each mismatch ϵ_i ($i = 1, 2, ..., 6$). During the data conversion, the Smart-DEM algorithm equalizes the piling up of errors by choosing every clock cycle the set of elements with lowest accumulated weights. In other words, the Smart-DEM algorithm balances the W_i, thus

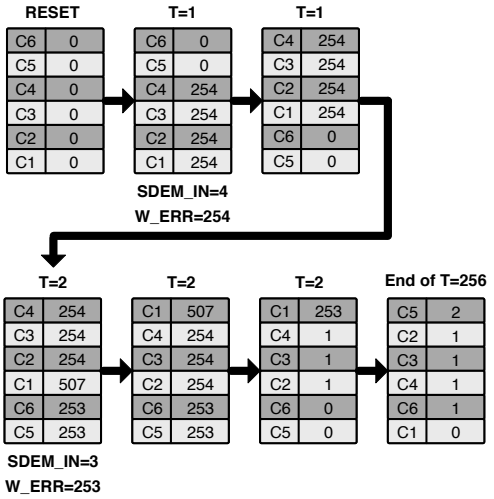

Fig. 4. Example of weights evolution during conversion ($V_{IN} = 0.926V_{REF}$).

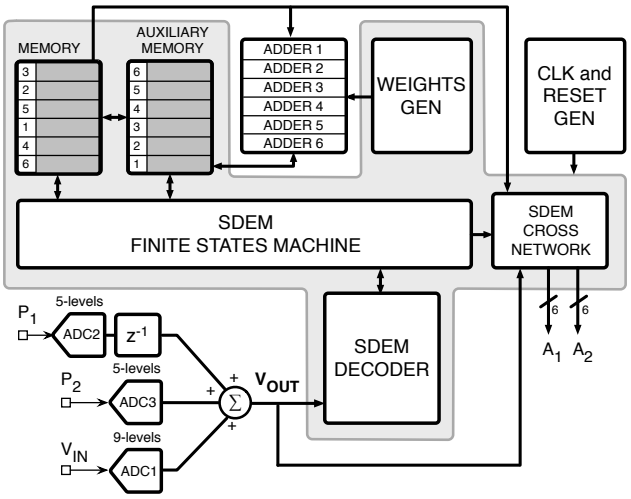

Fig. 5. Smart-DEM block implementation.

minimizing ϵ_{tot}. The ideal case is when all the weights W_i are equal: using (4), ϵ_{tot} is equal to 0. DEM algorithms of $\Sigma\Delta$ modulators transform the mismatch into shaped noise. The same algorithms are not suitable for Nyquist rate ADCs because they use the full Nyquist range.

The flow of the Smart-DEM algorithm is as follows:

1) Before the conversion, reset the weights for all the elements to zero.
2) In each clock cycle, select the unity elements with the minimum weight. If it is the last clock period, jump to Step 4).
3) Update the weight of the selected elements, then go back to Step 2).
4) Conversion finished.

Fig. 4 gives an example on how the weights change inside the Smart-DEM block for $V_{IN} = 0.926V_{REF}$, being V_{REF} the reference voltage equal to 1 V. Before the data conversion starts, the weight of each element is reset to 0. In clock cycle 1, the input of Smart-DEM is 4, which means 4 elements should be used. Therefore, unity elements C1, C2, C3 and C4 are chosen and the corresponding weight 254 is updated. After that, the weight array is sorted and the larger values are moved at the top of the stack. In clock cycle 2, the input for Smart-DEM is 3 and 3 elements with the minimum weight are selected (C5, C6 and C1). However, the corresponding weight of this clock period changes to 253 and it should added to the existing weights. After sorting, the minimum weight in the array is subtracted to all weights to avoid hardware overflow. Finally, after 256 clock periods, the W_i ($i = 1, 2, ..., 6$) is no more than 2 and the total effect of the mismatch is negligible.

Fig. 5 shows the block diagram of the SDEM digital control implemented in this design. The decoder transforms the addition of ADCs outputs into a thermometric representation. Under the control of the finite state machine, the current weights are added to the weights of used elements. The insert-sorting algorithm orders the results, temporarily stored in the auxiliary memory. The minimum of values is subtracted to reduce the required length of registers and returned back to the principal memory. The cross network uses the new order of elements in the next clock period to give rise to the A_1 and A_2 switching controls.

III. Measurement Results

An experimental prototype, fabricated in a 0.18-0.5-μm CMOS technology with dual poly and 6 metal layers, verifies the performances. The analog supply voltage is 3.3 V; the digital section operates with 1.5-V supply. The external reference voltages are 3.15 V and 0.15 V, respectively. The analog sampling frequency is 10 kHz for an analog clock of 2.56 MHz. The digital section (about 1200 gates) implementing the Smart-DEM algorithm runs at 32 times the analog clock frequency. The digital output is the addition of the three ADCs. The measured converter power consumption is 200 μW for the analog and 80 μW for the digital part.

Fig. 6 gives histograms of 2048 repeated measurements on the same part with zero input. The three histograms are for SDEM disabled, SDEM enabled, and SDEM enabled plus one step chopping at $K = 180$. The standard deviation of the histograms measures the input referred noise voltage. It is 1.58 LSB (18 μV) and 0.87 LSB (10 μV) without and with SDEM. Indeed, mismatch increases the inaccuracy. The mean of the

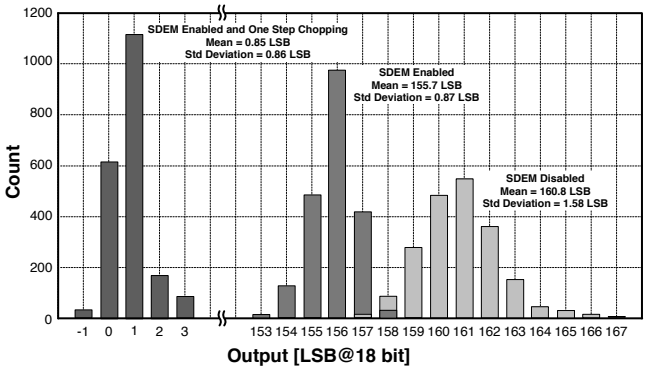

Fig. 6. Histograms of repeated measures with shorted inputs.

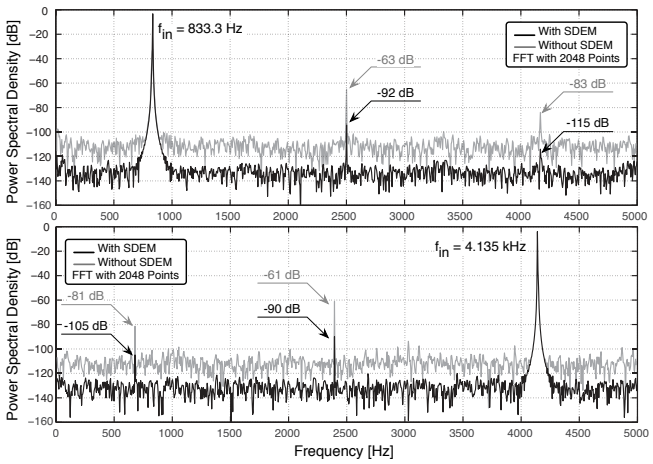

Fig. 7. Measured output spectra.

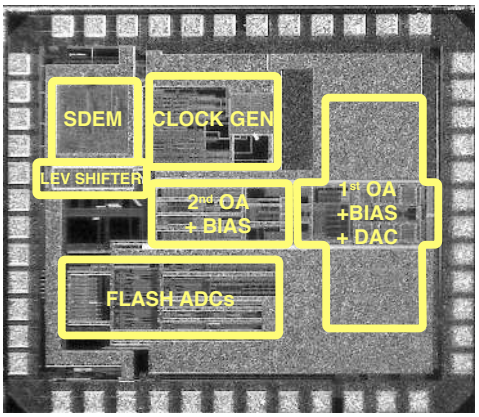

Fig. 9. Chip microphotograph.

histogram measures the input offset (160.8 LSB = 1.84 mV and 155.7 LSB = 1.78 mV, respectively). Again, the mismatch causes the difference. The one step chopping at K = 180 leads to α_1 = 16.1x10^{-3}; the residual offset becomes 0.85 LSB (9.7 μV). The result indirectly estimates a -2.42 mV offset for the second op-amp.

Fig. 7 shows the converter output spectra (FFT with 2048 points) with −2-dB$_{FS}$ sine waves at 833.3 Hz and 4.135 kHz, respectively, with and without SDEM. With SDEM and low frequency, the measured SNDR is 105 dB, equivalent to 17.15 bit. The SNDR at Nyquist drops by 1.3 dB with a loss of 0.22 bit. Third harmonic distortion dominates the SFDR: −92 dB$_{FS}$ with low frequency signal and −90 dB$_{FS}$ when the signal is close to the Nyquist frequency. The fifth harmonic is well below the third one in both cases. As Fig. 7 shows, the SNDR value drops to 82 dB without SDEM and harmonics are significant. The achieved FoM is 177.5 dB, following the Schreier's formula, [5], while it is equal to 190 fJ/conversion-step when using the Walden's expression.

Fig. 8 illustrates the DNL obtained with the sine wave histogram method and an input sine wave of 50-mV$_{pp}$. The limited explored interval results from the memory of the instrument (8Mb). The measured DNL within the [-0.8, 1] LSB range confirms the value of measured SNDR.

The chip microphotograph with main circuital blocks highlighted is given in Fig. 9. The active area is 1270 x 900 μm^2 (the chip area is 1600 x 1300 μm^2). To avoid interferences, a shield of top metal completely covers the DAC capacitive array. The area of the SDEM is 260 x 260 μm^2, only 6% of the active area.

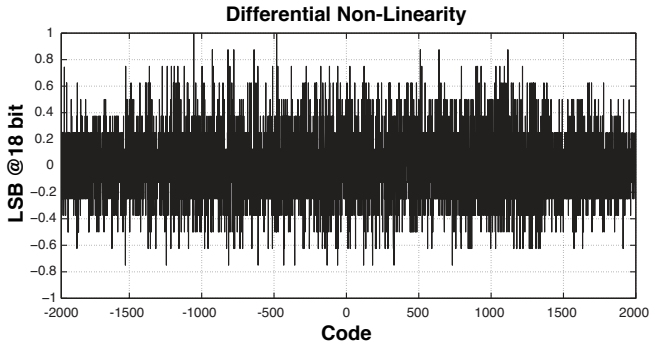

Fig. 8. Measured DNL.

IV. Conclusion

Multi-bit quantization in incremental converters is possible only if the unity elements mismatch is carefully compensated for. Since conventional DEM methods used for ΣΔ modulators are not suitable for incremental schemes, a Smart-DEM algorithm effective for reducing mismatch effects in multi-level DACs of incremental converters is proposed. The technique has been applied to a 3-bit second-order incremental converter. Experimental results show that the circuit is able to achieve a resolution of more than 17-bit over a 5-kHz bandwidth with 256 clock periods while consuming 280 μW. The achieved FoM is 177.5 dB.

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