A 10b 320 MS/s 40 mW Open-Loop Interpolated Pipeline ADC

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Abstract

An open-loop interpolated pipeline ADC is proposed. Weight controlled capacitor arrays are introduced to realize an interpolation and a pipelined operation with open-loop amplifiers. The 10-bit ADC fabricated in 90 nm CMOS demonstrates ENOB of 8.5b over 80 MHz bandwidth (BW) and a conversion rate of 320 MS/s without linearity compensation and consumes 40 mW. The FoMs are 780 fJ/c.-s. defined by the 80 MHz BW and 390 fJ/c.-s. defined by the 320 MSps conversion rate with a BW of 80 MHz.

Keywords: ADC, pipeline, open loop, interpolation and CMOS.

Introduction

A pipelined ADC is suitable for high speed and high resolution conversion, which is required for multi-level modulations, such as 16QAM and 64QAM broadband communication systems. However, the performance has saturated due to insufficient OpAmp gain with technology scaling. To address this issue, techniques using open-loop amplifiers [1] and low-gain and high-speed OpAmps [2] with a digital linearity compensation have been developed. However, they seem to have some issues such as the increase of test cost caused by the long compensation time and the sensitivity to environmental changes.

An A/D conversion scheme that does not require the absolute gain accuracy but only the relative gain accuracy between open-loop amplifiers is an interpolation [3] and a pipelined method [4]. Fig. 1 (a) shows resistor strings method [3][4]; however, it is not suitable for CMOS technology due to static current. Serially connected capacitors shown in Fig. 1 (b) result in higher impedance, a large unit capacitance, and large nonlinearity due to paracitic capacitances. An array of two capacitors connected in series, shown in Fig.1 (c), increases the number of unit capacitance with a rate of $2N^2$, where N is the number of interpolation, and time constant. A weight controlled capacitor array is proposed in this paper. The capacitor array samples the output signals of the amplifiers and adds the stored charges by weighting the capacitance between a pair of capacitor arrays according to the result of the comparison. This method can realize a large number of interpolations with a small number of capacitors keeping the load capacitance constant to shorten the time constant. Furthermore it can cancel offset voltages self-consistently, which is suitable for a pipelined operation.

Circuit description

Fig. 2 shows a block diagram of the ADC. A fully differential scheme is used; however, a single-ended scheme is used in this paper to simplify the explanation. An input signal, V_{in} and a reference voltage V_r are fed to a pair of capacitor arrays and the first four-bit comparators (CMP1) generate the first conversion data and control the switches of the capacitor arrays to be used as a Capacitor DAC (CDAC) to generate residue voltages. The amplifiers A_{1a} and A_{1b} are open-loop amplifiers with a gain of about three. The output signals of these amplifiers are sampled on the interpolation capacitor arrays and compared by the comparators using gate-width-weighted interpolation (CMP2) [5]. The comparators CMP2 generate the second conversion data and control the switches for the interpolation capacitor arrays to generate a pair of interpolated signals. These actions are repeated in a pipelined fashion. The signals after the outputs of the first amplifiers A_{1a} and A_{1b} are composed with weight controlled capacitor arrays. Thus no reference voltage is required unlike conventional ADCs.

Fig. 3 shows a voltage diagram of the output voltages of preceding amplifiers and interpolated voltages. The comparators compare the voltages and divide the output voltages between V_{oa} and V_{ob} into eight equal pieces. The interpolated range covers the range determined by the comparators with overlapping regions. The interpolated voltages are composed by the sum of capacitive weighted voltages; V_{oa} and V_{ob}. Fig. 4 shows the capacitor arrays of the interpolation circuits. The input signals, V_{ia} and V_{ib}, are amplified and the output voltages, V_{oa} and V_{ob}, are sampled on all the capacitors. In the next phase, each capacitor is controlled to be connected to the input terminals of amplifiers or to remain connected to ground by the comparison. Fig. 5 shows the equivalent circuit of the capacitive interpolation. C_{a1} and C_{a2} represent the capacitors connected to the input signal terminals and C_{b1} and C_{b2} represent the capacitors connected to ground. The interpolated voltage V_x is

$$V_x = -\frac{C_{a1}G_a(V_{in} - V_{ra}) + C_{b1}G_b(V_{in} - V_{rb})}{C_{a1} + C_{b1}} \quad (1)$$

The input offset voltages, which reduce the linearity, are canceled and the accurate interpolated voltages can be generated if the gains of amplifiers are sufficiently similar. The first amplifiers use the differential CMOS amplifier with source degeneration resistors, as shown in Fig. 6, and the other amplifiers use a simple differential amplifier.

Measurement results and conclusion

The chip is fabricated in 90 nm CMOS technology and occupied area is 0.46 mm^2, as shown in Fig. 7. The supply voltage is 1.2 V. The power consumption is 40 mW (24 mW for the analog and 16 mW for the digital) at a conversion rate of 320 MS/s. Fig. 8 shows the measured results. INL and DNL are +1.4/-1.75 LSB and +0.96/ -0.61 LSB, respectively. SNDR of 53 dB is measured up to 320 MS/s. Also, SNDR of 53 dB is obtained up to f_{in} of 80 MHz. The FoM of 780 fJ/c.-s. defined by the BW and 390 fJ/c.-s. defined by the conversion rate of 320 MS/s with the f_{in} set as a quarter of f_s, which is the upper effective input frequency for communication systems, are obtained. Table 1 summarizes and compares the performances.

The circuit implementation of the proposed conversion architecture should be optimized; even so, the use of open-loop amplifier will be demanded for further scaled CMOS with low voltage operation and an excessive requirement for linearity compensation should be relaxed. As a result, the proposed method is worthy of consideration as a future ADC architecture.

Acknowledgements

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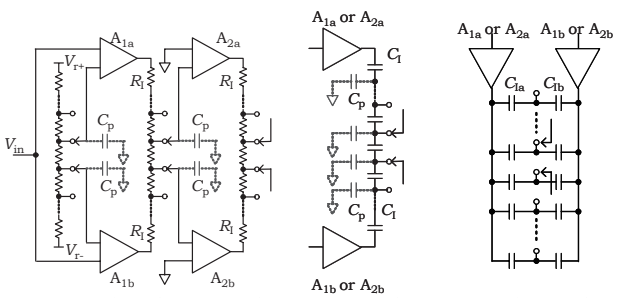

(a) Resistive interpolation [3] [4]. (b) Capacitive interpolation by series capacitors. (c) Capacitive interpolation by weighted capacitors.

Fig. 1. Conventional interpolation methods.

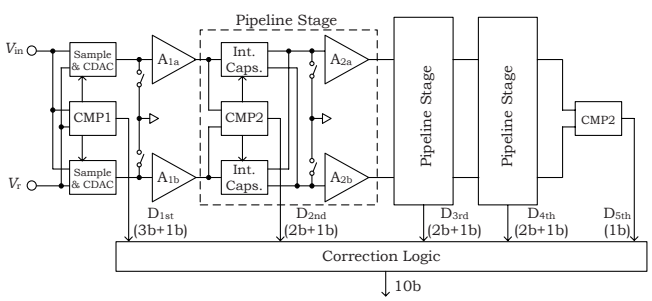

Fig. 2. Functional block diagram of proposed ADC.

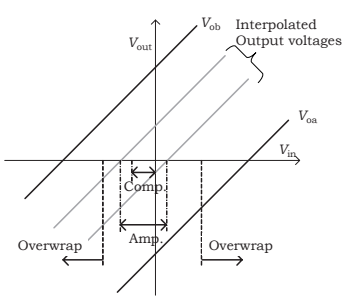

Fig. 3. Voltage diagram.

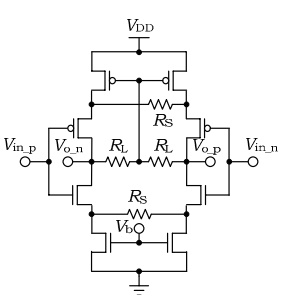

Fig. 6. CMOS diff. Amp. (A1).

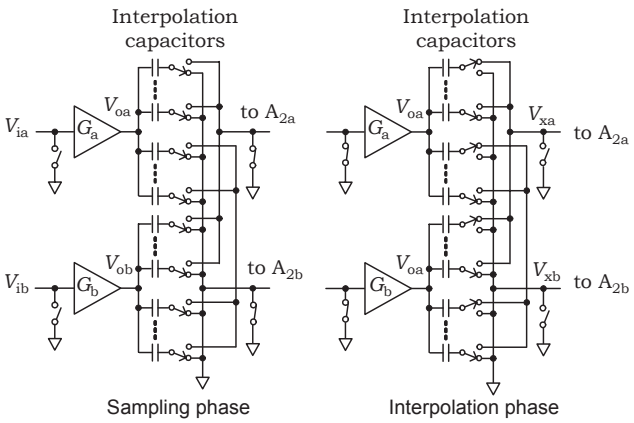

Fig. 4. Capacitor arrays for the proposed interpolation.

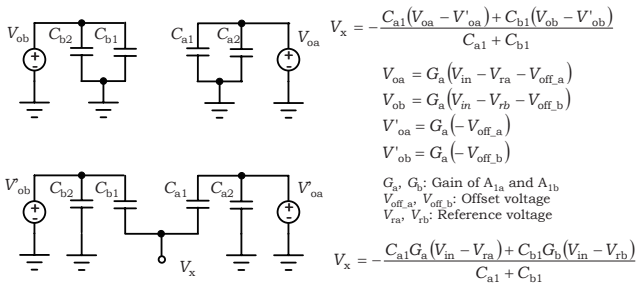

Fig. 5. Equivalent circuit for the interpolation.

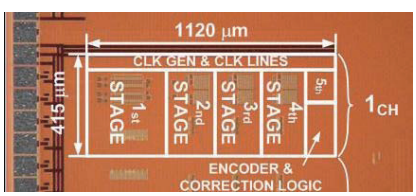

Fig. 7 Chip photograph.

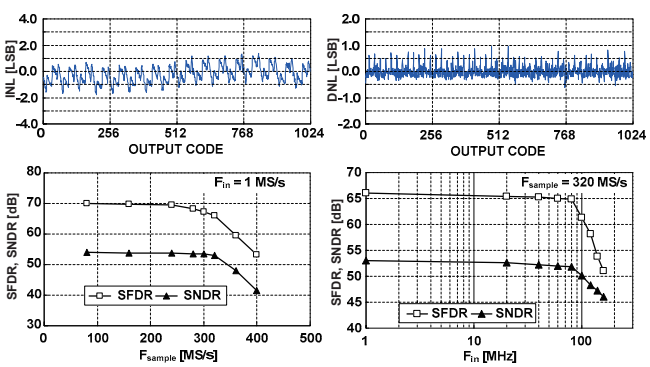

Fig. 8. Measurement results.

Table 1. Performance summary and comparison.

	This Work	[2]	[6]	[7]
Resolution (bit)	10	10	10	10
F_{sample} (MS/s)	320	500	205	320
V_{DD} (V)	1.2	1.2	1	–
Power dissipation (mW)	40	55	61	42
$ENOB_{peak}$ (bit)	8.5	8.5	8.7	8.7
FoM_{Fs}/ FoM_{ERBW} (pJ/c.-s)	0.39 / 0.78	0.31	0.65	0.36/0.44
Technology (nm)	90	90	90	90
Active Area (mm^2)	0.46	0.5	1	0.21
Amplifier type	Open	Closed	Closed	Closed
Linearity Compensation	No	Yes	No	Yes