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A 119dB Dynamic Range Charge Counting Light-to-Digital Converter for Wearable PPG/NIRS Monitoring Applications

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***Abstract*— This paper presents a low power, high dynamic range (DR), reconfigurable light-to-digital converter (LDC) for photoplethysmogram (PPG), and near-infrared spectroscopy (NIRS) sensor readouts. The proposed LDC utilizes a current integration and a charge counting operation to directly convert the photocurrent to a digital code, reducing the noise contributors in the system. This LDC consists of a latched comparator, a low-noise current reference, a counter, and a multi-function integrator, which is used in both signal amplification and charge counting based data quantization. Furthermore, a current DAC is used to further increase the DR by canceling the baseline current. The LDC together with LED drivers and auxiliary digital circuitry are implemented in a standard 0.18 µm CMOS process and characterized experimentally. The LDC and LED drivers consume a total power of 196 µW while achieving a maximum 119 dB DR. The charge counting clock, and the pulse repetition frequency of the LED driver can be reconfigured, providing a wide range of power-resolution trade-off. At a minimum power consumption of 87 µW, the LDC still achieves 95 dB DR. The LDC is also validated with on-body PPG and NIRS measurement by using a photodiode (PD) and a silicon photomultiplier (SIPM), respectively.**

***Index Terms*— Photoplethysmogram (PPG), near-infrared spectroscopy (NIRS), light-to-digital converter (LDC), dynamic range (DR), ambient light cancellation, dual-slope, charge counting, reconfigurable.**

I. Introduction

Optical sensing techniques like photoplethysmogram (PPG) and near-infrared spectroscopy (NIRS) are widespread in wearable electronics such as smartwatches, health patches, and headsets [1]-[3]. Both modalities complement the conventional electrode-based sensing techniques such as electrocardiogram (ECG) and electroencephalogram (EEG) by providing more spatial information with higher user comfort [4]. A PPG signal obtained by single green/red light can detect heart rate by measuring the blood volume changes and two-channel PPG signals obtained by red/infrared light can measure oxygen saturation (SpO_2). PPG allows long-term monitoring during daily life in a home setting and it can also be used in hospital settings, e.g. monitoring anesthesia depth during surgeries [5]-[7]. A NIRS signal is obtained with near-infrared light (700 nm-900 nm) and it can measure the hemodynamics in the brain and the microvascular blood flow of muscle based on the different absorption coefficients between hemoglobin and deoxygenated -hemoglobin in the near-infrared region. The technique finds its applications in brain mapping, brain-computer interfaces, and other medical cases like brain disorder detection [8][9]. Conceptually, for both modalities, suitable light sources, often LEDs with specific wavelengths illuminate the tissue. Light detectors, i.e. a photodiode (PD) or a silicon photomultiplier (SIPM) generates photocurrent from the diffusely reflected light [10], which is amplified and digitized by the readout circuit. It provides a measure of the change in light absorption and reveals the underlying biomedical information [11]-[13].

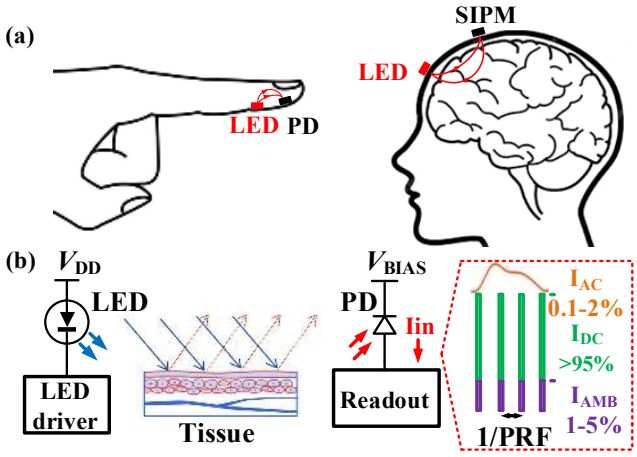

Fig. 1. (a) Reflective mode measurement on finger (PPG) and forehead (NIRS) (b) A typical PPG/NIRS sensor system

The major challenge for PPG/NIRS sensor readout is the high

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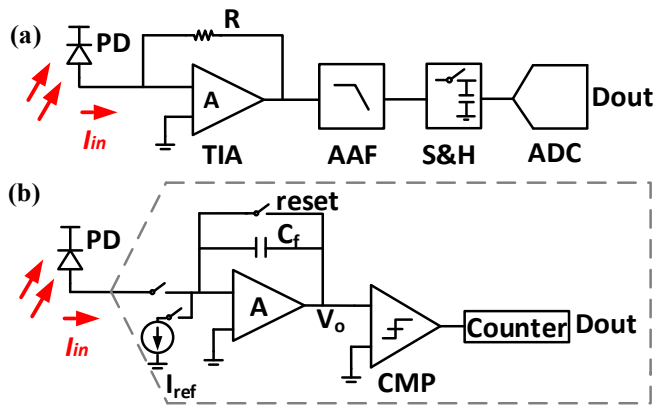

Fig. 2. (a) Conventional TIA based PPG/NIRS readout (b) Proposed LDC

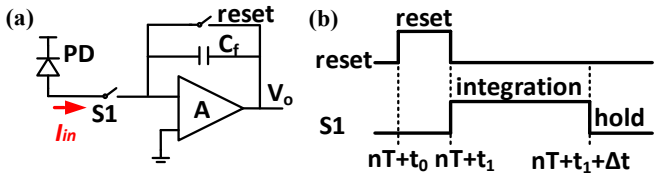

Fig. 3. (a) Simplified model for pulsed current integration (b) Timing diagram

dynamic range (DR) required by the small perfusion index (PI, AC/DC ratio) of the PPG/NIRS signal. Namely, a small AC component containing information on blood volume and oxygenation change is superposed on a large DC component from bones and muscles. The PI is around 1-5% measured on the finger and it can be as low as 0.05-0.25% on the chest. This small PI together with possible interference from ambient light and motion artifacts pose a strict DR requirement for the readout circuit. Some applications like NIRS brain mapping and cognitive study requires an even higher DR (> 100 dB) [14].

Meanwhile, wearable devices powered by small batteries have a very limited energy budget. Low power consumption is thus very important to prolong the battery lifetime and enable long-term monitoring [15]. Besides, high reconfigurability is favorable to readout signal in different measurement locations conditions. Namely, the LED current, the pulse repetition frequency (PRF), the channel gain, and the conversion resolution should be made reconfigurable according to the measurement conditions [16].

A PPG/NIRS sensor system includes the LED drivers and the readout, where a transimpedance amplifier (TIA) is typically used, as shown in Fig. 2 (a), to convert the photocurrent to a voltage [1]. An anti-aliasing filter (AAF) is then needed to limit the bandwidth to avoid noise folding, and a sample/hold circuit together with an ADC are used for data conversion [17]. The required LEDs current can be as high as 100mA, dominating the system power consumption. To reduce the power, in current domain, the LED is usually pulsed with a certain duty-cycle [18], e.g. a 1% duty-cycle with a peak current of 10 mA results in an average current of 100 µA. Moreover, an inductor-based LEDs driver is proposed, which removes the high supply voltage needed in conventional LED drivers and thus saves power in voltage domain [19]. Reducing the peak current can also reduce power consumption, resulting in undesirable small signal amplitude. Therefore, from a power minimization point of view, a low PRF and a short LED pulse should be used without compromising signal amplitude.

Readout circuit requires high bandwidth for short LED pulses and usually, the ADC sampling rate is the same as the PRF. This bandwidth is much higher than the PRF in typical cases [20]. For example, assuming a PRF of 1kHz and a 100uS pulse width is used (10% duty-cycle), the bandwidth of the TIA needs to be at least 50 kHz to achieve a 99.3% settling accuracy. As a result, the broadband TIA noise will fold back into the 500 Hz bandwidth of the ADC output. With 1% duty-cycle, the noise folding effect will be X10 (in terms of noise power) for the same settling requirement. This power-noise trade-off needs to be investigated carefully in any PPG/NIRS readout design.

Besides the readout noise, the ADC quantization noise and nonlinearities also can limit the DR. High-resolution SAR ADCs can be exploited to reduce the quantization noise [21]-[23]. However, a SAR scheme usually requires calibration and dedicated layout matching techniques to achieve good linearity [24]. Apart from reducing the noise, the DR can be enhanced by increasing the input current range with a current DAC (IDAC)[32]-[34] and correlated double sampling based ambient cancellation can also help [35][36].

Recently, LDC is becoming prevalent in biomedical optical sensor readout, where the readout frontend merges with data converters. The sigma-delta LDC proposed in [25][26] can achieve high resolution at the cost of high LEDs power because a high PRF is required for oversampling [27]. The LDC exploiting a self-integration scheme (signal current integration on the parasitic capacitance of the photodetector) together with a level-crossing ADC proposed by Kim et al. can reduce the front-end power consumption significantly [28][29]. Antonino et al. proposed a similar readout architecture using on-chip pinned-diode and an incremental ADC, which achieves an even lower power consumption[30][31]. Both solutions may suffer from a nonlinearity limited DR due to the voltage-dependent capacitance of the PD.

To solve the above-mentioned problems, a power-efficient, high DR, high reconfigurable, charge counting based LDC is proposed [37]. It employs a multi-function integrator to convert the signal current to a voltage while forming a low-pass filter to ease the noise folding effect [38]. As the key component in the proposed LDC, the same integrator also implements the sample/hold functionality during data conversion, which effectively reducing the number of noise sources. The proposed LDC works in a dual-slope, charge counting mode to realize a direct light to digital conversion in the time domain, with high linearity [39]. The low noise integrating readout scheme with the high linearity charge counting based digitization contributes to a higher DR, which is further increased by a 7-bit IDAC and an ambient light cancellation scheme. A prototype is implemented in a standard 0.18 µm CMOS technology. Measurement results show that the proposed LDC achieves a best-in-class DR of 119 dB.

The rest of the paper is organized as follows. Section II describes the system architecture and the operating principle of the proposed LDC. Section III shows the circuit implementation of the LDC. Section IV presents the noise-power analysis. The

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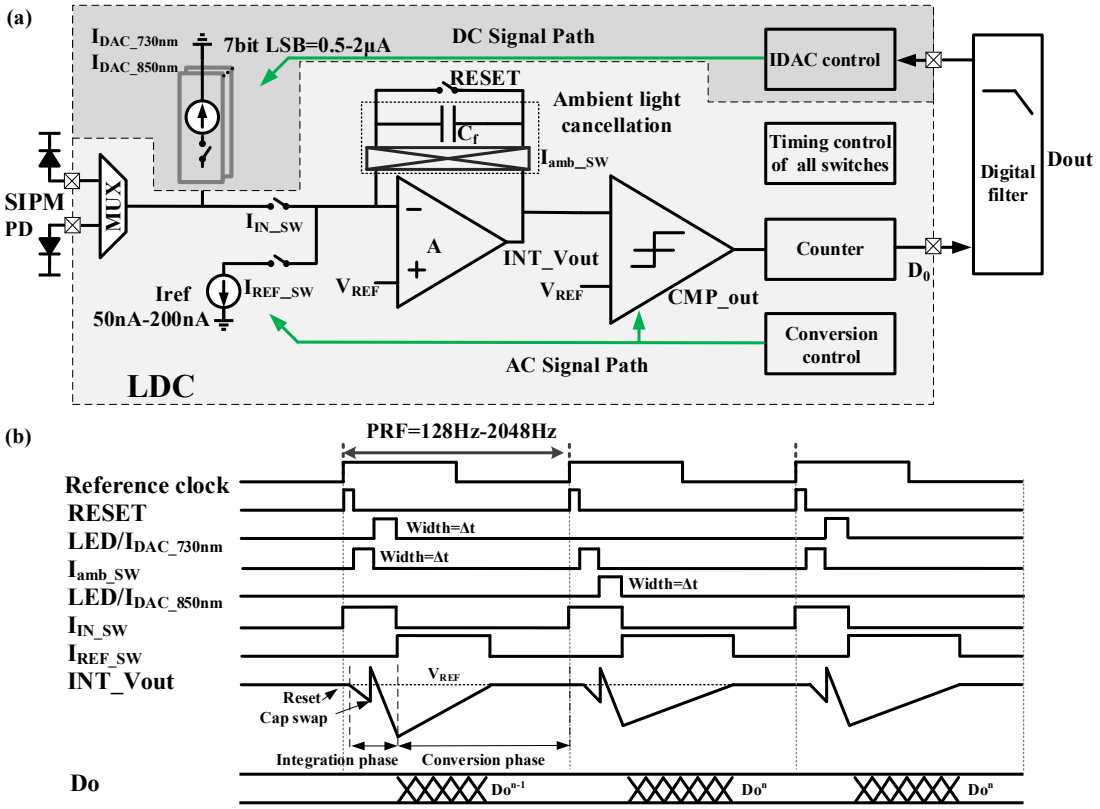

Fig. 4. (a) Block diagram and implementation details of the LDC (b) Timing diagram

measurement results are described in section V and conclusions are drawn in Section VI.

II. THE PROPOSED ARCHITECTURE

The working principles of the LDC are described in this section including the system architecture, the DC compensation /ambient light cancellation scheme, and the reconfigurability.

A. *Readout architecture*

The simplified architecture of the proposed LDC is shown in Fig. 2 (b). It consists of an integrator, a current reference, a comparator, and a counter. Different from the conventional TIA, in the proposed LDC, a duty-cycled integration is used to convert the signal current to a voltage, where the gain can be easily reconfigured by changing the integration time window, which is synchronized to the LED pulses. The operation of this duty-cycled integration is shown in Fig. 3 (a). The photocurrent is integrated on the capacitor C_f during a period Δt [40]. The transfer function of this duty-cycled integration is expressed in (1). This transfer function contains a first-order filter (-3 dB bandwidth $0.44/\Delta t$), which can ease the noise-aliasing effect without additional power and noise contribution[41].

$$Vo(f) = \frac{I_{in}}{C_f} \cdot \Delta t \cdot sinc(\pi f \Delta t) \quad (1)$$

$$Vo = \frac{\Delta t}{C_f} \cdot I_{in} \quad (2)$$

The output voltage of the integrator can be found in (2). Since the input PPG/NIRS signal has a bandwidth of < 20 Hz, which is much lower than $1/\Delta t$, it can be assumed that $sinc(\pi f \Delta t) \approx 1$. After the pulse current integration is done, the charge stored on C_f has a linear relationship with the input photocurrent. Different from the conventional solution in Fig. 2 (a), where a separate ADC is used, the proposed LDC uses a second slope (the first slope is the integration) to count the charge on C_f by discharging C_f with the reference current I_{ref} as shown in Fig. 4(a). The charge is counted by a counter that is trigged by the comparator when V_O reaches V_{ref}. Thus, V_O is converted from the voltage domain into the time domain. The total down-integration time t_{down} recorded by the comparator and counter operating at frequency f_{clock} to determine the input signal current with the counter output code D_{out}, can be expressed as follows:

$$I_{in} = I_{ref} \cdot \frac{t_{down}}{\Delta t} = I_{ref} \cdot \frac{D_{out}}{\Delta t \cdot f_{clock}} \quad (3)$$

From (3), the input current is determined by the ratio between the two time periods and the value of I_{ref}. It is worth noting that the same current sink I_{ref} is used to count the charge in each conversion and hence this circuit architecture does not require dedicated component matching to achieve high linearity. Moreover, the dual-slope operation makes the LDC immune to the integrator's offset.

The proposed LDC exploits the multi-function integrator, which implements sampling, current to voltage conversion, and filtering together. Therefore, the power consumption and noise can be reduced compared to conventional solutions where more building blocks are required. Moreover, the LDC benefits from the dual-slope charge counting mechanism for its time domain linearity and accuracy, which will be further discussed in section IV. A long counting time during the conversion phase limits the maximum PRF that can be used, this can be solved by using a higher counting clock frequency at the cost of higher

power. Moreover, in this design, the integrator cannot be duty-cycled according to the LED pulses [22], which slightly increases the system power consumption.

B. DC compensation and ambient light cancellation

The block diagram is shown in Fig. 4 (a). Both PD and SIPM are supported by the readout. For PPG measurements, the PD is used while the SIPM is used for NIRS measurements on the forehead. The sensitivity of a SIPM is higher, at the cost of a high reverse bias voltage [45]. The light current generated by a SIPM can go up to 100 μA, which is higher than a typical PD, which is typically around 10 to 30 μA. To accommodate the large DC component in the signal, the LDC has two signal paths: one for the AC-component and one for the DC-component. The DC-signal path uses 7-bit IDAC to cancel most of the DC current before it enters the integrator. The remaining AC-signal or DC residual are then amplified and quantized by the dual-slope operation as explained in section II-A. Since this cancellation is digitally controlled, the full signal can be reconstructed in the digital domain and both AC signal and DC signal can be easily classified, effectively increasing the input range of the LDC.

Ambient light is a slow-varying interference, which can degrade the DR. The ambient light is canceled by swapping the integration capacitor [15][21]. The timing diagram of the cancellation operation is shown in Fig. 4 (b). Before each LED pulse, the integration capacitor C_f of the integrator is reset. In the first integration phase, the ambient signal is firstly integrated on C_f and in the second integration phase, synchronized with LED pulse, both ambient and signal light are integrated on C_f. Making the time window of these two phases the same, the ambient light is effectively canceled and only the signal light remains.

C. Reconfigurability

The DR of the proposed LDC can be reconfigured to fit the requirement of the different photodetectors and measurement conditions.

The PRF decides the noise folding factor since it equals the sampling frequency and the noise bandwidth of the integrator is decided by the pulse width which is far beyond the PRF. A higher PRF results in a higher power consumption but also in a lower input-referred current noise and thus a higher DR. Meanwhile, the comparison clock decides the quantization noise of the proposed LDC, a higher frequency provides a smaller LSB and thus lower quantization noise. More details about the reconfigurability and power-DR trade-offs are discussed in Section IV.

III. CIRCUIT IMPLEMENTATION

The main building blocks are described in this section including the integrator, comparator, current reference, and IDAC. The control signals for these blocks are provided by the digital control circuitry.

A. Multi-function integrator

The integrator converts the photocurrent into a voltage. Its input impedance is defined as the impedance of integration capacitor C_f divided by the open loop gain of the core voltage amplifier. Thus, the open-loop gain needs to be made high so that the equivalent impedance of the integrator is much smaller than the internal impedance of the PD or SIPM to avoid signal attenuation. Since C_f has a typical value of 10 to 100pF the parasitic capacitance of the SIPM is around 1nF, the open loop gain of the amplifier is designed > 80 dB to ensure enough gain accuracy. This is not an issue with typical PD due to their smaller internal capacitance.

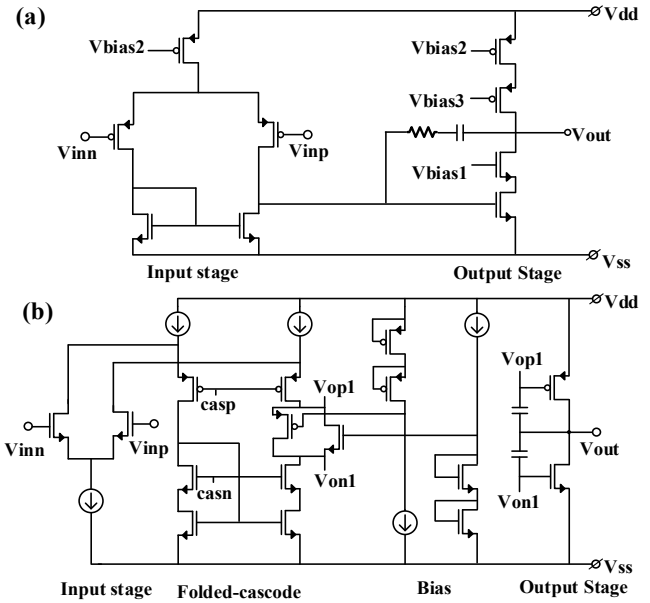

Fig. 5. (a) Conventional amplifier with PMOS input and class-A output stage. (b) Proposed core amplifier in the multi-function integrator with NMOS input stage and class-AB output stage.

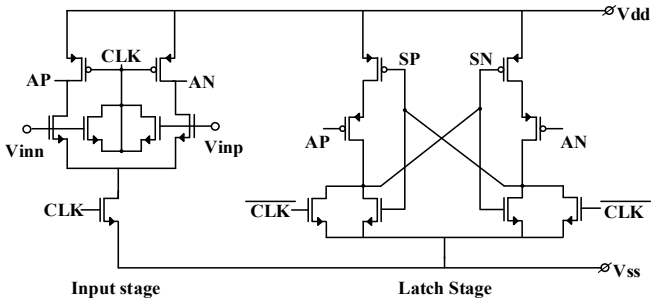

Fig. 6. Dynamic comparator with NMOS input stage

A two-stage OTA is used as the core amplifier. Compared with the conventional miller-compensated two-stage amplifier shown in Fig.5 (a), the folded-cascode input stage of the proposed OTA can provide a higher DC-gain, as shown in Fig. 5 (b) [44], which is desirable for low input impedance. Besides, a push-pull class-AB output stage [45] is used to provide a large output sink/source current, providing good compatibility for both common PDs and SiPMs. This class-AB output stage can provide higher current with a lower quiescent bias than both the classic class-A output stage in miller-compensated amplifiers [15][42][43] and the source follower based output stage [26]. The bandwidth of the amplifier is designed to be 3 MHz to allow short pulses, which reduces the LED power. The input transistors are biased in the weak-inversion region to obtain low-noise operation together with low power consumption. The integrator consumes 50 μA current at a 1.2 V supply voltage.

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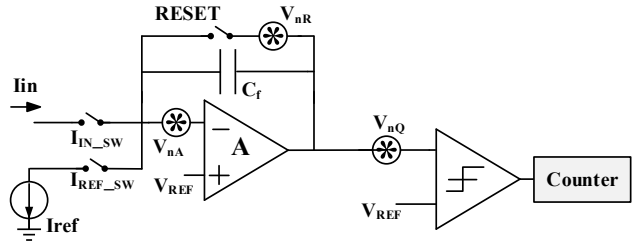

Fig. 7. Noise modeling of the LDC including the reset noise, the amplifier noise and the quantization noise

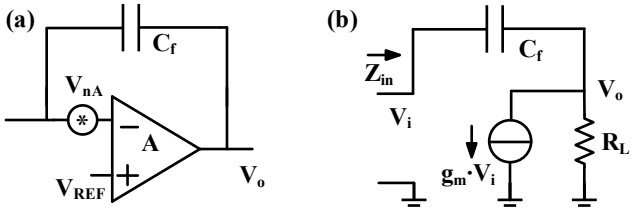

Fig. 8. (a) Simplified noise model of the integrator (b)Input impedance of the core amplifier

B. Comparator

The output of the integrator is monitored by a dynamic comparator during down integration. In contrast to the integrator's offset, the offset of the comparator can result in a constant error and converted to the digital domain as a DC component. However, compared with the large DC current, this influence of the comparator's offset is negligible. Moreover, the integration capacitor is much larger than the parasitic capacitance of the comparator's input pairs, making the kick-back effect of the dynamic comparator minor in this single-ended architecture.

As shown in Fig. 6, a two-stage latch comparator is used [46]. The NMOS input pair is biased in weak inversion region to obtain a good power efficiency. Moreover, the same common-mode voltage is applied for the amplifier to provide a large output swing while maintaining efficiency. A dummy input pair with an opposite clock is designed to further suppress the kick-back effect by compensating the charge. The noise of the comparator is around 50 μV_{rms}, mainly originating from the input pair. This is not a dominant noise source in LDC. The propagation delay is 1 ns which allows a maximum comparison frequency of more than 50 MHz [46][47].

The current consumption of the comparator is proportional to the comparison clock frequency. The comparator is synchronized with the counter and stops when the output of the integrator reaches the reference voltage V_{ref}.

C. Current reference and IDAC

The current reference is used to discharge capacitor C_f during the down-integration period. The noise of the current reference needs to be minimized. The reference current for the IDAC is generated from an on-chip bandgap reference, filtered with an external capacitor (10 μF) to reduce the noise. The I_{ref} branches are implemented by current mirrors with source degeneration resistors to further reduce the noise [48]. The output current for I_{ref} is between 50 nA to 200 nA. The 7-bit IDAC has a similar architecture but a higher reference current from the bandgap. A total of 128 units (7-bit) are implemented to have a maximum output current of 200 μA, sufficiently large to cancel the DC-component even for SIPMs.

IV. Noise and power optimization

The shot noise of the PD should be taken into consideration before the noise analysis of the LDC. However, a 100 μA light current of the PD only results in a 5.7 pArms/$\sqrt{Hz}$ shot noise floor. Considering the low bandwidth of the PPG/NIRS signal, shot noise is negligible. As mentioned in Section II.C, the total noise of the LDC consists of two components (Fig. 7): the integrator noise and the quantization errors, both of which are thoroughly analyzed in this section. Moreover, a noise power optimization strategy is discussed together with the wide range of reconfigurability.

A. Integrator noise

The integrator noise consists of the kT/C noise of the reset switch and the integration noise from the core amplifier. Before each sampling period, the reset switch resets the integration capacitor in a short time, generating noise as shown in (4), where k is the Boltzmann's constant, and T is the absolute temperature. A simplified model of the integrator is shown in Fig. 8 to derive the noise of the core amplifier during the integration. Assuming the noise of the input pair in the amplifier is dominant, the input voltage noise of the integrator can be expressed by (5), where g_m is the transconductance of the input pair of the core amplifier and f_k is the corner frequency of the flicker noise.

$$V_{nR}^2 = \frac{kT}{C_f} \tag{4}$$

$$V_{nA}^2 = \frac{4kT}{g_m} \cdot \left(1 + \frac{f_k}{f}\right) \tag{5}$$

The thermal noise from the reset switch is negligible when typical values for C_f (~100 pF) and g_m (~1 mS) are used. Combining with (1), the output noise of the integrator is expressed by (6). where t_{tot} is the total integration time including both integration periods ($t_{down} \gg \Delta t$). The output voltage noise power is shown in (7). The first term in (7) is the total white noise power, which usually dominates over the second term, the flicker noise power, because of the low corner frequency compared with the amplifier's bandwidth [49]. As a result, the final value of (7) represents the white noise power of the LDC.

$$V_{nO}^2 = 4kTg_m \cdot \left(1 + \frac{f_k}{f}\right) \frac{1}{{C_f}^2} \int_0^\infty {t_{tot}}^2 \cdot sinc(\pi f t_{tot})^2 df \tag{6}$$

$$V_{nO}^2 \cong 4kTg_m \frac{{t_{tot}}^2}{{C_f}^2} \cdot \left(\frac{1}{2t_{tot}} + f_k \cdot \ln(f_k)\right) \cong \frac{2kT}{C_f} \cdot \frac{g_m}{C_f} \cdot t_{tot} \tag{7}$$

Now, there is a relationship between the maximum total integration time t_{tot} and the given PRF, namely the conversion period needs to be finished within one sample period. Assuming a full-swing signal needs to be converted with the maximum total integration time, the PRF can be calculated to be $1/t_{tot}$. Meanwhile, g_m/C_f defines the unity gain frequency of the core amplifier. Therefore, (7) can be rewritten as follows:

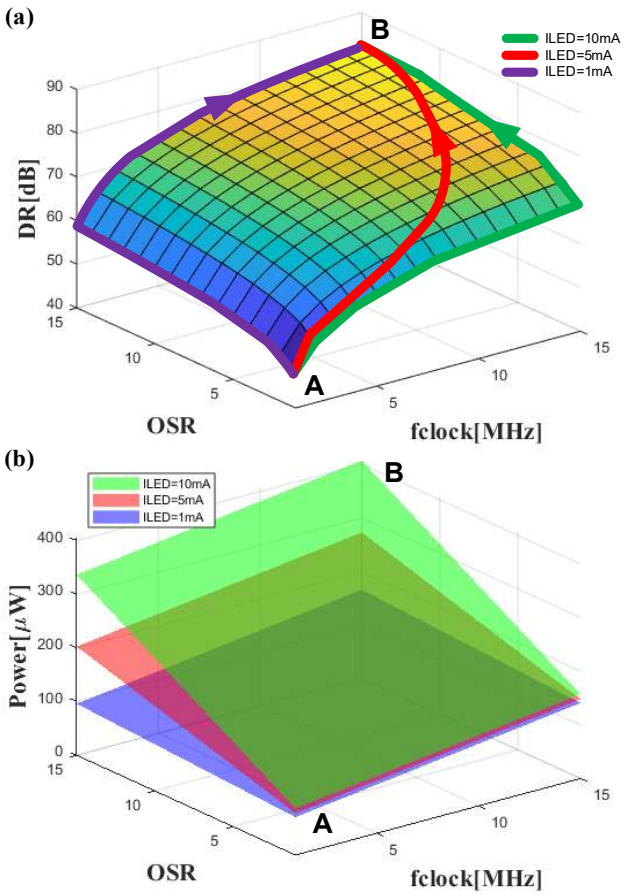

Fig. 9. (a) The trade-off between OSR, f_{clock} to achieve the same DR (AC signal path) by the minimum power (b) The total power consumption at different LED current

$$V_{nO}^2=\frac{kT}{C_f}\cdot\left(\frac{4\pi f_0}{PRF}\right) \quad (8)$$

where f_0 is the unity gain bandwidth of the core voltage amplifier. From this equation, all the broadband noise from the amplifier is folded back to PRF/2. In this case, the noise folding effect can be severe because f_0 is much higher than the sampling frequency. A higher PRF can help ease the noise folding effect, but still limited by the LED power and the conversion time. To investigate the noise folding ratio, (9) can be rewritten as follows:

$$V_{nO}^2=\frac{kT}{Cf}\cdot\left(\frac{4\pi n}{D}\right) \quad (9)$$

where n (n > 3) is the number of time constants needed for settling purposes and D is the duty-cycle. A larger D can reduce the output noise from the integrator at the cost of more LED power, because the LED needs to be enabled for a longer time.

B. *Quantization noise*

The PRF defines the sampling rate of the LDC, which is oversampled because the bandwidth of the input light signal is low. The oversampling ratio (OSR) can be written as OSR=PRF/2f_{in}. The quantization error of the LDC depends on the resolution of the LDC. The LSB of the LDC is the integrator output's voltage drop within one counting step. The total quantization error is:

$$V_{nQ}^2=\left(\frac{I_{ref}}{C_f\cdot f_{clock}}\right)^2\frac{1}{12} \quad (10)$$

where f_{clock} is the comparison clock frequency. From (10), the quantization noise of the LDC can be reduced while increasing f_{clock} and the PRF at the cost of both a higher comparator power consumption and LED power consumption. Finally, after filtering to the signal bandwidth, the total in-band noise of the LDC is:

$$V_{nO}^2=\left(\frac{I_{ref}}{C_f\cdot f_{clock}}\right)^2\frac{1}{12\cdot OSR}+\frac{kT}{C_f}\cdot\left(\frac{2\pi f_0}{OSR^2\cdot f_{in}}\right) \quad (11)$$

Additionally, the timing jitter results in noise as well especially during the up integration. The biggest random timing jitter during one clock cycle is:

$$V_{nT}^2=\frac{\delta t}{C_f}\cdot I_{in} \quad (12)$$

Since the integration time Δt >> δt, the random timing jitter is averaged and can be neglected at the output.

C. *Noise-power optimization with reconfigurability*

The power consumption of the AC-path can be optimized for certain DR requirements, namely the PRF and the comparison clock frequency which allows the minimal power can be determined. On the one hand, the achieved AC-path DR can be expressed by (13) (where V_O is the maximum output voltage and K_1, K_2 are constants), showing that a higher OSR and higher f_{clock} can give a high AC-path DR. On the other hand, the power consumption also increases with a higher value of OSR (the LED power) and the f_{clock} (comparator and counter power), as expressed in (14).

$$DR=10\log_{10}\frac{{V_O}^2\cdot OSR}{\left(\frac{K_1}{f_{clock}}\right)^2+\left(\frac{K_2}{OSR}\right)} \quad (13)$$

$$Power=P_{LED}\cdot OSR+P_{Com}\cdot f_{clock}+P_{Amp} \quad (14)$$

It is worth noting that, different LED currents are needed to achieve full input signal range for sensors with different measurements (sensor locations, the distance between LED and PD, or the skin tones). Thus, the LED current level has an important impact on the following optimization.

The relationship between the AC-path DR, OSR and f_{clock} is shown in Fig. 9 (a), assuming the full input range is used in the AC signal path by tuning the LED current. Moreover, the relationship between the total power consumption, OSR and f_{clock} is shown in Fig. 9 (b). The three surfaces show the total power in case of a peak current of 1mA, 5mA and 10mA at a duty-cycle of 1%. Obviously, at higher LED current, the total power increases faster with OSR than with f_{clock}.

Observing point A in both Fig. 9 (a) and (b), where a low AC-path DR is achieved with the minimum power consumption, if a high AC-path DR is required, different setting strategies are needed at different LED peak current levels. At high LED peak current, e.g. 10 mA, the optimal points can be obtained by firstly increase the f_{clock} till the folded integrator noise is dominating, and then increase OSR, as shown by the green arrow in Fig.9 (a), because increasing OSR consumes more power than increasing f_{clock}. On the contrary, at low LED peak current e.g. 1mA, the OSR should be increased before increasing f_{clock} as shown by the blue arrow in Fig. 9 (a), because in this case increasing OSR consumes less power. For

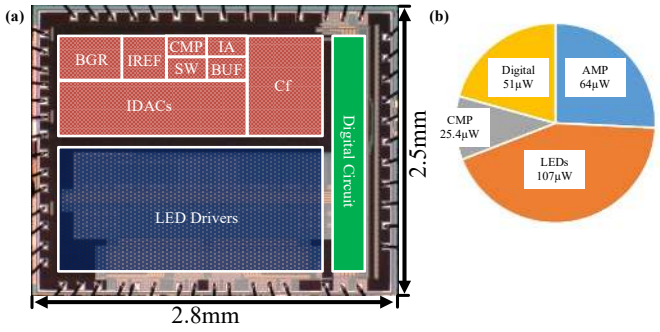

Fig. 10. (a) Micro-diagram of the LDC (b) Power distribution of the chip

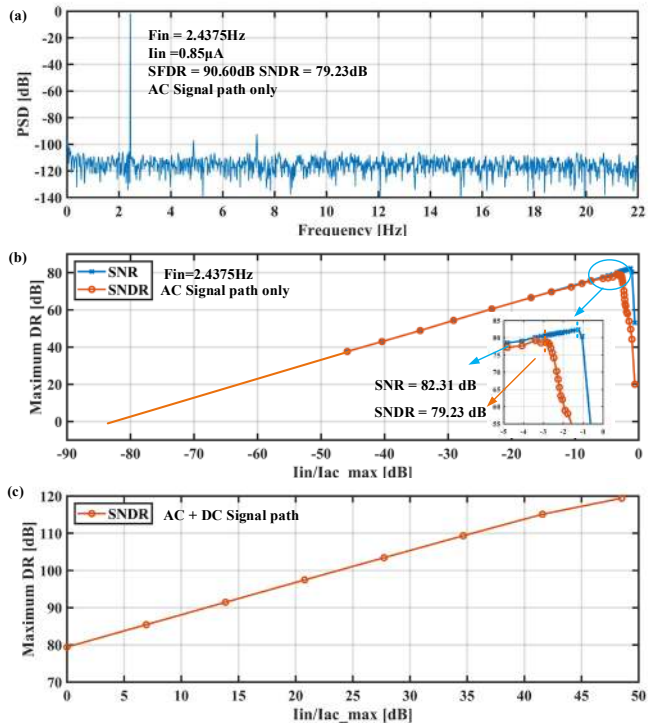

Fig. 11. (a) PSD of the AC signal path within the signal band (b) SNR, SNDR of the AC signal path with different input current range (c) Maximum DR when both AC/DC signal path enabled

a medium current (5 mA), the OSR and f_{clock} can be increased together to obtain the optimal operation point as shown by the red arrow in Fig.9 (a). The highest DR can be achieved at point B, where both OSR and the f_{clock} are high. Combined with DC-path, the maximum DR-power optimization procedure is verified by the measurement results in the next section.

V. Implementation Results

Fig. 10 (a) shows the micrograph of the prototype, which was implemented in a 0.18 µm standard CMOS technology [37]. The total area of which is 7 mm^2 and more than half of the area is taken by the LED drivers, which can carry current levels up to 100mA supplied by a constant voltage. A large area is needed for heat dissipation and to comply with electro-migration rules. For both electrical and in-vivo validation, off-chip commercial detectors (both PD & SIPM) and LEDs have been used. The readout IC operates from a supply voltage of 1.2 V. Fig. 10 (c) shows the power distribution of the chip for a 5 mA LED levels with 512 Hz total PRF and 20 µS pulse width.

The spectrum of the AC-path is measured by injecting a sinewave current into the LDC. Fig. 11 (a) shows the spectral response of the AC-path for a 2.4375Hz input sinewave current within the BW of interest (20 Hz). Within the BW of interest, an SFDR of 90.6 dB an SNDR of 79.23 dB are obtained, equivalent to an ENOB of 12.9 bit for the AC-path. Fig. 11 (b) shows the AC-path DR & SNR as a function of the input current amplitude. The highest DR and SNR are derived by sweeping the input current amplitude. As can be seen in Fig. 11 (b), the highest SNDR for the AC-path is 79.23 dB and the highest SNR is 82.31 dB. Enabling the DC-path fully and recombining the AC & DC digital outputs increases the maximum (effective) DR to 119 dB as seen in Fig. 11(c) [37].

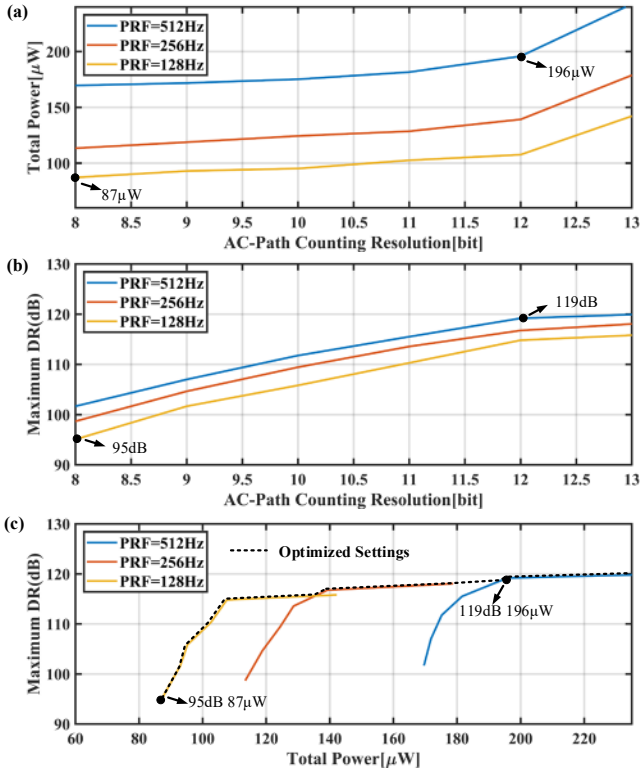

Fig. 12. (a) Power of the LDC over different AC-path counting resolution (b) Max DR (AC+DC) of the LDC over different AC-path counting resolution (c) Max DR (AC+DC) of the LED vs total power of the LDC

As discussed in section IV, a large range of reconfigurability can be achieved with the proposed LDC. Since the counting step depends on the comparison clock frequency and the reference current, the AC-path counting resolution of the LDC can be easily modified. Also, the PRF can be easily modified as explained before has a major impact on the LED power, and the maximum DR. Fig. 12 (a) shows the trade-off between the sensor's power and the AC-path counting resolution over different PRF. Fig. 12 (b) shows the relationship of how the AC-path counting resolution and PRF influence the maximum DR, assuming the DC-path is fully enabled. By combining these 2 curves, Fig. 12 (c) shows the trade-off between total system power and the final achieved maximum DR for the whole sensor. One can easily derive the pareto-optimal conditions for the lowest power consumption for any given DR from this curve. If < 115 dB of maximum DR is required for the application, it's more power-efficient to increase the maximum DR by changing the LDC's AC-path counting resolution, in

TABLE I PERFORMANCE COMPARISON

	[21]	[22]	[33]	[32]	[30]	[28]	[26]	This Work
Technology	0.13µm	0.13µm	0.18µm	65nm	0.18µm	0.18µm	0.18µm	0.18µm
VDD	1.2/3.3	1.5/2.7	1.2/3.3	1.2/3.3	1.8/3.3	--	1/2.5	1.2/3.3
Max input	63µA	--	--	10nA	--	--	51.2µA	200µA
Amb.Remove	Yes	6µA	40µA	Yes	--	--	28.2µA	50µA
DC.Substract	7.6-bit	6-bit	7-bit	--	--	--	8-bit	7-bit
Gain	19k-90M	--	1k-100k	56M-560G	--	--	--	5k-4M
PRF	600Hz	30-670Hz	2-512Hz	20-80Hz	40Hz	160kHz	100Hz	512Hz[c]
Max DR	112dB	95dB	87dB	60dB	--	--	92.7dB	119dB
LED Current @Duty Cycle	50mA @1.7%	12mA @1%	75 µA	0-17.2 mA	Sub-mA[a] @0.07%	--	7.6mA[b] @10.24%	5mA @1%
LED power	5.5mW*	0.32mW[d]	0.15mW	--	1.97µW	--	1.95mW	107µW
AFE Power	370µW**	69 µW	132µW	--	2.63µW	13-25µW	8.1µW	89µW
Area	2.5mm^2	--	16mm^2 [e]	16mm^2 [e]	20mm^2	1.8mm^2	4.9mm^2	7 mm^2 [f]
Architecture	TIA+ADC	TIA+ADC	TIA+ADC	TIA+ADC	TIA+ADC	LDC (1bΔΣ)	LDC (1bI-ΔΣ)	LDC (Slope)

* Two LED power ** Including digital power [a] Green LED=12.04µW Red LED=1.97µW [b] For recorded PPG signal [c] From 2Hz~2048Hz
[d] For a 2.7V supply [e] Including other readout channels [f] External cap for filtering reference current

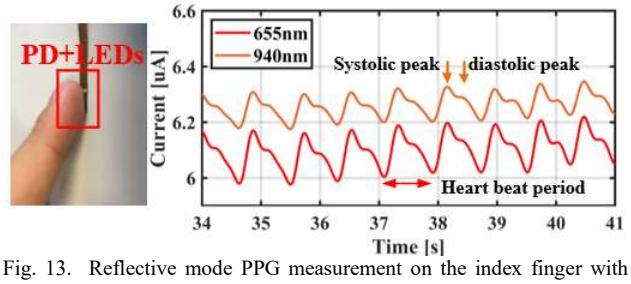

Fig. 13. Reflective mode PPG measurement on the index finger with PD. LEDs generates 665nm, 940nm wavelengths lights.

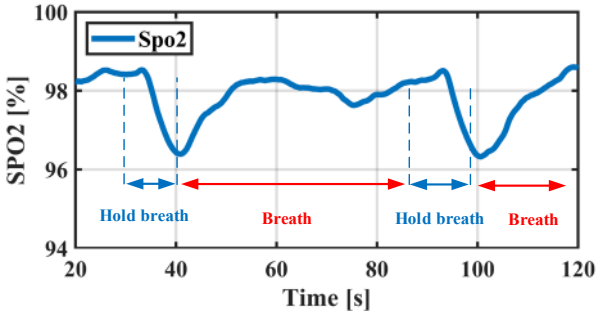

Fig. 14. SpO_2 measurement on the finger during two holding breath periods

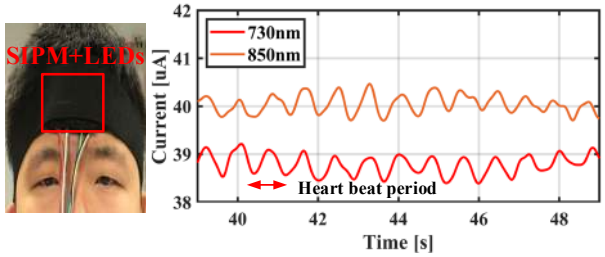

Fig. 15. NIRS measurement on the forehead with SIPM. LEDs generates 730nm, 850nm wavelengths lights.

other words, the comparison clock. However, for > 115 dB of maximum DR, it is better to choose the higher PRF, where the dominant noise source is the thermal noise of the integrator. Further decreasing the quantization noise won't improve the maximum DR but consumes more power. The maximum DR can vary from 95 dB to 119 dB while consuming a power between 87 µW to 196 µW including AFE and LEDs.

Dual-wavelength recording is used to measure the PPG response on the index finger of a male subject. The LEDs were biased with a 5mA peak current with 1% duty-cycle. The red LED is connected to a 2.6 V external supply and the infrared LED is connected to a 1.7 V external supply respectively for better power efficiency. Fig. 13 shows the output of the dual-wavelength sensor, clearly showing two PPG waveforms. Recorded by the PD, the typical range for a PPG signal is a few µA. Each cycle of the PPG wave represents a heartbeat, which is roughly one beat per second. The systolic and diastolic peak can be distinguished and the distance between these two peaks can be used as an indicator for the aging of the heart [50]. Fig. 14 shows the calculated SpO_2 (blood oxygenation) during a controlled breathing exercise from the two-stream PPG waves. A clear drop in SpO_2 can be observed when the subject holds his breath. Two breath-holding experiments have been done to verify the SpO_2 measurement [51]. Again, two LEDs with different wavelengths have been used for NIRS recording on the forehead. Instead of a PD, an SIPM detector is used for higher sensitivity since the NIR light needs to penetrate deeper to reach the brain and the reflected light is therefore weaker. The LED current is biased at 5 mA and the duty-cycle is 1%. Both ambient light cancellation and DC-path are enabled in this experiment. Fig. 15 shows a clear heartbeat signal in both wavelengths as expected, though the shape is different from regular PPG due to the brain oxygenation information contained within.

Table I summarizes the performance of proposed LDC and compares it with recently published PPG and NIRS readout circuits. The LDC achieves a maximum DR of 119 dB, which is more than two times (7 dB) higher than the state-of-the-art.

Meanwhile, the lowest power consumption (87 µW) including the readout and two LEDs is reported, while still providing a maximum DR of 95 dB. The maximum input range is 200 µA when the IDAC is active, enabling recording with SIPM. Finally, this LDC also provides a wide range of reconfigurability to suit different measurement scenarios.

VI. Conclusion

This paper presents a sub-mW LDC sensor for PPG and NIRS applications. Compared with the traditional TIA-based readout architecture. The proposed LDC exploits a multi-function integrator to reduces system complexity, achieving excellent DR and noise performance with the time domain charge counting operation. Compared to the prior art, the LDC achieves the highest maximum DR of 119dB and the lowest power consumption with a large range of reconfigurability. The LDC has been validated with on-body PPG and NIRS measurement by using a photodiode (PD) and a silicon photomultiplier (SIPM), respectively. It is now being integrated into a multiple modalities bio-signal recording and processing platform where the heart rate and SpO_2 can be extracted on-chip in real-time.

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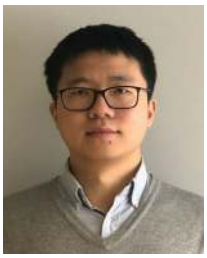

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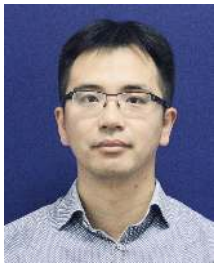

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