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# A 12.4–32 GHz CMOS Down-Conversion Mixer for 28 GHz 5G New Radio (NR)

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**Featured Application: 28 GHz 5G communication receiver; 24 GHz radar system; 19 GHz low-Earth-orbit (LEO) satellite communication (SatCom) receiver.**

**Abstract:** We report a low voltage ($V_{DD}$) and power ($P_{DC}$) 12.4–32 GHz CMOS down-conversion mixer with high conversion gain (CG) for 28 GHz 5G communications. A quarter-wavelength ($\lambda/4$) transmission line (TL) and a coupling capacitor ($C_c$), named the $\lambda/4$-TL-C-based coupler, is proposed. This is the way to attain low-$V_{DD}$, independent RF transconductance (gm)-stage bias, harmonic suppression, and near perfect coupling from the RF gm stage to the LO switch transistors. The body-self-forward-bias (BSFB) technique, i.e., connection of the gm-stage transistors' body to drain via a large body resistance, is used for threshold voltage ($V_{th}$) and $V_{DD}$ reduction and substrate leakage suppression. CG and noise figure (NF) enhancement at the same or even a lower $P_{DC}$ is achieved because lower $V_{DD}$ and higher gm (due to larger bias current) are used. To facilitate the RF measurement, a compact Wilkinson-power-divider-based balun with small-phase deviation and amplitude imbalance is included at RF and LO inputs. The mixer consumes 6.5 mW and achieves a CG of 14.4 ± 1.5 dB for 12.4–32 GHz (i.e., 3 dB bandwidth ($f_{3dB}$) of 19.6 GHz), a lowest noise figure ($NF_{min}$) of 7 dB, and figure-of-merit (FOM) of 0.023, which is one of the best results ever reported for millimeter-wave (mm-wave) down-conversion mixers with an $f_{3dB}$ larger than 10 GHz and $P_{DC}$ lower than 10 mW.

**Keywords:** CMOS; low voltage; low power; transmission line; coupler; down-conversion mixer



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## 1. Introduction

In a phased-array transceiver for 28 GHz 5G new radio (NR), the down-conversion mixer is a crucial component in each digital channel for conversion of the receiving RF signals to intermediate-frequency (IF) or baseband (BB) signals [1–10]. The basic requirements of a down-conversion mixer include a small chip area, low supply voltage ($V_{DD}$) and power ($P_{DC}$), and decent input impedance ($Z_{in}$) matching, conversion gain (CG), 3 dB CG bandwidth ($f_{3dB}$), noise figure (NF), LO–RF isolation, and power linearity (such as an input 1 dB compression point ($P_{1dB}$) and third-order intercept point (IIP3)). Recently, several millimeter-wave (mm-wave) down-conversion mixers have been reported [1–8]. For instance, in [2], a wideband (24–40 GHz) down-conversion mixer employing body-effect control for CG enhancement in 65 nm CMOS was demonstrated. However, a $P_{DC}$ of 10.3 mW and LO input power ($LO_{in}$) of 5 dBm leaves room for improvement. In [3], a 23–25 GHz folded down-conversion mixer using cross-coupled PMOS transistors (CCPTs) for CG boosting in 0.13 µm CMOS is reported. However, a $P_{DC}$ of 16.8 mW and $f_{3dB}$ of 2 GHz are not satisfactory. In [8], a 88–100 GHz down-conversion mixer using the parallel of CCPT and series-RL as the core IF load (i.e., CCPT-RL-based core IF load) for CG and IF-bandwidth enhancement in 90 nm CMOS is reported. Yet, a $V_{DD}$ of 1.2 V (due to the cascode of three transistors) still has room for improvement. To demonstrate that low $V_{DD}$ and $P_{DC}$, wideband, and decent CG and NF can be achieved for a down-conversion mixer

for 28 GHz 5G NR, we report a 6.5 mW 12.4–32 GHz down-conversion mixer with a CG of 14.4 ± 1.5 dB and NF of 7–9.7 dB in 90 nm CMOS using the body-self-forward-bias (BSFB) technique, the CCPT-RL-based core IF load, and λ/4-TL-C-based coupler (constituting a λ/4 transmission line (TL) and a coupling capacitor ($C_c$)). In this paper, mixer circuit design is introduced in Section 2, the measurement results of the mixer and comparisons with previous work is discussed in Section 3, and a conclusion is presented in Section 4.

## 2. Circuit Design

Figure 1a shows the illustrative diagram of the proposed low-$V_{DD}$ and low-$P_{DC}$ down-conversion mixer. In theory, the $Z_{in}$ of a grounded lossless λ/4-TL (denoted $TL_{qw}$) is infinite at the operation frequency of $f_0$ (=$\omega_0/2\pi$) and the odd-harmonic frequencies ($3f_0$, $5f_0$, etc.) and is zero at DC and the even-harmonic frequencies ($2f_0$, $4f_0$, etc.). Instead of the transformer coupling approach [7], two λ/4-TL-C-based couplers are used to achieve near perfect coupling from the RF transconductance (gm) stage to the LO switch transistors. The λ/4-TL-C-based coupler has the merits of a straightforward design and layout, as well as harmonic suppression. The low $V_{DD}$ and optimized noise, gain, and linearity design of the mixer become possible due to the separate DC bias of the RF gm stage and the LO-transistors/IF loads. In brief, the bias currents of transistors $M_3/M_4$ and $M_5/M_6$ flow to the ground through $TL_{qw}$ instead of the RF gm stage or transformer secondary coil. The outputs of the RF gm stage transmit to $M_3/M_4$ and $M_5/M_6$ near perfect through the λ/4-TL-C-based couplers instead of direct transmit or the transformer coupling. This is the way to achieve low $V_{DD}$ and optimized design. Moreover, CCPT-RL-based core IF load is used for load-impedance ($Z_L$)/CG enhancement while keeping a low $P_D$ and wide IF bandwidth. The BSFB technique, i.e., connection of the gm-stage transistors' body to their drain via a large body resistance $R_B$ (13.1 kΩ in this work) is used for threshold voltage ($V_{th}$) and $V_{DD}$ reduction, in addition to substrate leakage suppression. CG and NF enhancement at the same or even a lower $P_D$ is achieved because of the lower $V_{DD}$ and higher gm due to larger overdrive voltage ($V_{ov}$) or bias current [11].

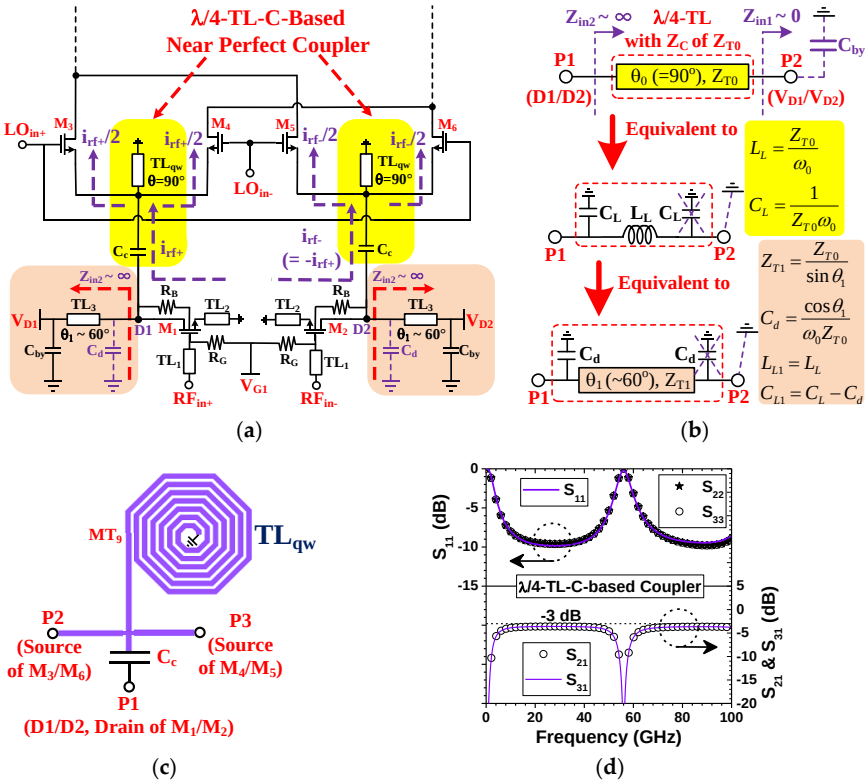



**Figure 1.** Illustrative diagrams of (**a**) a mixer using a λ/4-TL-C-based coupler, and (**b**) the current-source load. (**c**) Layout and (**d**) simulated results of the coupler.

Figure 1b shows the current-source-load design of the gm stage. A lossless $TL_{qw}$ with an electrical length ($\theta$) of 90° and characteristic impedance ($Z_C$) of $Z_{T0}$, such as the one in Figure 1c (with $Z_{T0}$ of 89.7 Ω), can be modeled by an inductance ($L_L$) and two parallel end-capacitance ($C_L$) as follows [12].

$$L_L = \frac{Z_{T0}}{\omega_0} \tag{1}$$

$$C_L = \frac{1}{Z_{T0}\omega_0} \tag{2}$$

On the condition that $Z_{in1}$ is equal to zero, $Z_{in2}$ is infinite at $\omega_0$ since the parallel of $L_L$ and $C_L$ exhibits an infinite impedance at $\omega_0$ from Equations (1) and (2). In the design of the current-source load of the gm stage, the parasitic capacitance ($C_d$) at drain nodes D1/D2 of $M_1/M_2$ should be considered. In theory, a $TL_{qw}$ with $Z_C$ of $Z_{T0}$ is equivalent to a TL (with smaller $\theta$ (of $\theta_1$), larger $Z_C$ (of $Z_{T1}$), and the same inductance ($L_{L1} = L_L$)) and two extra parallel end-capacitance $C_d$ values (=$C_L - C_{L1}$). One of the required $C_d$ values is provided by the parasitic $C_d$ and the other has no effect (due to in parallel with a short-circuit). $Z_{T1}$ and $C_d$ are given by

$$Z_{T1} = \frac{Z_{T0}}{\sin\theta_1} \tag{3}$$

$$C_d = \frac{\cos\theta_1}{Z_{T0}\omega_0} \tag{4}$$

Suppose $Z_{T0}$ is 65 Ω, then $L_L$ is 369.6 pH and $C_L$ is 87.4 fF at $f_0$ of 28 GHz according to Equations (1) and (2). From Equations (3) and (4), $\theta_1$ is 60° and $Z_{T1}$ is 75.1 Ω due to a $C_d$ equal to 43.7 fF in this work.

Figure 1c shows the simplified layout of the λ/4-TL-C-based coupler in Figure 1a. A compact spiral $TL_{qw}$ (with size of 73.6 × 76.1 μm$^2$ and metal width/space of 3/2 μm) and a $C_c$ (with size of 32 × 36 μm$^2$ and equivalent capacitance of 1.76 pF) are used. Figure 1d shows the simulated reflection coefficients ($S_{11}$, $S_{22}$, and $S_{33}$) and gain ($S_{21}$ and $S_{31}$) of the coupler. The coupler achieves decent $S_{21}$ and $S_{31}$ of −3.595 dB at 28 GHz and $S_{21}$ and $S_{31}$ better than −4 dB for 8.7–46.9 GHz. At 56 GHz, decent second-harmonic suppression ($S_{11}$ of −0.22 dB, $S_{22}$ and $S_{33}$ of 0 dB, and $S_{21}$ and $S_{31}$ of −89 dB) is achieved.

Figure 2a,b show the circuit diagram and chip of the down-conversion mixer with the important component parameters labeled. The chip area is 0.879 × 0.562 mm$^2$, i.e., 0.494 mm$^2$. The mixer comprises a double-balanced Gilbert-cell-based mixer core (with a differential RF gm stage using the BSFB technique, two λ/4-TL-C-based couplers, and a CCPT-RL-based core IF load), two Wilkinson-power-divider-based baluns, and differential output buffer amplifiers. The mixer was designed and implemented in 90 nm CMOS. This process offers nine metal layers, named $MT_1$ to $MT_9$ from bottom to top. The interconnection lines, as well as the TL inductors, were implemented with the 3.4 μm-thick upmost metal ($MT_9$) to minimize the resistive loss. The Momentum three-dimensional (3D)-planar EM simulator in ADS (Advanced Design System) is used for EM-circuit cosimulation. Substrate and layer parameters of ADS Momentum are set up according to the process information provided by the foundry. This ensures the post-layout simulation results of the mixer close to the measurement ones. Instead of the transformer coupling approach (with a pair of λ/4 TLs for harmonic suppression) [7], a straightforward λ/4-TL-C-based coupler introduced in Figure 1 is used between the RF gm stage and the LO switch transistors. The BSFB technique, also shown in Figure 1, is used in the RF gm stage for $V_{th}$ and $V_{DD}$ reduction, as well as substrate leakage suppression. CG and NF enhancement at the same or even lower $P_D$ is achieved because lower $V_{DD}$ and higher gm (due to larger bias current) are used. To enhance $Z_L$/CG and keep a low $P_D$ and decent IF bandwidth, a CCPT-RL-based core IF load is used. At $V_{DD}$ = 0.8 V and $V_{D1} = V_{D2} = V_{G1} = V_{G2}$ = 0.4 V, the mixer dissipates 6.4 mW. Compared with the traditional mixer for the direct-conversion receiver, the mixer consumes low $P_D$ and achieves significant CG and NF enhancement.

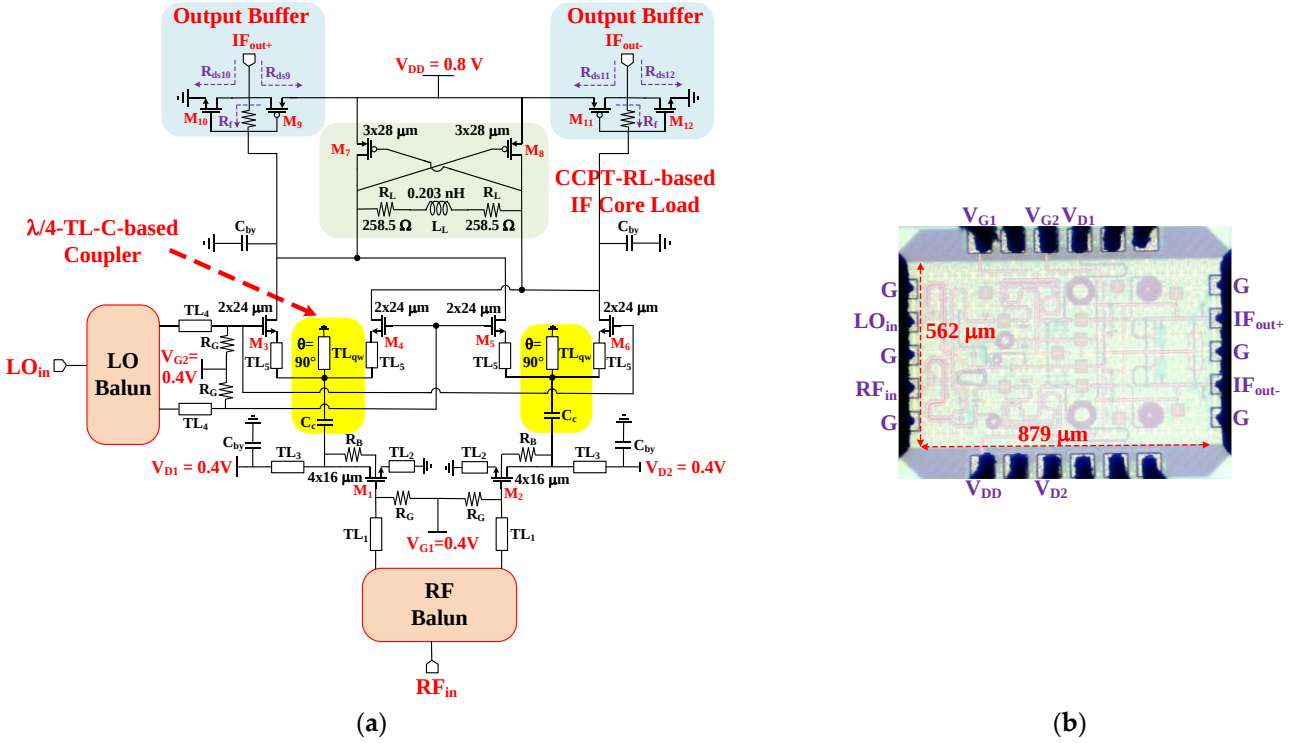



**Figure 2.** (**a**) Schematic diagram, and (**b**) chip photo of the down-conversion mixer.

Figure 3 presents the illustrative diagram of the 28 GHz-band Wilkinson-power-divider-based balun [12]. It is used as the RF and the LO baluns. The compact Wilkinson power divider constitutes a noninverting coupled line with an electrical length (θ) of 22°, a parallel grounded capacitance $C_{P1}$ at the input, and a parallel $R_PC_P$ between the outputs. The coupled line, i.e., two noninverting spiral or meandering TLs with inductance of $L_L$, has a positive mutual inductance (M) and an equivalent parallel inductance $L_P$ (=$L_L(L_L - 2M)/M$) between the outputs. This leads to a significant TL-length reduction (from about λ/10 to λ/16) for the power divider. The effect of $L_P$ can be cancelled by $C_m$ (=$M/[\omega_0^2 L_L(L_L - 2M)]$) in Figure 3. The π-network comprised of $C_{P2}$, $L_{S1}$, and $C_{P3}$ introduces a phase delay of 90°, while the T-network comprised of $C_{S1}$, $L_{P1}$, and $C_{S2}$ (or the π-network comprised of $L_{P2}$, $C_{S3}$, and $L_{P3}$) introduces a phase lead of 90°. This is the way to achieve balun operation of the device.

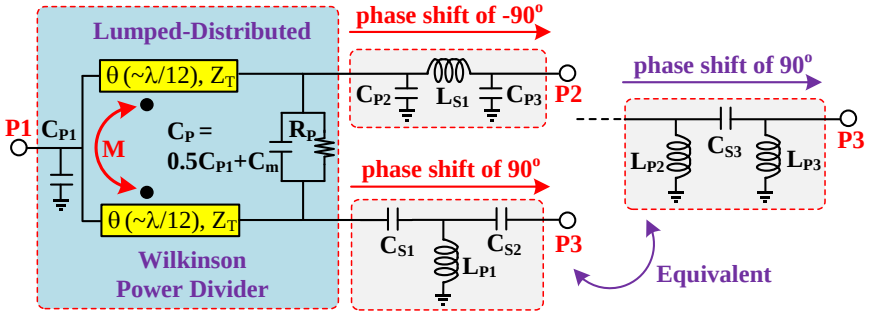
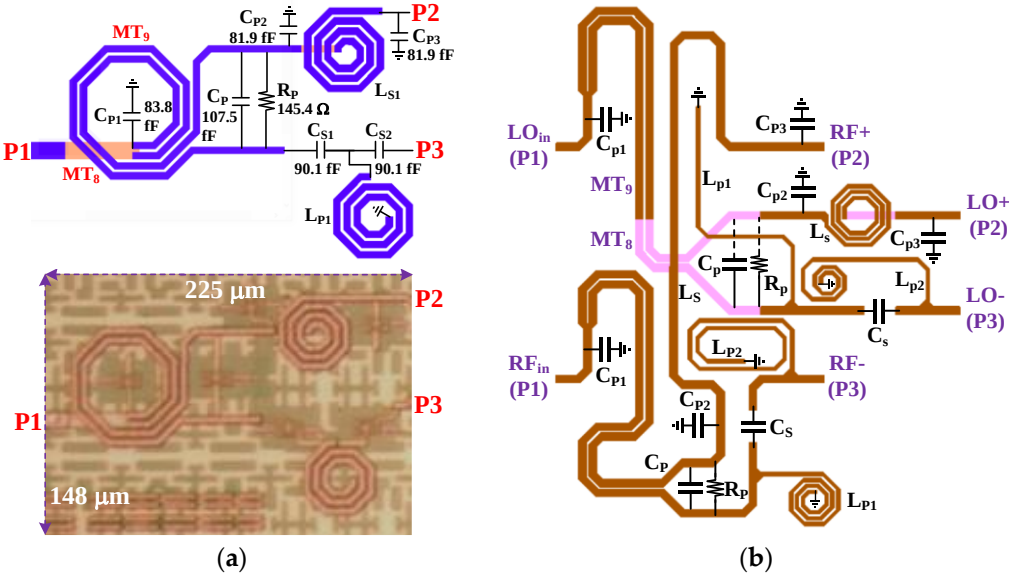



**Figure 3.** Illustrative diagram of the power-divider-based balun.

Shown in Figure 4a is the simplified layout and chip photo of the first test balun, balun-1. A spiral layout is used for $L_{S1}$ and $L_{P1}$ in order to achieve a compact size. Balun-1 occupies a chip area of only 0.225 × 0.148 $mm^2$, i.e., 0.033 $mm^2$. Figure 4b shows the simplified layout of the RF and the LO baluns (i.e., dual balun-2) of the down-conversion mixer in this work. A symmetrical layout is crucial for the differential mixer core to attain good port-to-port isolation and overall performance. Therefore, the dual-balun-2 layout

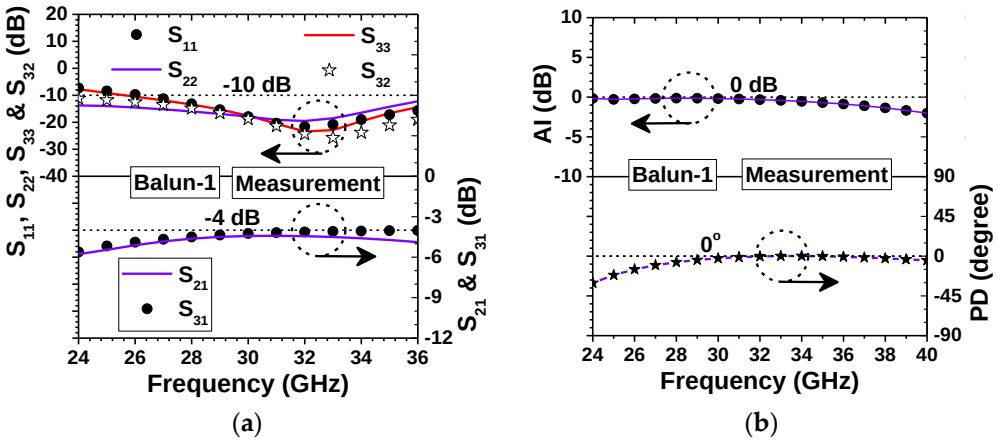
in Figure 4b is used to fit the symmetrical layout of the mixer core. The dual balun-2 occupies a chip area of 0.089 $mm^2$. According to our previous experience, measured results of mm-wave passive devices are consistent with the simulated results of the EM simulator HFSS and ADS Momentum [13]. To expedite the realization of the down-conversion mixer, tape-out of the mixer is conducted based on the EM-circuit cosimulation result of the layout, i.e., post-layout simulation result, via ADS Momentum. Therefore, tape-out of the test device of dual balun-2 was not performed.




(**a**) (**b**)

**Figure 4.** (**a**) Layout and chip photo of balun-1. (**b**) Layout of dual balun-2.

The measured reflection coefficients ($S_{11}$, $S_{22}$, and $S_{33}$), isolation between the outputs $S_{32}$, and gain ($S_{21}$ and $S_{31}$) of balun-1 are shown in Figure 5a. Balun-1 achieves a local minimum $S_{11}$ of −21.6 dB at 32 GHz and $S_{11}$ better than −10 dB from 26.2 GHz to over 50 GHz. The corresponding −10 dB input, matching the bandwidth ($f_{10dB}$), is wider than 23.8 GHz. Balun-1 achieves a local minimum $S_{22}$ of −19.5 dB at 32 GHz and $S_{22}$ better than −10 dB from DC to 36.7 GHz, equivalent to an $f_{10dB}$ of 36.7 GHz. Balun-1 achieves a minimum $S_{33}$ of −23.4 dB at 32 GHz and $S_{33}$ better than −10 dB for 25.7–39.7 GHz, equivalent to an $f_{10dB}$ of 14 GHz. Moreover, balun-1 attains a local minimum $S_{32}$ of −25.7 dB at 33 GHz and $S_{32}$ better than −10 dB from DC to over 50 GHz, equivalent to a −10 dB isolation bandwidth ($f_{10dB,iso}$) wider than 50 GHz. Balun-1 achieves $S_{21}$ of −4.441 dB at 32 GHz and $S_{21}$ better than −5 dB for 26.3–36.7 GHz, close to the measured $S_{31}$ (−4.131 dB at 32 GHz, and better than −5 dB from 25.5 GHz to over 50 GHz).




(**a**) (**b**)

**Figure 5.** Measured (**a**) S-parameters, and (**b**) AI and PD of balun-1.

Figure 5b shows the measured amplitude imbalance AI (equal to $S_{21}$(dB) − $S_{31}$(dB)) and phase deviation PD (equal to $S_{21}$(degree) − $S_{31}$(degree) − 180°) of balun-1. Balun-1 achieves the best AI of −0.127 dB at 28 GHz and AI within ±1 dB for 22.2–36.7 GHz, as well as the best PD of −0.08° at 35 GHz and PD within ±5° for 28.6–40.3 GHz. Compared to that with the commonly used Marchand balun with poor $S_{22}$, $S_{33}$, and $S_{32}$ (of −6 dB in theory) [8], better overall performance is achieved.

Figure 6a shows the simulated AI and PD of balun-2. Balun-2 attains the best AI of 0 dB at 27.5 GHz and AI within ±1 dB for 23.5–30.6 GHz, as well as the best PD of 0° at 26.4 GHz and PD within ±5° for 24.1–32.6 GHz. Figure 6b shows the simulated RF-port reflection coefficient ($S_{11}$), LO–RF isolation, CG, and NF of the mixer. The mixer achieves a minimum $S_{11}$ of −32.9 dB at 39 GHz and $S_{11}$ better than −10 dB for 21.7–44.5 GHz (i.e., $f_{10dB}$ of 22.8 GHz). The good $S_{11}$ is attributed to the decent input matching of the balun (see Figure 5a) and good matching between the balun outputs and the differential RF inputs. Due to the symmetrical layout and $C_{by}$ of the mixer core, the mixer achieves decent LO–RF isolation of 44.9 dB at 28 GHz and 40.3–62.4 dB for 0–50 GHz. Moreover, the mixer achieves a maximum CG of 15.8 dB at 26 GHz and CG of 14.3 ± 1.5 dB for 14.3–32.5 GHz (i.e., $f_{3dB}$ of 18.2 GHz). The decent CG and $f_{3dB}$ are attributed to the CCPT-RL-based core IF load and the gain-enhanced gm stage. The mixer achieves a minimum NF of 6.2 dB at 24 GHz and NF of 6.2–9.3 dB for 14–33 GHz. The good NF of the mixer is attributed to its high CG and simultaneous noise and $Z_{in}$ matching of the gm stage.

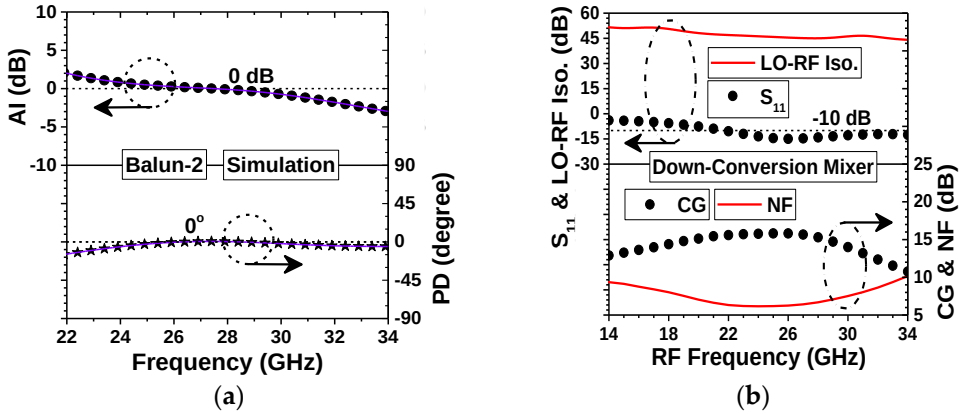



**Figure 6.** Simulated (**a**) AI and PD of balun-2, and (**b**) $S_{11}$, LO–RF isolation, CG, and NF of the down-conversion mixer.

## 3. Results

At $V_{DD}$ = 0.8 V and $V_{D1}$ = $V_{D2}$ = $V_{G1}$ = $V_{G2}$ = 0.4 V, the down-conversion mixer dissipates 6.5 mW, close to the simulated one (6.4 mW). The on-wafer S-parameter measurement of the mixer was conducted using a Keysight N5245B four-port PNA network analyzer (0.01–50 GHz). Figure 7a shows the measured and simulated RF-port reflection coefficient ($S_{11}$) of the mixer. The mixer achieves a measured minimum $S_{11}$ of −34.6 dB at 40 GHz and $S_{11}$ better than −10 dB for 20.4–44.2 GHz (i.e., $f_{10dB}$ of 23.8 GHz), close to the simulated result (minimum $S_{11}$ of −32.9 dB at 39 GHz and $f_{10dB}$ of 22.8 GHz (21.7–44.5 GHz)). For a mixer or amplifier using series RLC resonance matching, its $f_{10dB}$ ($50/(3\pi L_{in})$ in theory) is inversely proportional to the input inductance $L_{in}$ [14,15]. For the differential RF inputs, $L_{in}$ (i.e., sum of the inductance of $TL_1$ and $TL_2$) is 435 pH, equivalent to $f_{10dB}$ of 12.2 GHz. The wideband $S_{11}$ of the mixer is attributed to the wideband matching between the RF-balun outputs and the RF inputs due to the small $L_{in}$ at RF inputs. Figure 7b shows the measured and simulated IF+ port reflection coefficient ($S_{33}$) of the mixer. The mixer achieves a measured $S_{33}$ better than −10 dB for 0–10.2 GHz (i.e., $f_{10dB}$ of 10.2 GHz), close to the simulated one ($f_{10dB}$ of 15.1 GHz (0–15.1 GHz)). The wideband $S_{33}$ is attributed to the $Z_{in}$ matching at low frequency (LF) since the design values of $R_{ds9}$||$R_{ds10}$||$R_f$ and $R_{ds11}$||$R_{ds12}$||$R_f$ are 50 Ω. The slight deviation of the measured $S_{11}$ and $S_{33}$ (from the simulated

ones) of the down-conversion mixer is mainly attributed to the substrate- and layout-layer parameters provided by the foundry being not accurate enough at mm-wave frequencies.

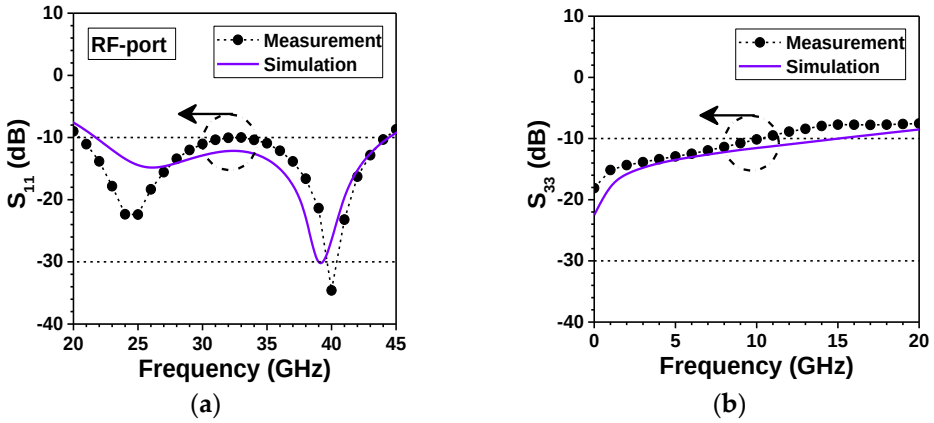



**Figure 7.** Measured and simulated (**a**) $S_{11}$, and (**b**) $S_{33}$ of the mixer.

Figure 8a shows the measured and simulated LO–RF and LO–IF isolation versus LO frequency characteristics of the mixer. The mixer achieves measured LO–RF isolation of 46.1 dB at 28 GHz and 41.6–55.9 dB for 0–50 GHz, close to the simulated one (44.9 dB at 28 GHz, and 40.3–62.4 dB for 0–50 GHz). Since the Miller capacitance (of $C_{gd}$) at D1/D2 of $M_1/M_2$ has been taken into account in the $C_d$ calculation, the decent LO–RF isolation is attributed to the symmetrical layout of the mixer core, and unilaterilization of the $C_{gd}$ effect of $M_1/M_2$. Moreover, the mixer achieves measured LO–IF isolation of 39.9 dB at 28 GHz and 36.6–82.7 dB for 0–50 GHz, close to the simulated one (43.3 dB at 28 GHz, and 36–84.8 dB for 0–50 GHz). The decent LO–IF isolation (especially at LF) is attributed to the symmetrical layout of the mixer core and the inclusion of $C_{by}$ between $M_3/M_5$ and $M_9/M_{10}$ (and $M_4/M_6$ and $M_{11}/M_{12}$) for low-pass filtering of the LO leakage. In brief, LO leakage around $f_0$ is suppressed by $C_{by}$. Therefore, LF (around DC) leakage at the IF output is minimized due to the effective suppression of the second-order nonlinearity of the CCPT-RL-based core IF load and the output buffer amplifiers. Figure 8b shows the measured and simulated CG versus $LO_{in}$ characteristics of the mixer at 28 GHz. Intrinsically, the mixer is a nonlinear multiplier. Hence, it is reasonable that the CG of the mixer increases with the increase in $LO_{in}$ until saturation of the LO switch transistors (i.e., close to perfect switch operation). At $LO_{in}$ of 0 dBm, the mixer achieves a measured/simulated CG of 15.6/15.7 dBm, close to those (16.6/16.2 dBm) at $LO_{in}$ of 4 dBm. This indicates that $LO_{in}$ of 0 dBm is a reasonable choice for the switch operation of the LO switch transistors.

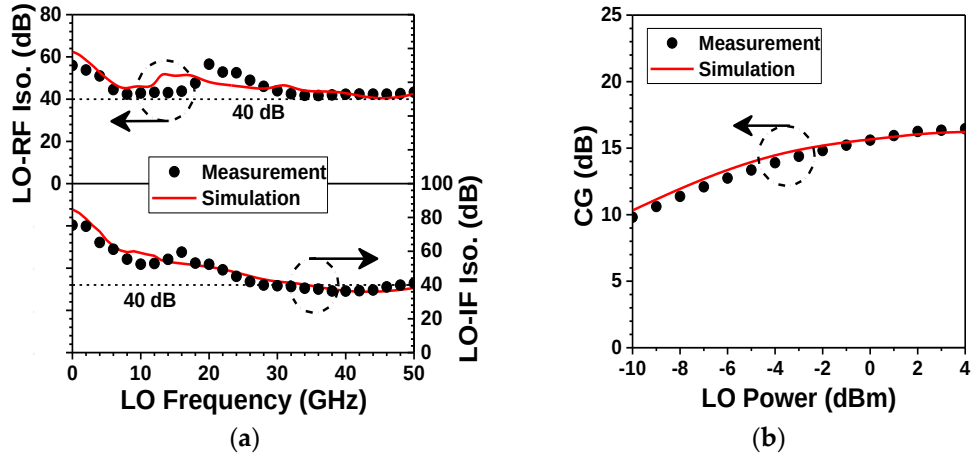



**Figure 8.** Measured and simulated (**a**) LO–RF and LO–IF isolation versus LO frequency, and (**b**) CG versus LO input power characteristics of the mixer.

The on-wafer NF measurement was performed using an Agilent N8975A noise figure analyzer (0.01–26.5 GHz). An Agilent 1–50 GHz noise source with a 7–20 dB excess noise ratio (ENR) is used at the RF input. The LO input signal is provided by an Agilent E8257D signal generator (up to 67 GHz). Figure 9a shows the measured and simulated CG and NF versus RF frequency characteristics of the mixer. IF frequency is fixed at 0.1 GHz. The mixer achieves a measured CG of 15.6 dB at 28 GHz and CG of 14.4 ± 1.5 dB for 12.4–32 GHz, corresponding to an $f_{3dB}$ of 19.6 GHz. The result is close to the simulated CG (15.7 dB at 28 GHz and 14.3 ± 1.5 dB for 14.3–32.5 GHz, corresponding to an $f_{3dB}$ of 18.2 GHz). The broadband CG of the mixer is attributed to the wideband RF- and LO-port $Z_{in}$ matching ($S_{11}$ and $S_{22}$) and near perfect wideband-coupling of the λ/4-TL-C-based coupler. Moreover, the mixer achieves a measured NF of 7.6 dB at 28 GHz and 7–9.7 dB for 12.4–32 GHz, close to the simulated NF (6.7 dB at 28 GHz and 6.2–9.3 dB for 12.4–33 GHz). Figure 9b shows the measured and simulated CG and NF versus IF frequency characteristics of the mixer. The mixer achieves a measured CG of 15.6–12.6 dB for 0.1–1.9 GHz. The 3 dB IF bandwidth ($f_{3dB,IF}$) is 1.9 GHz, wider than the required 1.5 GHz for 5G NR band N257 (28 ± 1.5 GHz) application. The result is close to the simulated one (15.7–12.7 dB for 0.1–2.2 GHz, i.e., $f_{3dB,IF}$ of 2.2 GHz). The mixer achieves a measured NF of 7.6–8.1 dB for 0.1–1.9 GHz, close to the simulated one (7.7–8.3 dB for 0.1–2.2 GHz). Furthermore, the mixer achieves a decent $P_{1dB}$ and IIP3 of −10.6 dBm and −1 dBm, respectively. For a larger $V_{DD}$ of 1 V, a better IIP3 of 1 dBm is achieved (not shown here).

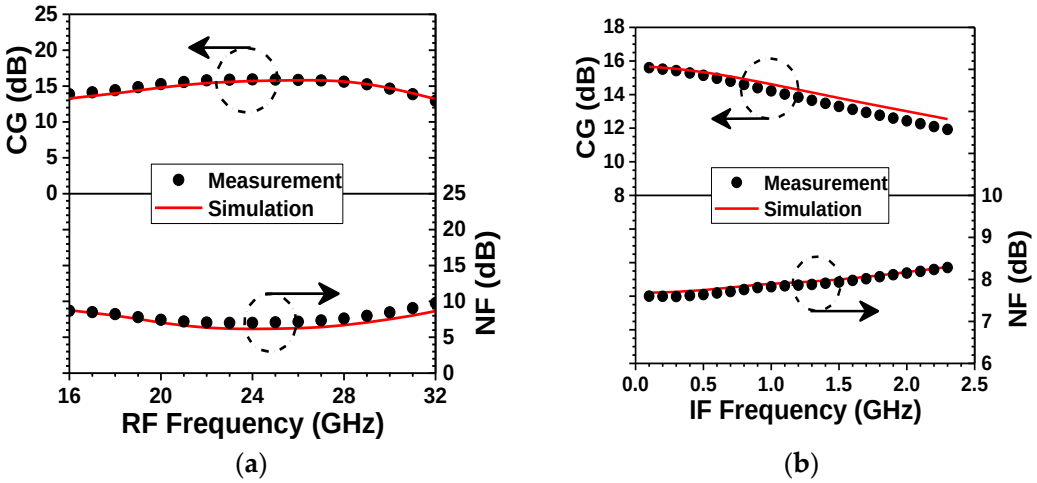



**Figure 9.** Measured and simulated (**a**) CG and NF versus RF frequency, and (**b**) CG and NF versus IF frequency characteristics of the mixer.

Table 1 is a summary of the 28 GHz down-conversion mixer and recently reported state-of-the-art mm-wave CMOS down-conversion mixers [1–7]. As can be seen, the mixer in this work is designed and implemented via a relatively cost-effective 90 nm CMOS process and achieves better overall performance than the mixer implemented with the costlier 40 nm CMOS technology in [6]. If a more advanced CMOS process is used for the mixer in this work, the overall performance can be further enhanced. This means that the proposed down-conversion mixer architecture has high potential for mm-wave communication systems. Overall, compared with that in [1–7], our mixer occupies a medium chip area, requires a medium $LO_{in}$, consumes low power, and achieves prominent CG, $f_{3dB}$, NF, LO–RF isolation, and IIP, and one of the best $FOM_1$s and $FOM_2$s. The remarkable results indicate that the proposed down-conversion mixer architecture is suitable for 28 GHz 5G NR and even a higher frequency system.

**Table 1.** Summary of the down-conversion mixer and recently reported state-of-the-art mm-wave down-conversion mixers.

| | CMOS Process | Topology | RF Freq. (GHz) | $LO_{in}$ (dBm) | CG (dB) | $f_{3dB}$ BW (GHz) | LO–RF Iso. (dB) | NF (dB) | IIP3 (dBm) | $P_{DC}$ (mW) | Area ($mm^2$) | $FOM_1$ | $FOM_2$ ($mW^{-1}$) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| This Work | 90 nm | Gilbert-cell with λ/4-TL-C-based coupler | 28 | 0 | 15.6 | 19.6 (12.4–32) | 46.1 | 7.6 | −1 | 6.5 | 0.494 | 0.023 | 0.14 |
| [1] | 90 nm | Double-balanced Gilbert-cell | 28 | 1 | −3.3 | 6 (25–31) | 47.4 | 14.3 | −3.4 | 6.4 | 0.522 | $8.7 \times 10^{-5}$ | $4.9 \times 10^{-3}$ |
| [2] | 65 nm | Double-balanced Gilbert-cell + IF buffer | 28 | 5 | 7.2 | 13 (26–39) | N/A | 12.3 | −2.5 | 10.3 | 0.4 | $6.1 \times 10^{-4}$ | 0.017 |
| [3] | 0.13 µm | Folded Gilbert-cell +IF buffer | 24 | −3 | 26.1 | 2 (23–25) | 58 | 7.7 | −27.4 | 16.8 | 0.96 | $8.9 \times 10^{-6}$ | 0.024 |
| [4] | 0.18 µm | Gilbert-cell using distributed DS tech. | 24 | 5 | −4.5 | 4 (22–26) | N/A | N/A | 23 | 16 | 0.72 | N/A | $2.48 \times 10^{-3}$ |
| [5] | 90 nm | Single balance with CCP feedback | 60 | 1 | 6.95 | 10 (57–67) | 50 | 14.4 | 0.2 | 16 | 0.35 | $4.2 \times 10^{-4}$ | 0.011 |
| [6] | 40 nm | Sub-harmonic+ Current-reused | 60 | 5 | −7.9 | 10.5 (56.5–67) | 45 (2LO–RF) | 14.4 | 0.1 | 3.45 | 0.586 | N/A | $5.3 \times 10^{-3}$ |
| [7] | 65 nm | Transformer-coupling cascode topology | 60/77 | −3 | 9.5 | 28 (62–90) | 48 | 9.2 | 5.8 | 15 | 0.527 | 0.017 | 0.033 |

$FOM_1 = CG[1] \cdot BW[GHz] \cdot IIP3[mW]/[(F-1)[1] \cdot P_{DC}[mW] \cdot f_T[GHz]]$, $FOM_2[mW^{-1}] = CG[1] \cdot BW[GHz]/[P_{DC}[mW] \cdot f_T[GHz]]$.

Finally, it would be informative to provide readers with a futuristic vision about what the future holds for us as we move forward [16–19]. Considering the saturation of the state-of-the-art microelectronic technologies in providing a faster operation speed, nowadays, hybrid optoelectronic platforms are considered a new solution to expand the operation bandwidth, while we can still enjoy the CMOS technology for implementing such hybrid systems. One direction that is gaining large momentum in the field is the utilization of hot-electron optoelectronic nano-devices. This concept relies on the fact that metals have an abundance of free electrons, so they can nicely capture light if they are fashioned as a nanoscale optical antenna. In addition, employing metals is a necessary part of electronic circuits, e.g., as electrical contacts. Therefore, if meticulously designed, a nano-metal with optical antenna properties can be used as an electrical contact as well; therefore, one can access the hot electrons in metals for optoelectronic applications [16]. Such hot carriers can enable the extremely fast switching of electrical signals [17]. In a capacitor configuration, such high-energy hot electrons have the possibility of being transported over a Schottky barrier in a very short timeframe. The injection of hot carriers into a dielectric/oxide/air material will change its conductivity in a very short timescale, thereby allowing for ultrafast optoelectronic switching, which is inherently a frequency down conversion process. The beauty of this technique is hidden in the fact that hot-electron optoelectronic systems do not rely on the absorption of light in a semiconductor. Therefore, practically any oxide or metal combination can be employed to produce a hot-electron optoelectronic convertor without being concerned about the intrinsic properties of employed materials or a capacitive nature of the circuit, which limits the bandwidth. Initial demonstrations of such switches were proposed recently [18,19]. However, practical devices are yet to be demonstrated.

## 4. Conclusions

We demonstrate a 6.5 mW 12.4–32 GHz CMOS down-conversion mixer with a decent CG of 14.4 ± 1.5 dB and NF of 7–9.7 dB for 28 GHz 5G NR. A λ/4-TL-C-based coupler is used for harmonic suppression and near-perfect coupling from the RF gm stage to the LO switch transistors. The BSFB technique is used for $V_{th}$ and $V_{DD}$ reduction. The CCPT-RL-based core IF load is used for $Z_L$ (i.e., CG) and $f_{3dB,IF}$ boosting. CG and NF enhancement at the same (or even a lower) $P_{DC}$ is achieved due to a lower $V_{DD}$ and higher gm and $Z_L$. As a result, low $P_{DC}$ and optimized CG, NF, and linearity are achieved for the mixer due to the separate bias (i.e., optimized design) of the gm stage and the IF loads.

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