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# A 12 bit 2.9 GS/s DAC With $IM3 < -60$ dBc Beyond 1 GHz in 65 nm CMOS

Chi-Hung Lin, Frank M. L. van der Goes, Jan R. Westra, Jan Mulder, Yu Lin, Erol Arslan, Emre Ayranci, Xiaodong Liu, and Klaas Bult

**Abstract**—A 12 bit 2.9 GS/s current-steering DAC implemented in 65 nm CMOS is presented, with an  $IM3 < -60$  dBc beyond 1 GHz while driving a  $50 \Omega$  load with an output swing of  $2.5 V_{DD}$  and dissipating a power of 188 mW. The SFDR measured at 2.9 GS/s is better than 60 dB beyond 340 MHz while the SFDR measured at 1.6 GS/s is better than 60 dB beyond 440 MHz. The increase in performance at high-frequencies, compared to previously published results, is mainly obtained by adding local cascodes on top of the current-switches with “always-ON” biasing.

**Index Terms**—CMOS, current-steering, D/A converters, digital-to-analog converter (DAC), full Nyquist, HD3, high frequency, high speed,  $IM3$ .

## I. INTRODUCTION

IN LARGE systems-on-chips (SoC), data converters are critical for connecting signals to the real world, often limiting the accuracy and speed of the overall system. The clear trend towards digital signal processing of traditional analog functions, reducing the analog front-end (AFE) and analog back-end (ABE) to a bare minimum, by connecting the data converter directly to the terminals, requires very high bandwidth and sampling speeds. As an example, 10 GBASE-T Ethernet requires a transmit DAC sampling at 1.6 GS/s with at least  $-70$  dB  $IM3$  up to a frequency of 400 MHz, while supporting an amplitude of  $2.5 V_{DD}$  driven in to a  $50 \Omega$  load.

In recent years, many papers have been published on high-speed DAC design [1]–[9], [11]. Most of these designs concentrate on obtaining good low-frequency performance and use techniques like calibration [1] or dynamic element matching [11]. However, these techniques do not help the performance at higher frequencies since at those frequencies matching problems are not the limiting factor anymore. The goal of this paper is to design a DAC which achieves a minimum of  $-70$  dB  $IM3$  at low frequencies, maintains that performance up to a minimum of 400 MHz and achieves at least  $-60$  dB  $IM3$  at 800 MHz, as is shown in Fig. 1. Currently, no published designs meet these requirements.

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C.-H. Lin is with Broadcom Corporation, Irvine, CA 92618 USA.

F. M. L. van der Goes, J. R. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult are with Broadcom Netherlands BV, 3981AJ Bunnik, The Netherlands.

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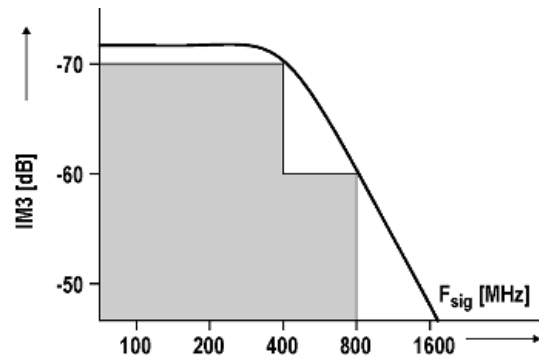


Fig. 1.  $IM3$  requirements for this design.

Section II introduces the chosen architecture. Sections III and IV deal with various distortion mechanisms that are dominant at low and high frequencies, respectively. In Section V the DAC cell for the thermometer-coded coarse DAC is shown and the implemented techniques are discussed in detail. The test chip and setup are discussed in Section VI, and the results of measurements along with a comparison with the theory (as discussed in Section V) as well as with previously published data are shown in Section VII. Finally, Section VIII summarizes the conclusions.

## II. ARCHITECTURE

For fast-sampling applications the current-steering architecture is the architecture of choice [1]–[9]. Because of the obvious advantages of thermometer-coded DACs with respect to differential nonlinearity (DNL), glitch energy, monotonicity and linearity on the one hand and on the other hand the advantages of binary-coded DACs with respect to compactness and simplicity, a segmented design was chosen (Fig. 2). Using the approach outlined in [2] the optimal segmentation ratio was determined and a 6 bit thermometer-coded DAC was combined with a 6 bit binary-coded DAC. A transformer connects the DAC to the load. For proper termination reasons, on each side of the transformer the impedance equals  $100 \Omega$  and the total effective impedance to the DAC equals  $50 \Omega$ .

The thermometer-coded MSB section (coarse DAC) determines the overall performance with respect to linearity and most of the design effort was focused on that block. The architecture is shown in Fig. 3. Although the final layout was not done in a matrix-style layout but rather in a single-line layout, the cells are driven by row and column decoders as this turns out to be area efficient. Latches are placed at the input of the DAC, after the column and row decoding and inside the cells.

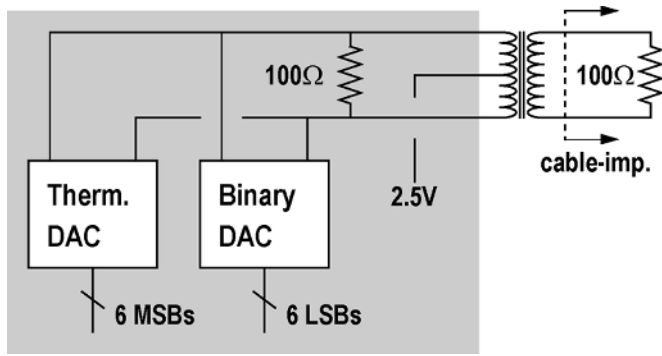


Fig. 2. Top-level architecture.

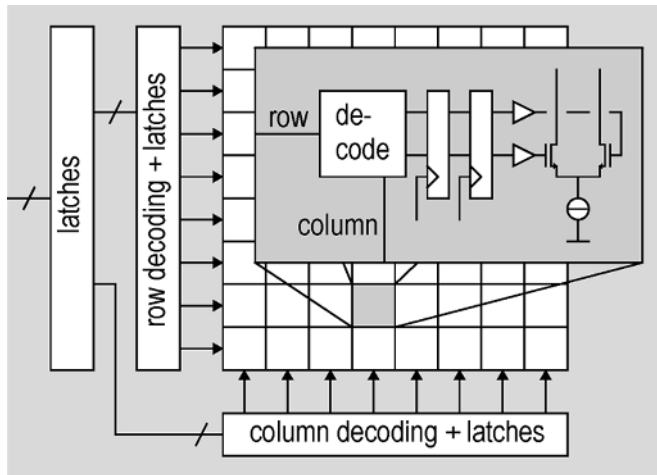


Fig. 3. Thermometer-coded coarse DAC.

### III. LOW-FREQUENCY PERFORMANCE

This section deals with error mechanisms that are frequency-independent and as such will dominate the accuracy at low frequencies.

#### A. Matching

Transistor mismatch in the current source of the DAC cell is a source of nonlinearity, especially in the coarse DAC. Care has to be taken to obtain good matching by using sufficient gate area [10], short distances between the transistors and equal environments through the use of dummy transistors. Many papers have been written about various techniques to improve matching between current sources, like calibration techniques [1] or dynamic element matching (DEM) [11]. Although there are ample examples of papers that show that for low frequencies this does indeed improve the linearity of the DAC, for high frequencies these techniques in general do not help and could possibly even degrade the performance. This is mostly because both techniques can cause extra tones in the output spectrum and complicate the design significantly, including the layout, whereas high-frequency performance mostly benefits from simplicity and low parasitic capacitances. As a result no matching improvement techniques were used other than proper layout and proper transistor sizing.

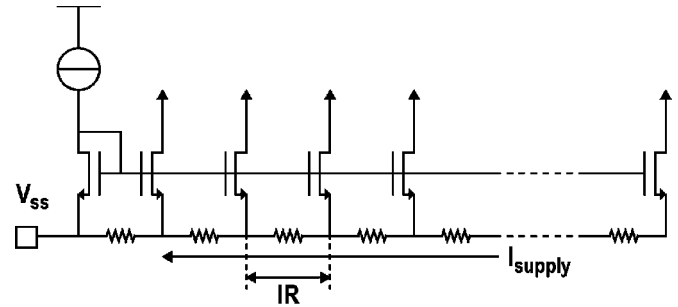


Fig. 4. IR drop in the supply line causes DNL.

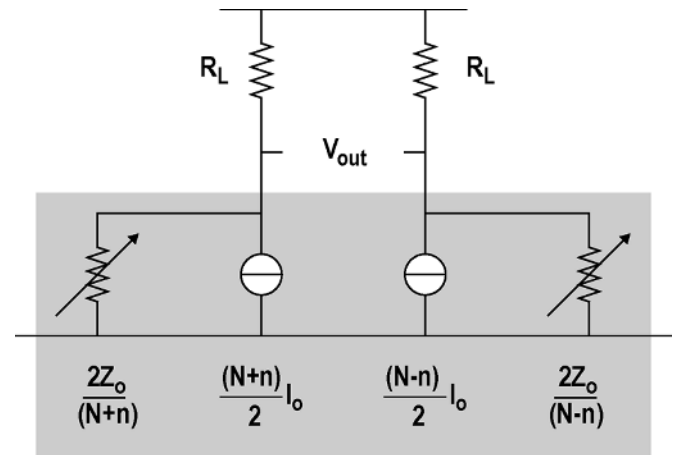


Fig. 5. The effect of finite current source output impedance on DAC linearity.

#### B. IR Drops on the Supply

Routing of the supply lines to the DAC current sources is a critical step. As the supply lines carry current, any resistance will cause voltage drops (“IR”, see Fig. 4) on the supply line, which in turn can cause the individual gate–source voltages to be unequal [12]. As a result the value of the currents will become smaller (or bigger) along the supply line (Fig. 4), causing not only a DNL problem, but, without any randomization, could also cause significant integral nonlinearity (INL) problems. Solutions can be found in using wide power supply lines and binary trees for the supply grid.

#### C. Finite Output Impedance

Finite output impedance of DAC current sources leads to distortion, as has been pointed out by several authors [4], [8], [9]. Fig. 5 shows a thermometer-coded DAC with ideal current sources, but with finite current source output impedance  $Z_o$ . In this graph,  $N$  equals the total number of current sources,  $I_o$  is the value of one current source and  $n$  equals the digital input code ( $-N \leq n \leq N$ ). Depending on the digital input code, more or less current sources are connected to the left and the right output nodes. Along with that also more or less output impedances are connected in parallel with the load impedance  $R_L$ . This means that the total effective load impedance becomes signal-dependent. Since the output voltage is a simple multiplication of the current and the output impedance, a signal-dependent load impedance leads to distortion.

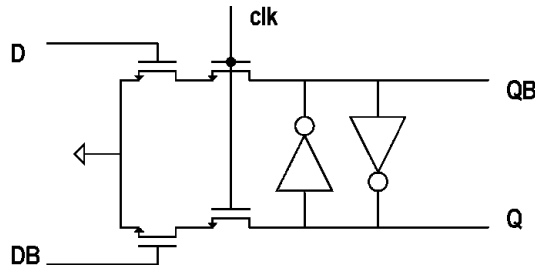


Fig. 6. Fast latch.

A straightforward calculation of the transfer function from the digital input word ( $n$ ) to the output voltage  $V_{\text{out}}$  in Fig. 5 leads to the following expression:

$$V_{\text{out}} = R_L N I_o \left[ \left( \frac{n}{N} \right) + \left( \frac{n}{N} \right)^3 \left[ \frac{R_L N}{2R_o} \right]^2 \right]. \quad (1)$$

For full swing conditions ( $n = N$ ) the expression for third-order distortion becomes

$$\text{HD3} = \left[ \frac{R_L N}{4R_o} \right]^2. \quad (2)$$

As (2) shows, low third-order distortion (due to this mechanism only) requires a high output impedance from each current source:  $R_o \gg NR_L$ . This can be fairly easily achieved at low frequencies by cascoding and if necessary double or active cascoding. For high frequencies this is not a sufficient solution as will be shown in Section IV.

#### IV. HIGH-FREQUENCY PERFORMANCE

High-frequency performance is quite a different problem from its low-frequency counterpart and special measures have to be taken.

##### A. Switch Gate Driving

It is well known that it is important to keep the voltage across the current sources as stable as possible during the output current transition from one side to the other [2], [8]. Special gate-driving circuits have been developed for that purpose [8]. However, it is also important that the transition itself is as short as possible. The main reasons for that are to reduce the effects of switch driver mismatch, clock jitter, decoding feedthrough and, to some extent, device noise.

CML drivers are often used to obtain maximum possible clock speed (because of the reduced swing), but the steepest transitions are obtained using regular CMOS logic. In this design the latch of Fig. 6 is used for two reasons: it creates the steepest transition [2] and has the shortest clock-to-Q delay known to the authors [8]. Inherently, this circuit has a low crossing of the Q and QB signals. If followed by inverters for Q and QB, the signals become high-crossing and can be used to drive the switch gates directly. It was found that the rapid transitions exhibited by this circuit have more benefits than any reduced swing circuit known to the authors.

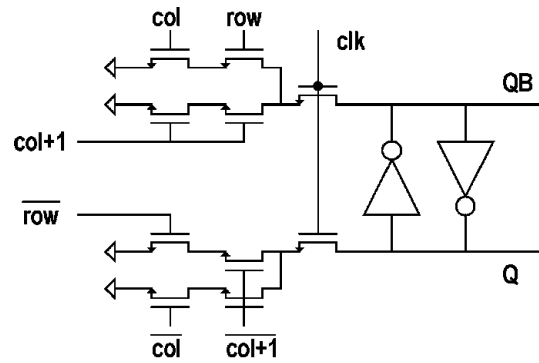


Fig. 7. Latch with symmetrical decoding.

##### B. Decoding Feedthrough

Since decoding signals contain information about the input signal, any feedthrough from the decoding to the DAC output can lead to distortion. As an example, in [8] data-dependent clock loading is discussed and a solution is presented. Another error mechanism is nonsymmetrical decoding. In the design presented here, decoding is done as if the current source cells were distributed in a matrix-style layout, using column and row signals [2]. A cell can get activated either because the next column signal is active or the current column and the current row are active. The circuit in Fig. 7 has been used to make sure that in all cases the cell gets activated with the same signal strength [3].

At high speed the transition of digital signals can still have a finite settling effect at the end of the clock period and a difference can emerge between the values of those signals that had to transition and those that already transitioned in a previous clock period. Adding an extra latch (Fig. 3) reduces this effect considerably.

##### C. Switch Driver Mismatch

Mismatch in switch driver transistors can lead to small differences in the speed of the transition and therefore also the exact switching moment. Deviations in switching moments are more important at higher signal speeds and therefore a degradation proportional to frequency is to be expected. Therefore, for good high-frequency performance, care should be taken to obtain good matching of the driver transistors. However, since any spread in switching moment is proportional to the switching time, the absolute transition of the driving signal should be as fast as possible. Both good matching as well as a fast transition require the driver transistors to be fairly large. The latch or logic preceding the driver is less sensitive and can be scaled down in size, leading to a tapered design in logic, latches and driver. Also the supply line needs to be low-Ohmic and routed in such a way that the actual driving strength for all drivers is matching well.

##### D. Output Current Tree

Equal delays are not only relevant in the clock-tree but just as much in the signal path. For that reason it is crucial to design the paths from the cells to the output nodes as well matched as possible. A binary output-current tree is used in an effort to keep all possible delays in the signal path the same.

### E. Output Impedance at Higher Frequencies

As discussed in Section III-C, finite current source output impedance causes distortion in current-steering DACs. Equation (2) shows the expression for third harmonic distortion (HD3) at low frequencies. In the analysis it was assumed that the output impedance was purely real and equal to  $R_o$ . At higher frequencies this assumption is no longer valid. A better assumption would be that the output impedance can be modeled by the parallel connection of a resistor and a capacitor:

$$Z_o = R_o // \left( \frac{1}{j\omega C_o} \right). \quad (3)$$

An expression for HD3 valid for all frequencies is found by substituting  $R_o$  in (2) by  $|Z_o|$ :

$$\text{HD3} = \left[ \frac{R_L N}{4|Z_o|} \right]^2. \quad (4)$$

As the impedance  $Z_o$  shows a first-order roll-off with frequency, it can be expected that for higher frequencies ( $\omega > 1/R_o C_o$ ) HD3 will degrade quadratically with frequency and this will become the dominant distortion mechanism. The effective output capacitance  $C_o$  being switched back and forth between the positive and the negative output will be referred to as the “switching capacitor” in the remainder of this paper and should be kept small.

A numerical example may make the above more clear. A 12 bit DAC is built from a 6 bit fine DAC and a 6 bit coarse DAC and the coarse DAC is thermometer coded. The number of current sources in the coarse DAC is 64 ( $= N$ ). Using (4) with a load resistance of  $50 \Omega (= R_L)$  and  $\text{HD3} \leq -67.5 \text{ dB} (= \text{IM3} \leq -70 \text{ dB})$  yields  $|Z_o| \geq 39 \text{ k}\Omega$ , which seems reasonable and could be achieved through cascoding. However, if this level of HD3 also is required at an output frequency of 600 MHz, the maximum capacitance in this impedance can be no more than 6.8 fF. This is very difficult to achieve indeed.

## V. THE DAC CELL

After discussing various error mechanisms in Sections III and IV, this section deals with the solution proposed here. The DAC-cell designed to combat these issues is shown in Fig. 8.

### A. Low-Frequency Issues

To obtain good matching between the coarse DAC currents, it is of key importance that transistor M1 is well matched to its counterparts in the other DAC cells. For this reason M1 is sized large enough to support the required matching [10] and is placed in a large array of transistors with ample dummy transistors placed at each end of the array. Triple cascoding (M2, M3/M4 and M5/M6) is used to prevent finite output impedance of the current sources dominating the low-frequency distortion.

### B. High-Frequency Output Impedance

The goal of this paper is to obtain good harmonic performance even at high frequencies. As pointed out in Section IV-F, it is crucial to keep the effective “switching” capacitance  $C_o$  as

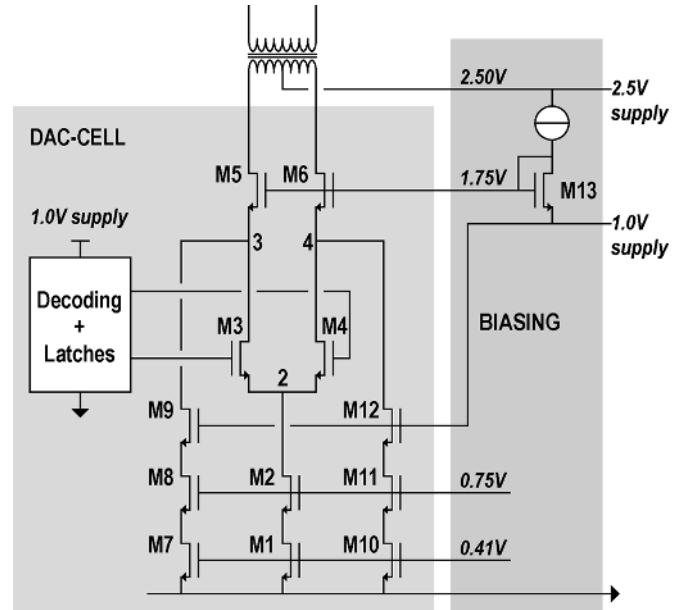


Fig. 8. DAC cell with biasing.

small as possible. Therefore, M2 is sized as small as possible to reduce the parasitic capacitance at the sources of switches M3 and M4, which themselves are also sized minimally. Since the switches operate with a large  $V_{gs}$ , their sizes are close to the minimum allowed in the technology. The device sizes in the DAC cell are therefore large at the bottom (for good accuracy), getting smaller in the middle (just large enough to support the current) and close to the minimum at the switches.

As discussed in Section V-A, M5 and M6 are added in each cell to reduce the effect of finite output impedance at low frequencies. Unfortunately, at higher frequencies this technique does not work that well. M5 and M6 do reduce the effect of parasitic capacitances from M1–M4, but also add their own parasitic capacitances, primarily their own  $C_{gs}$ 's [9]. When M3 and M4 are switching, so are the  $C_{gs}$ 's of M5 and M6 and they become the dominant limitation of the switching output impedance of the current source.

### C. The “Switching Impedance”

It is important at this point, to realize that the part of the output impedance that is degrading the distortion performance is only that part which is actually switching. Any impedances (like parasitic capacitances) which are not switching, but are rather fixed at each side of the output, are not contributing to distortion. This observation leads to one of the key contributions of this paper. In the remainder of this paper the term “switching impedance” is used for that part of the output impedance that is actually switching, equivalent to  $Z_o$  in (3) and (4). At higher frequencies  $Z_o$  is dominated by the “switching capacitance”  $C_o$ .

### D. The Proposed Solution

Adding small current sources (M7–M9 and M10–M12) to the sources of cascodes M5–M6 prevents the cascodes from being fully switched off. This means that even if the current from the

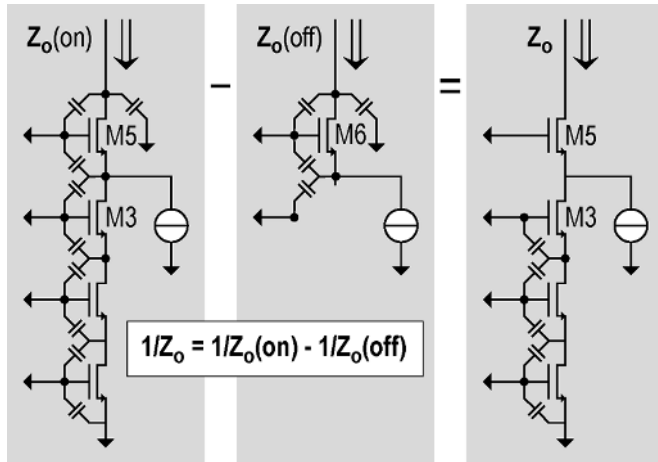


Fig. 9. Subtracting the “off” impedance  $Z_o$  (off) from the “on” impedance  $Z_o$  (on). The resulting switching-impedance  $Z_o$  is shown on the right.

current source M1/M2 is not routed through a particular cascode, that cascode remains active. In turn this means that the parasitic capacitances associated with nodes 3 and 4 can still be observed from the DAC cell output, irrespective of the status of the switches M3–M4. Since switching the current in the cell from one side to the other does not change the effective capacitance seen from the output node as a result of the parasitic capacitors associated with nodes 3 and 4, these capacitors will not contribute to distortion degradation. Now, the first capacitors that due to the switching of the cell will cause an observable change in the effective capacitance seen at the output are the  $C_{gs}$ 's of M3 and M4. However, their effect on finite output impedance is reduced by the intrinsic gain ( $g_m \cdot r_{out}$ ) of the cascode transistors M5–M6. The use of the cascode transistors M5–M6 together with the small current sources M7–M9 and M10–M12 achieves a reduction of the observable “switching” output impedance, and therefore also the distortion, by an order of magnitude.

To make the solution proposed here more clear, the effect discussed above is illustrated in Fig. 9, where both the circuits of the “on” impedance  $Z_o$  (on) as well as the “off” impedance  $Z_o$  (off) are shown. The switching impedance  $Z_o$  can be obtained mathematically through

$$\frac{1}{Z_o} = \frac{1}{Z_o(on)} - \frac{1}{Z_o(off)} \quad (5)$$

as is shown in Fig. 9. By “subtracting” the two circuits, as a result of which all the capacitances associated with M5/M6 are cancelled, the first “switching” capacitor observable from the output becomes the  $C_{gs}$  of M3/M4. However, the effect of this capacitance is reduced by the intrinsic gain of both M3/M4 as well as M5/M6, improving the performance by a factor  $(g_m \cdot r_{out})^2$ .

In order to keep the power dissipation as low as possible, the additional current sources should be kept as small as possible. Their sole purpose is to keep M5–M6 “on” in order to keep the parasitic capacitances associated with nodes 3 and 4 observable at all times. However, if the additional current source values are too small, the switching of the DAC cell will vary the  $C_{gs}$ 's of M5–M6 too much and a finite effect on distortion will be

the result. Simulations have shown that a relative small value of 1%–2% of the main current source is sufficient to keep the  $C_{gs}$ 's of M5–M6 fairly constant.

It should be noted that a similar configuration (pseudo-differential instead of differential) has been presented in [13]; also an additional current is fed to a cascode on top of a switched current source. However, in their case the purpose to do this is to keep the cascode in strong inversion in order to allow fast switching. The advantage with respect to distortion is not mentioned. Since the purpose of the DAC in [13] is to produce a PAM-4 signal, no distortion measurements are supplied either.

### E. Biasing

Fig. 8 also shows the biasing of this design. A transformer was used to connect to the load impedance. As the total effective load impedance is  $50 \Omega$  and a  $2.5 V_{ppd}$  swing is required by the application, the total available current for driving the load is 50 mA. As a result of that large signal swing, the center tap of the transformer is biased at 2.5 V, which necessitates the use of thick-oxide devices for M5 and M6. All other DAC cell transistors are thin-oxide transistors.

To prevent that any of the other transistors see more than the allowed 1.0 V at their drain terminals, M5 and M6 are biased as shown in Fig. 8 on the right side. A thick-oxide bias diode (M13), with its source connected to the 1.0 V supply, is used to bias the gates of M5 and M6 in such a way that their sources are always a few hundred mV below the 1.0 V supply. Since the small current sources M7–M9 and M10–M12 keep M5 and M6 always on, there is no risk that nodes 3 and 4 will go beyond 1.0 V. The gates of the second cascodes in the additional current sources (M9 and M12) are connected to the 1.0 V supply to mimic the behavior of M3 or M4 (whichever is “on”). The buffers driving the gates of M3 and M4 are supplied from the same supply. Fig. 8 is also showing some typical values for bias voltages.

## VI. TEST CHIP

The 12 bit DAC was built from a 6 bit thermometer-coded coarse DAC and a 6 bit binary-coded fine DAC (as shown in Fig. 2). The coarse DAC uses 63 DAC cells as depicted in Fig. 8. As mentioned before, although the layout of the coarse DAC was implemented with all the current sources in a straight line (as opposed to a matrix style layout), the decoding was implemented using column and row decoding using the circuit of Fig. 7, as this results in a effective decoding structure.

Two direct digital frequency synthesizers (DDFS) were integrated along with the DAC to enable two-tone testing. This avoids the problem of having to bring high-frequency digital signals onto the chip for test purposes. In the real application that is of course also not necessary because the digital signals to drive the DAC come from a dedicated digital signal processor (DSP).

## VII. MEASUREMENTS

The design was implemented in 65 nm CMOS technology and measures  $0.31 \text{ mm}^2$ . The layout is shown in Fig. 10. The power dissipation was 188 mW, combined from a 1.0 V

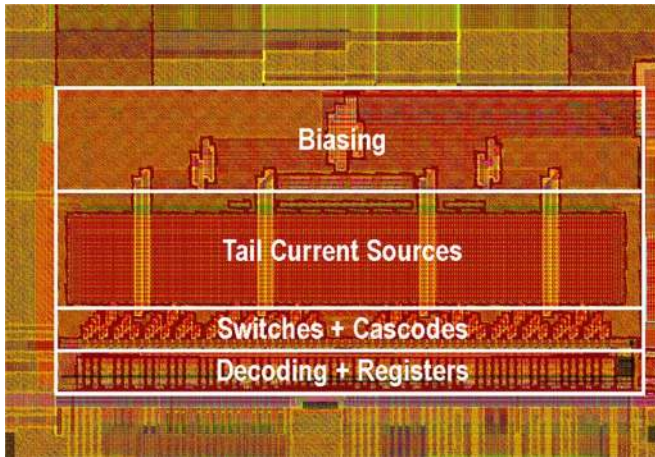


Fig. 10. DAC layout.

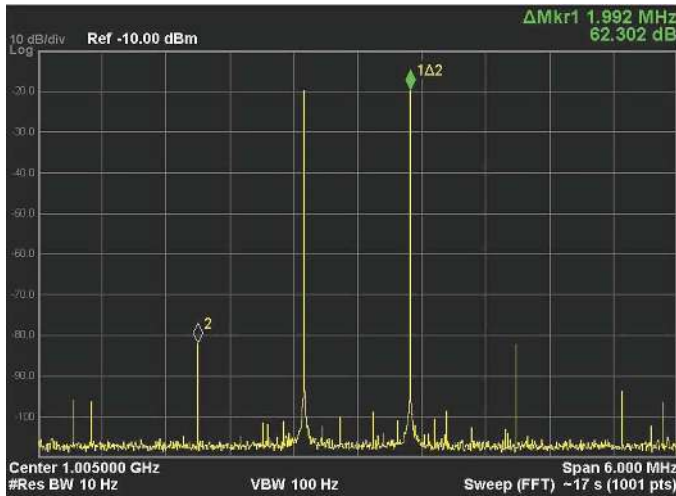


Fig. 11. Two-tone measurement centered around 1 GHz while sampling at 2.9 GS/s.

and 2.5 V supply. The measured INL and DNL were 0.51 sb and 0.31 sb, respectively, on a 12 bit level. All dynamic measurements were performed using the two on-board DDFSs. Although the circuit was designed for a 1.6 GS/s application, it ran with good performance up to 2.9 GS/s. Many of the measurements were performed at 2.9 GS/s, others at the speed of the application, 1.6 GS/s.

#### A. IM3 Measurements

Fig. 11 shows a spectrum of the output signal of a two-tone test centered at 1 GHz and sampling at 2.9 GS/s. As can be seen, the IM3 is better than  $-62$  dB. Many of those measurements were taken and Fig. 12 shows the measured IM3 results versus signal frequency, sampling at 2.9 GS/s. The figure shows a  $-70$  dB IM3 bandwidth of 550 MHz and a  $-60$  dB IM3 bandwidth of more than 1 GHz.

#### B. Comparison With Theory

In order to show the validity of the simple high-frequency distortion model discussed in Section IV-F, the output-impedance of the DAC cell, as shown in Fig. 8, was simulated, both for

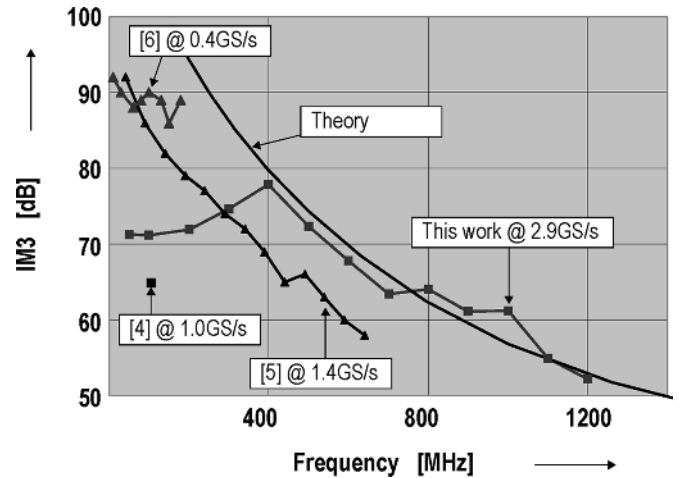
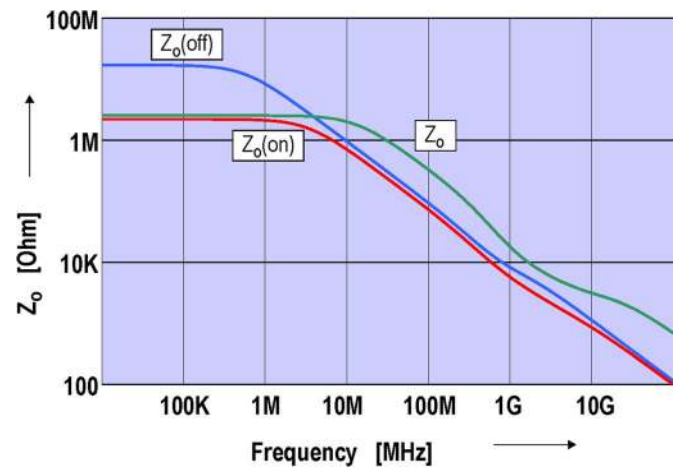


Fig. 12. Measured IM3 versus signal frequency. Note the differences in output swing and sampling frequency.

Fig. 13. Simulated output impedances  $Z_o$  (on) and  $Z_o$  (off) versus frequency. The switching impedance  $Z_o$  is calculated using (5).

the output that is “on” as well as for the output that is “off”. The results are shown in Fig. 13 as  $Z_o$  (on) and  $Z_o$  (off). An effective switching impedance  $Z_o$  was extracted using (5). By taking the imaginary part of  $Z_o$  we can make an estimate of the switching capacitance. Both the imaginary part of  $Z_o$  as well as the switching capacitance is shown in Fig. 14. For frequencies up to about 200 MHz the estimated switching capacitance is about 5 fF, after which the capacitance increases and peaks around 1.5 GHz at 9.5 fF. At a frequency of 600 MHz the value is about 6.5 fF, very close to what was needed for our goal of  $-70$  dB IM3 at that frequency.

Using the data from Fig. 14 in (5), with  $R_L = 50 \Omega$  and  $N = 64$ , an estimate was made of the IM3 for higher frequencies. This is shown in Fig. 12 as the curve labeled “Theory”. As can be seen, for higher frequencies ( $>400$  MHz) a very close match is obtained with the measured data, showing the validity of the theory. The IM3 at lower frequencies is clearly dominated by other effects, most likely a combination of matching errors, IR drops and transformer effects. The peaking observed around 400 MHz can be explained by a cancellation effect. The low-frequency distortion mechanism (mismatch, IR drops,

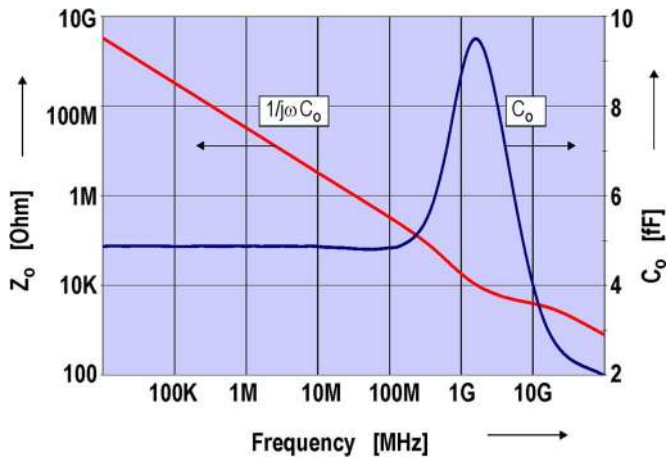


Fig. 14. Simulated imaginary part of the switching output impedance and the associated output capacitance  $C_o$  versus frequency.

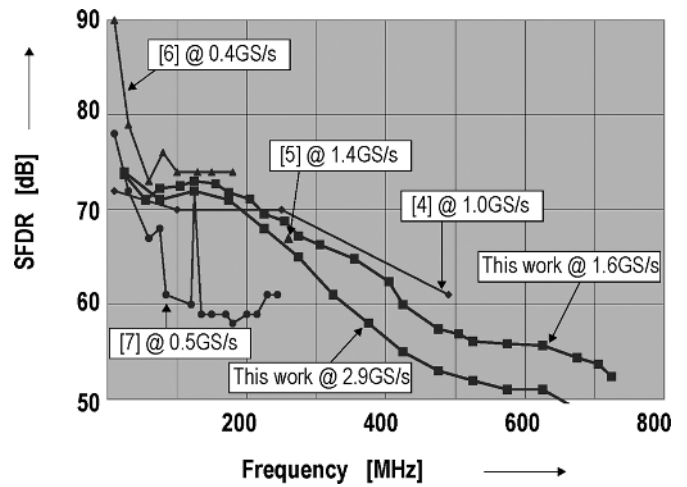


Fig. 16. Measured SFDR versus signal frequency. Note the differences in output swing and sampling frequency.

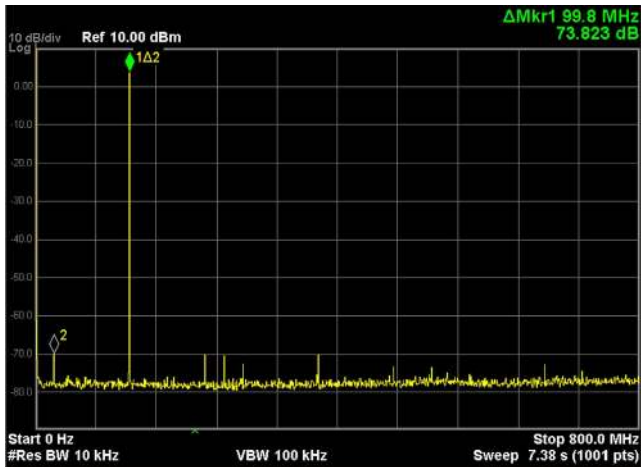


Fig. 15. SFDR measurement producing a tone at 125 MHz while sampling at 1.6 GS/s.

transformer) cancels with the high-frequency mechanism (finite output impedance).

### C. SFDR Measurements

SFDR was measured at 1.6 GS/s and 2.9 GS/s. A spectrum of the output signal measured at 1.6 GS/s and producing an output tone of 125 MHz is shown in Fig. 15. Many of those measurements were performed and Fig. 16 shows the results. It shows a 70 dB SFDR bandwidth of 225 MHz and a 60 dB SFDR bandwidth of 550 MHz. The SFDR results clearly show a lower bandwidth than the IM3 results. This is to be expected and can be explained as follows. In the first place, IM3 measurements only look at close-in third-order components, while SFDR measurements look at all the tones. Secondly, and more importantly, all measurements have been performed through a transformer (see Figs. 2 and 8), which has a bandwidth of about 300 MHz. This means that if the signal frequency is higher it gets attenuated. However, spurious tones which are folded back to lower frequencies (below the transformer bandwidth), do not get attenuated. This mechanism degrades the measured SFDR performance results significantly. The same mechanism has no effect on IM3 measurements, since the signal tones and the close-in

TABLE I  
COMPARISON WITH PUBLISHED DATA

Reference	Tech [nm]	F <sub>clk</sub> [GHz]	I <sub>load</sub> [mA]	Swing [V <sub>ppd</sub> ]	Power [mW]	NPE [%]
This work	65	2.9	50	2.5	188	66
[4]	350	1.0	16	0.8	110	12
[5]	180	1.4	30	1.5	200	23
[6]	250	0.4	20	1.0	400	5
[7]	180	0.5	15	0.75	216	5

tones are approximately at the same frequency and get the same attenuation.

### D. Comparison With Literature

Table I shows a comparison with published data [4]–[7]. Although all designs are driving a 50 Ω load, the available current varies significantly, from 15 mA [7] to 50 mA (this work). This results in equally significantly different signal swings. When comparing power dissipation, the available power for the load,  $P(R_{load})$  should be considered as well. A comparison of absolute power dissipation would make no sense. Here we use a normalized power efficiency (NPE) defined as

$$NPE = \frac{P_{peak}(R_{load})}{0.25 P_{supply}} \quad (6)$$

The factor 0.25 is used to allow the theoretical maximum of the NPE to be 100%. Note that the NPE varies significantly from design to design (5%–66%) and this work achieves the highest NPE.

The vast differences in maximum signal swing also have a strong influence on distortion performance. As is generally known, third-order distortion is proportional to the square of the signal amplitude. Fig. 12 also shows the results presented by [4]–[6]. Although the results presented here outperform the previously published results for frequencies above 300 MHz, the real difference is, as a result of the vast differences in signal



TABLE II  
PERFORMANCE OVERVIEW

CMOS	65nm
NOB	12
F <sub>clk</sub>	2.9 GS/s
I <sub>load</sub>	50 mA
Swing	2.5 V <sub>ppd</sub>
Power	188 mW
NPE	66 %
INL	0.5 lsb
DNL	0.3 lsb
70dB IM3 Bandwidth	550 MHz
60dB IM3 Bandwidth	1020 MHz
70dB SFDR Bandwidth	225 MHz
60dB SFDR Bandwidth	550 MHz

amplitude, much more pronounced. For IM3, the best results to which to compare are presented by [6], which are produced at an output swing of 1.5 V<sub>ppd</sub>, compared to 2.5 V<sub>ppd</sub> presented here. This results in an additional  $(2.5/1.5)^2 = 9$  dB difference in IM3 compared to [6], on top of the (approximately) 9 dB shown in the graph. Note that the results presented above are produced at a sampling speed of 2.9 GS/s, more than twice the sampling speed of the second best in Table I.

Fig. 16 shows the results of SFDR measurements of [4]–[7] and the results of this work. In this case the best results to use for comparison are presented by [4]. However, [4] shows an amplitude of 0.8 V<sub>ppd</sub>, compared to 2.5 V<sub>ppd</sub> presented here. The difference in amplitude is equivalent to an additional  $(2.5/0.8)^2 = 20$  dB in SFDR. Table II gives an overview of the measured performance of this work.

### VIII. CONCLUSION

A 12 bit 2.9 GS/s current-steering CMOS DAC was presented with a  $-70$  dB IM3 bandwidth of 550 MHz and a  $-60$  dB IM3 bandwidth of 1.0 GHz. These results were obtained while driving a 50  $\Omega$  load with 2.5 V<sub>ppd</sub> swing. The DAC presented combines the highest clock frequency (2.9 GS/s) with the highest output swing (2.5 V<sub>ppd</sub>) at the best power efficiency (66%), while simultaneously achieving the highest  $-60$  dB and  $-70$  dB IM3 bandwidth. The increase in performance at high frequencies compared to previously published results is mainly obtained by adding “always-on” cascodes on top of the current switches.

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**Chi-Hung Lin** was born in Keelung, Taiwan, in 1967. He received the B.S. degree in electrical engineering from National Taiwan University in 1989 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, in 1994 and 1998, respectively.

From 1989 to 1991, he served in the Chinese Army Missile Corps as a Maintenance Officer and was granted the best personnel award in 1991. From 1991 to 1994, he was involved in the study of CMOS device physics and reliability. In 1994, he joined Broadcom Corporation, where he has been involved in the research and development of high speed data converters and mixed signal IC design. He has been published in five ISSCC proceedings and holds 12 U.S. patents.

Dr. Lin was a co-recipient of the 2004 ISSCC Jan Van Vessel Award.



**Frank M. L. van der Goes** was born in Delft, The Netherlands, in 1966. He received the Ph.D. degree in electrical engineering from the Delft University of Technology in 1996.

From 1996 to 1999, he worked on analog signal processing circuitry for digital TV/radio receivers at Philips Research. He joined Broadcom as a staff scientist in the Analog and RF Microelectronics Department in 1999. He is currently a Senior Principle Scientist and is involved in analog electronics for communication applications.

Dr. van der Goes was a co-recipient of the Jan van Vessel Award for Best European Conference Paper in ISSCC 2004.



**Jan R. Westra** received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1993 and 1998, respectively.

From 1997 to 1999, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom Netherlands, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He is author of the book *Oscillators and Oscillator Systems—Classification, Analysis and Synthesis* (Kluwer Academic Publishers, 1999) and holds 14 U.S. patents in circuit design.

Dr. Westra was a co-recipient of the Jan van Vessel Award for Best European Conference Paper on ISSCC 2004.



**Jan Mulder** received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1994 and 1998, respectively.

From 1998 to 2000, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom Netherlands, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He has published over 50 papers in technical journals and conference proceedings. He holds 35 U.S. patents in circuit

design. He is the author of the book *Dynamic Translinear and Log-Domain Circuits* (Kluwer, 1999) and co-editor of the book *Research Perspectives on Dynamic Translinear and Log-Domain Circuits* (Kluwer, 2000).

Dr. Mulder was a co-recipient of the Jan van Vessel Award for Best European Conference Paper on ISSCC 2004.



**Yu Lin** was born in Chaozhou city, China, in 1980. He received the B.Sc. degree in electronics engineering from Dalian Maritime University, China, in 2003 and the M.Sc. degree in microelectronics from Delft University of Technology, The Netherlands in 2005. He is currently pursuing the Ph.D. degree in mixed-signal microelectronics at the Technische Universiteit Eindhoven, The Netherlands.

From 2006 to 2008, he worked at Broadcom Corporation, Bunnik, The Netherlands, as an analog IC designer. His main interests are in high speed and

high resolution data converters.



**Erol Arslan** received the Ing. degree from the Katholieke Industriële Hogeschool Antwerpen in Belgium in 1995.

He subsequently joined Alcatel, Antwerp, Belgium, where he worked on analog integrated circuits for ADSL and burst mode PON receivers. In 1998 he joined Xemics, Neuchatel, Switzerland, where he worked on low-power wireless transceivers. Later in 1999 he joined Sipex, Zaventem, Belgium, working on CMOS optical receivers and laser drivers for optical ethernet networks. After being a consultant

for a silicon-on-glass development in 2001 at Sarif, Vancouver, WA, he joined Broadcom, Bunnik, The Netherlands, in 2002 to work on ADC and DAC circuits. He is the author of two patents in the field of analog design.



**Emre Ayranci** was born in Izmir, Turkey, in 1981. He received the B.Sc. degree in microelectronics engineering from Sabanci University (SU), Istanbul, Turkey, in 2004 and the M.Sc. degree in electronics from Technical University of Denmark (DTU) in 2006.

From 2005 to 2007, he was an analog/mixed-signal IC designer in Intel Corporation, where he worked on PLL and CDRs in 10 Gb/s+ networking circuits. He was a research intern in the German Aerospace Center in 2003. Since 2007, he has been working

on high-speed data converters at Broadcom Corporation. He is the SSCS R8 GOLD representative and Benelux section PA and GOLD Chairman. He was the founder and chairman of DTU and SU student branches and Denmark student representative.

Mr. Ayranci received Garring scholarship in 2004 and SU Merit Scholarship in 1999. He is the recipient of the Best Paper Award in IEEE Denmark student paper contest (SPC) and an R8 SPC finalist.



**Xiaodong Liu** received the B.S. degree from Jilin University, Changchun, China, in 2002, and the M.Sc. degree from Delft University of Technology, Delft, The Netherlands, in 2005, both in electrical engineering.

He joined Broadcom as an Analog Design Engineer with Broadcom Netherlands in 2006. His field of interest is analog high-speed circuit design.



**Klaas Bult** received the M.Sc. degree in 1984 and the Ph.D. degree in 1988.

He joined Broadcom in 1996, after six years at Philips Research Labs and two years at UCLA. At Broadcom he started the Analog Design Group in Irvine, CA and later Broadcom's Design Center in Bunnik, The Netherlands. He is now Vice President and CTO of Operations and Central Engineering within Broadcom. He is also a Broadcom Fellow. He is an author of many international publications and holds more than 45 patents.

Dr. Bult received the Lewis Winner Award for Outstanding Conference Paper in ISSCC, 1990, 1992 and 1997, and the Jan van Vessel Award for Best European Conference Paper in ISSCC 2004.