A 12-bit 3.125 MHz Bandwidth 0–3 MASH Delta-Sigma Modulator

Ahmed Gharbiya, *Member, IEEE*, and David A. Johns, *Fellow, IEEE*

***Abstract*—We demonstrate a 12-bit 0–3 MASH delta-sigma modulator with a 3.125 MHz bandwidth in a 0.18 μm CMOS technology. The modulator has an oversampling ratio of 8 (clock frequency of 50 MHz) and achieves a peak SNDR of 73.9 dB (77.2 dB peak SNR) and consumes 24 mW from a 1.8 V supply. For comparison purposes, the modulator can be re-configured as a single-loop topology where a peak SNDR of 64.5 dB (66.3 dB peak SNR) is obtained with 22 mW power consumption. The energy required per conversion step for the 0–3 MASH architecture (0.95 pJ/step) is less than half of that required by the feedback topology (2.57 pJ/step).**

***Index Terms*—ADC, analog-to-digital conversion, delta-sigma modulation, MASH, multi-bit, multistage, oversampling.**

I. Introduction

DELTA-SIGMA ($\Delta\Sigma$) modulators are widely used for high-resolution and moderate-bandwidth analog-to-digital converters (ADC). In particular, the multi-stage topology (MASH) [1] is attractive for high-order low oversampling ratio (OSR) ADC. The popularity of MASH for low OSR stems from the improvement in the achievable Signal to Quantization-Noise Ratio (SQNR) when compared to single-loop topologies. The SQNR advantage is due to the enhanced stability which allows for a more aggressive design, and hence, a larger input-signal level in MASH structures. In previous implementations, cascades of $\Delta\Sigma$ ($\Delta\Sigma$ MASH) and cascades of $\Delta\Sigma$ followed by a zero-order quantizer ($\Delta\Sigma$-0 MASH, also known as the Leslie-Singh architecture [2]) have been reported. Examples of $\Delta\Sigma$ MASH include discrete-time implementations [3]–[5], a continuous-time implementation [6], and a hybrid continuous-time/discrete-time realization [7].

In this work, the missing piece of MASH topologies, the 0-$\Delta\Sigma$ MASH structure [8], [9], is demonstrated and analyzed in a 0.18 μm CMOS technology [10]. It is found that the 0-$\Delta\Sigma$ MASH is stable for a larger input-signal level than any traditional topology. The enhanced stability improves the achievable SQNR in the 0-$\Delta\Sigma$ MASH. A proof-of-concept 0–3 MASH prototype is fabricated to evaluate the concept and compare it to a third-order order single-loop feedback $\Delta\Sigma$ topology. The improved resolution and power efficiency of the 0-$\Delta\Sigma$ MASH topology are shown.

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The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, M5S 3G4 Canada (e-mail: a.gharbiya@utoronto.ca, johns@eecg.utoronto.ca).

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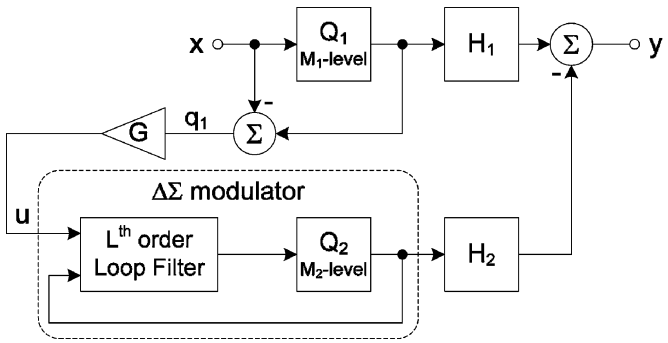

Fig. 1. The 0-L MASH $\Delta\Sigma$ modulator consists of a zero-order quantizer in the first-stage and an Lth order single-loop $\Delta\Sigma$ modulator in the second-stage in addition to digital filters H_1 and H_2.

The outline of this paper is as follows. Section II presents the concept of the 0-$\Delta\Sigma$ MASH architecture. Section III discusses practical implementation issues for the 0-$\Delta\Sigma$ MASH. Section IV illustrates the design of the 0–3 MASH. Section V summarizes the measured performance of the test-chip. Finally, conclusions are presented in Section VI.

II. 0-$\Delta\Sigma$ MASH Modulator

The 0-$\Delta\Sigma$ MASH concept is illustrated using a cascade of two stages (0-L) as shown in Fig. 1. The two stage example is used for simplicity but the results are nonetheless applicable to higher-order cascading. The first-stage is the zero-order quantizer with a reference voltage $V_{\mathrm{ref,Q1}}$. The second stage is an Lth order single-loop $\Delta\Sigma$ modulator with an internal quantizer having a reference voltage $V_{\mathrm{ref,Q2}}$. The reference voltages $V_{\mathrm{ref,Q1}}$ and $V_{\mathrm{ref,Q2}}$ can be different, however, they are limited by the supply voltage. In addition, there are two digital filters, H_1 and H_2, that process the digital code to generate the final output y from the 0-L MASH.

The first stage generates a quantization noise signal q_1 which is fed to a $\Delta\Sigma$ modulator in the second stage after an optional inter-stage gain G. Since the first-stage provides the signal q_1 to the $\Delta\Sigma$ modulator in the second stage, both stages operate at the same rate. Therefore, the first-stage is an oversampled zero-order quantizer. Linear analysis of the 0-L MASH, after replacing the quantizers with additive noise sources, leads to the following result:

$$y = H_1\, x - H_2\, \mathrm{NTF}_2\, q_2 + (H_1 - H_2\, G\, \mathrm{STF}_2)\; q_1 \qquad (1)$$

where STF_2 and NTF_2 are the signal transfer function (STF) and the noise transfer function (NTF) of the second stage respectively, and q_1 and q_2 are the quantization noise from the first and second stages respectively. The output from both stages is

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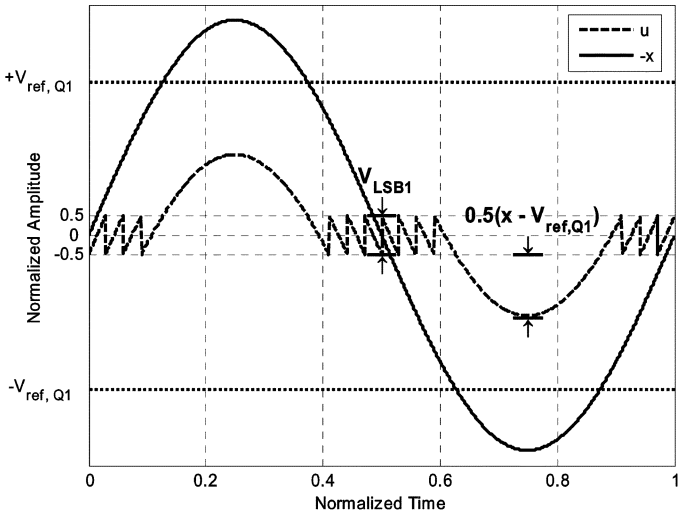

Fig. 2. A sample sinusoidal input-signal to the 0-L MASH and the input to the $\Delta\Sigma$ modulator in the second stage for 8 levels quantization in Q_1. As long as x is less than $V_{\mathrm{ref,Q1}}$, u is quantization noise only, once x exceeds $V_{\mathrm{ref,Q1}}$, u contains an input-signal component.

processed in the digital domain to obtain the final output y. By choosing H_1 to be $(G\,\mathrm{STF}_2)$ and H_2 to be the NTF of the first stage (which is one), the final output becomes

$$y = G\,\mathrm{STF}_2\,x - \mathrm{NTF}_2\,q_2. \tag{2}$$

Therefore, the quantization noise from the first stage is canceled at the output and q_2 is shaped by the NTF of the $\Delta\Sigma$ modulator in the second stage.

To understand the mechanism that leads to the enhanced performance of the 0-L MASH topology, consider the input to the second stage u as shown graphically in Fig. 2 for a sinusoidal input and 8 levels in Q_1 as an example. The signal u can be expressed mathematically as

$$u = \begin{cases} G\,q_1 & x < V_{\mathrm{ref,Q1}} \\ G\,\left(V_{\mathrm{LSB1}} + (x - V_{\mathrm{ref,Q1}})\right) & x \geq V_{\mathrm{ref,Q1}} \end{cases}. \tag{3}$$

In other words, as long as the input-signal is less than the reference voltage of the quantizer in the first stage $V_{\mathrm{ref,Q1}}$, the signal into the second-stage is the amplified quantization noise of the first-stage $(G\,q_1)$. Once the input-signal exceeds $V_{\mathrm{ref,Q1}}$, the signal into the second-stage includes a quantization noise component from the first-stage and an input-signal component. Since the first-quantizer is overloaded, it gives a fixed output equal to one LSB. Therefore, after the inter-stage gain, the quantization noise component of the second-stage input is $(G\,V_{LSB1})$. The signal component is the amount of input-signal above the range of the first quantizer $(x - V_{\mathrm{ref,Q1}})$. Therefore, after the inter-stage gain, the signal component of the second-stage input is $(G(x - V_{\mathrm{ref,Q1}}))$. The 0-L MASH is stable and operational after overloading Q_1 because there are no stability concerns for the zero-order first stage.

Two parameters of the 0-L MASH topology are derived next: the inter-stage gain range and the maximum stable input-signal level. To determine the inter-stage gain analytically, consider the maximum input into the second-stage of the 0-$\Delta\Sigma$ MASH which is given by

$$u_{\max} = k\,V_{\mathrm{ref,Q2}} \tag{4}$$

where k is a constant ranging from 50% to 80% [11] and depends on the loop order and the number of bits in the quantizer Q_2. Next, assuming Q_1 is not saturated, the output of the first stage amplified by the inter-stage gain is

$$u = G\,q_1. \tag{5}$$

The maximum value of q_1 under the non-saturation condition is one LSB as shown in Fig. 2. Thus, using (5), the maximum allowable input $u_{\max}$ into the $\Delta\Sigma$ modulator in the second stage is

$$u_{\max} = G\,V_{\mathrm{LSB1}} = G\,\frac{V_{\mathrm{ref,Q1}}}{M_1} \tag{6}$$

where M_1 is the number of levels in the first quantizer Q_1. From (4) and (6), the maximum inter-stage gain can be determined:

$$G \leq k\,\frac{V_{\mathrm{ref,Q2}}}{V_{\mathrm{ref,Q1}}}M_1. \tag{7}$$

If the inter-stage gain is set to less than its maximum value, the dynamic range of the second-stage $\Delta\Sigma$ modulator is not fully utilized. Therefore, the input-signal level can exceed $V_{\mathrm{ref,Q1}}$. In this case, only the second part of (3) is relevant where x is substituted by $x_{\max}$, the maximum input into the $\Delta\Sigma$ modulator is given by

$$\begin{aligned} u_{\max} &= G\,\left(V_{\mathrm{LSB1}} + (x_{\max} - V_{\mathrm{ref,Q1}})\right) \\ u_{\max} &= G\,\left(\frac{V_{\mathrm{ref,Q1}}}{M_1} + (x_{\max} - V_{\mathrm{ref,Q1}})\right). \end{aligned} \tag{8}$$

Substituting (4) into (8) and solving for $x_{\max}$, the maximum input-signal level can be determined:

$$x_{\max} = k\,\frac{V_{\mathrm{ref,Q2}}}{G} + V_{\mathrm{ref,Q1}}\left(1 - \frac{1}{M_1}\right). \tag{9}$$

Equation (9) holds as long as the inter-stage gain is bounded by (7).

The behavior of the 0-$\Delta\Sigma$ MASH topology is described by (7) and (9). To help better appreciate these equations, consider the 0–3 MASH modulator shown in Fig. 7 and described later in Section IV. System level simulations using MATLAB show that the third-order $\Delta\Sigma$ modulator achieves a maximum SQNR of 71 dB for an input level of -2 dBFS. For the 0–3 MASH topology with an inter-stage gain of one, the maximum SQNR improves to 82 dB for an input level of 9 dBFS. For an inter-stage gain of one for example, the 0–3 MASH tolerated an input-signal that is 3.5 times greater than the third-order feedback topology. As the inter-stage gain increases, the SQNR for a given input-level is improved and the maximum stable input level is decreased, thus, the dynamic range is maintained as shown in Fig. 3.

An additional advantage of the 0-L MASH is the low swing and low distortion characteristics of the $\Delta\Sigma$ modulator if the input is limited to $V_{\mathrm{ref,Q1}}$. If Q_1 is not overloaded, the input to

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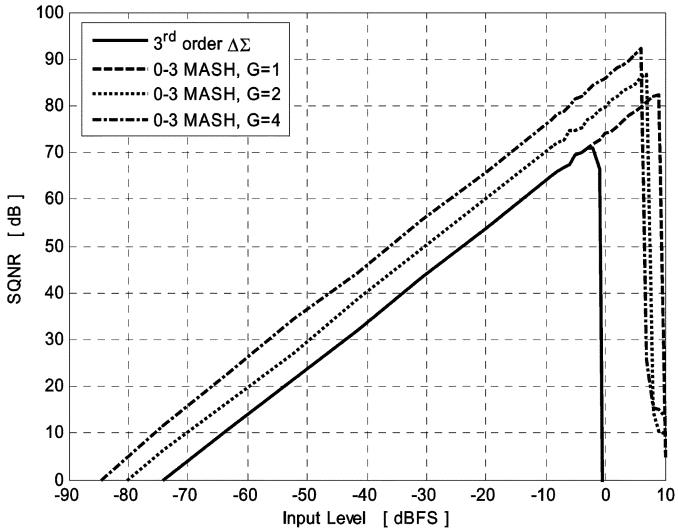

Fig. 3. System level simulations of the SQNR versus input-signal level for the third-order order feedback $\Delta\Sigma$ modulator and the 0–3 MASH shown in Fig. 7 with various inter-stage gains ($G = 1$, 2, and 4). For the 0–3 MASH, as the inter-stage gain increases, the SQNR for a given input-level is improved and the maximum stable input level is decreased.

the second stage is quantization noise only. Processing quantization noise reduces the swing at the internal nodes of the modulator which relaxes the headroom requirements, and allows for more efficient opamp architectures to be used. Moreover, distortion becomes independent of the input signal, which relaxes the linearity requirements. This advantage is similar to input-feedforward topologies where the loop filter only processes quantization noise [12]. In traditional MASH topologies, the first-stage $\Delta\Sigma$ modulator processes the signal in addition to quantization noise. On the other hand, the first-stage in the 0-$\Delta\Sigma$ MASH can be implemented as a flash ADC where opamp linearity and limited swing becomes less important.

III. Practical Considerations

This section analyzes some practical issues for the implementation of the 0-$\Delta\Sigma$ MASH modulator. First, the requirements of the first stage quantizer are explained. Second, the matching between the analog and digital domains is discussed. Third, the effect of timing skew between Q_1 and the analog signal path is studied. Finally, the options and tradeoffs for the realization of the adder in the first stage are analyzed.

The first-stage zero-order quantizer in the 0-$\Delta\Sigma$ MASH architecture contains an ADC and a digital-to-analog converter (DAC). The performance of the ADC is relaxed because any errors made by the ADC results in an error in q_1 (see Fig. 1). Since q_1 is cancelled at the output, the error made by the ADC is therefore eliminated. On the other hand, the DAC feeds the quantized signal directly into the input of the modulator. Therefore, the DAC performance is critical for the overall performance of the 0-$\Delta\Sigma$ MASH. The DAC has to be linear to at least the resolution of the 0-$\Delta\Sigma$ MASH; otherwise, it becomes the limiting factor in the achievable performance. The DAC also contributes thermal noise to the 0-$\Delta\Sigma$ MASH, in the same way the feedback DAC in the $\Delta\Sigma$ modulator contributes thermal noise since both are connected at the virtual ground of the first opamp. Therefore, thermal noise contribution from the DAC in the first-stage must be included in the noise budget. On the other hand, thermal noise at the first-stage ADC input only affects its performance. Since errors by the first ADC result in an error in q_1, which is canceled at the output, thermal noise in the ADC is less important.

The 0-$\Delta\Sigma$ MASH topology is a noise canceller; therefore, matching between the analog and the digital domains is required for the quantization noise from the first quantizer to be cancelled at the output. Matching can be achieved by the proper design of the analog circuits. Alternatively, digital circuits can be calibrated to match the analog ones, and hence maintain the relaxed requirements on the analog components [6], [13], [14]. In modern CMOS technology digital calibration is an effective way to achieve the matching.

To understand the effect of analog imperfections on the modulator behavior, consider the 0–3 MASH topology shown later in Fig. 7. If the opamp in the first integrator suffers from low open-loop gain (A), the transfer function of the integrator is modified as follows [15]:

$$\frac{v_o}{v_i} = \frac{(1-\varepsilon_\alpha)\ z^{-1}}{1-(1-\varepsilon_\theta)\ z^{-1}} \tag{10}$$

where $\varepsilon_\alpha \approx 1/(A\beta)$ is a gain error, $\varepsilon_\theta \approx 1/A$ is a phase error, and β is the integrator feedback factor. The STF of the third-order feedback modulator is modified to

$$\mathrm{STF} = \frac{(1-\varepsilon_\alpha)\ z^{-2}}{1+\varepsilon_\theta\ z^{-1}+(\varepsilon_\theta-\varepsilon_a)\ z^{-2}}. \tag{11}$$

Therefore, the digital filter H_1 must be modified to match the STF in order to achieve cancellation of the quantization noise from Q_1.

Fortunately, as we will see in Section IV, the analog specifications such as opamp gain and bandwidth as well as coefficient matching are quite reasonable for a 12-bit 0–3 MASH topology without the need of digital calibration.

Timing skew at the input of the 0-$\Delta\Sigma$ MASH is inevitable without adding a sample-and-hold circuit at the front-end. Therefore, understanding the timing skew effect is important. Analysis of the linearized system for the modulator shown in Fig. 4 with a delay of z^{-n} in Q_1, where n is the amount of latency relative to the sampling period, leads to the following result:

$$y = G\,\mathrm{STF}_2\,x - \mathrm{NTF}_2\,q_2. \tag{12}$$

In addition, the input to the $\Delta\Sigma$ modulator in the second stage is

$$u = -G\ \left(\left(1-z^{-n}\right)\ x - q_1\right). \tag{13}$$

Therefore, the transfer function of the 0-L MASH is not affected by latency in Q_1. The input of the $\Delta\Sigma$ modulator however, contains an input-signal component shaped by $(1-z^{-n})$ in addition to q_1. The shaped input-signal has an insignificant effect if the delay n is small. Therefore, the timing skew is not a critical issue even without a sample-and-hold at the front-end. In other words,

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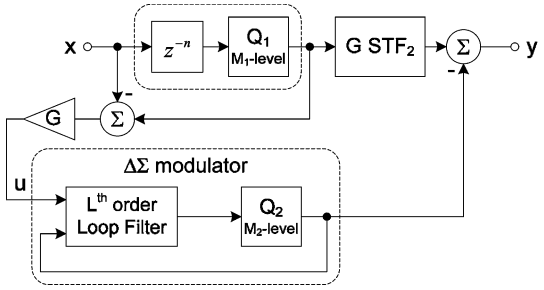

Fig. 4. The 0-L MASH with a delay of z^{-n} in the first quantizer Q_1.

errors made by the first stage affect u only. Since u is cancelled at the output, errors made by Q_1 are not critical.

A special and practical case of the latency is half a period $(n = 1/2)$. Utilizing the $z^{-1/2}$ delay in the quantizer path relaxes the timing requirements imposed on the first stage and allows more processing time for quantization, dynamic element matching (DEM) and DAC operations. It also suggests a method to map the 0-$\Delta\Sigma$ MASH topology into the continuous-time domain where delay is inevitable.

There are two possibilities for the implementation of the adder in the first stage. One option is to add the signals from ADC_1 and ADC_2 in the analog domain. To do so, two separate DACs connected to the virtual ground of the first integrator feed the output of the ADCs to the loop filter. The analog processing option is illustrated conceptually in Fig. 5(a). The second option is to add the signals from ADC_1 and ADC_2 in the digital domain and feed the sum back to the loop filter through a single DAC. The digital processing concept is illustrated conceptually in Fig. 5(b). The single DAC in Fig. 5(b) must have higher resolution than DAC_1 or DAC_2 in Fig. 5(a) to be able to handle the sum of the quantizers output. Adopting the digital option increases latency due to a more complex digital processing and DEM. On the other hand, the analog option is more sensitive to coefficient errors.

To understand the robustness of the single DAC implementation and the susceptibility of the two separate DACs to coefficient mismatch, consider the linearized first-order 0–1 MASH shown in Fig. 6 with inter-stage gain of one. Furthermore, assuming that DEM is utilized, each DAC element is used equally, therefore, the effective unit capacitor size is simply the average of all the unit elements. With an average error in the coefficients of the first DAC (ε_1) and the second DAC (ε_2), analysis of the modulator shows that the output signal contains

$$\frac{z^{-1}\left[\varepsilon_1 - z^{-1}\varepsilon_2\right]}{-\left(1 + z^{-1}\varepsilon_2\right)}\, q_1. \tag{14}$$

Therefore, mismatch between the DACs in the analog addition implementation results in quantization noise leakage to the output. On the other hand, if the addition is performed in the digital domain, the errors are equal $(\varepsilon_1 = \varepsilon_2 = \varepsilon)$ and the output signal contains

$$\frac{z^{-1}\varepsilon\left(1 - z^{-1}\right)}{-\left(1 + z^{-1}\varepsilon\right)}\, q_1. \tag{15}$$

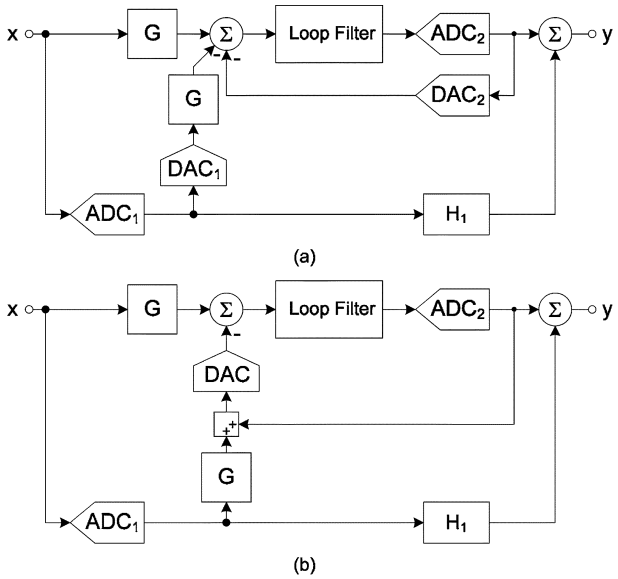

Fig. 5. Two possible implementations of the 0-L MASH front-end. (a) Analog addition uses two DACs to feed the outputs of the two quantizers to the loop filter. (b) Digital addition adds the outputs of the two quantizers in the digital domain and feeds the sum back through a single DAC. The first option is more sensitive to coefficient errors. The second option increases latency due to a more complex digital processing and DEM.

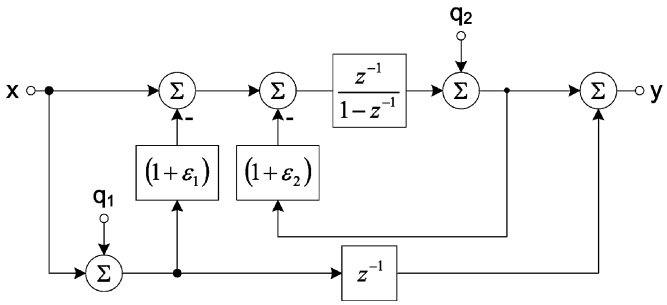

Fig. 6. Linearized 0–1 MASH modulator used to evaluate the effect of DAC coefficient errors for the single DAC and two DACs implementation.

The quantization noise leakage to the output is noise-shaped for the digital implementation. Therefore, the digital implementation has lower sensitivity to DAC coefficient errors. In other words, the single DAC implementation provides better matching between the analog and digital domains, thus reducing the effect of DAC coefficient errors.

For the implementation of the test-chip, the following choices are made. First, to obtain analog-digital matching, the analog circuits are designed to meet the quantization noise cancellation requirement without the need for digital calibration. Next, to deal with the timing requirement of the first-stage, the double-sampled input technique [16], [17] is used instead of the inherent delay approach presented in this section. Finally, the front-end summation is implemented using the two separate DACs approach.

IV. Design of the Experimental Modulator

The objective of the test chip is to build a re-configurable modulator that is capable of operating as either a 0-$\Delta\Sigma$ MASH

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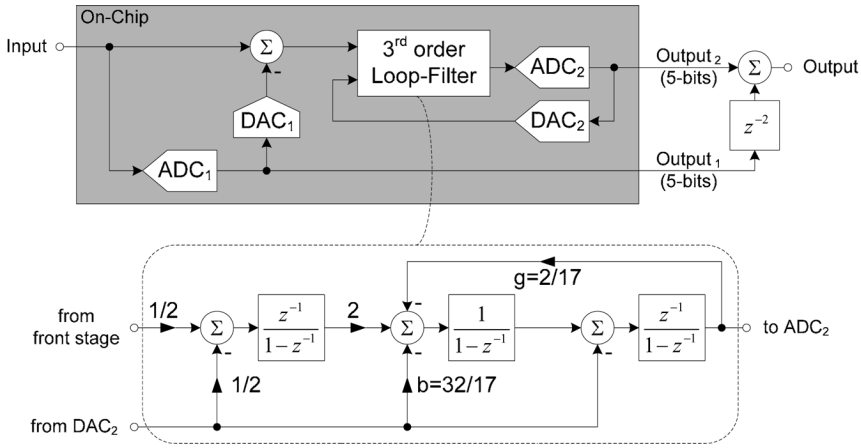

Fig. 7. System level of the experimental 0–3 MASH modulator. The first stage is a 17-level quantizer and the second stage is an optimized third-order feedback $\Delta\Sigma$ topology with 17-level internal quantizer.

or as a single-loop feedback $\Delta\Sigma$ modulator. The re-configurability feature facilitates evaluation of the proposed modulator and allows for a comparison with a traditional architecture.

A. System Level Design

The system level of the MASH modulator is shown in Fig. 7. The second stage is a third-order feedback $\Delta\Sigma$ topology with optimized NTF zeros. The feedback topology is chosen because it has an all-pass STF. The second stage uses a 17-level internal quantizer ADC_2 with reference voltage levels of $\pm 0.5\ \mathrm{V_{diff}}$ which is limited by opamp swing. In the first stage, ADC_1 also uses a 17-level quantizer but with reference voltage levels of $\pm 1.0\ \mathrm{V_{diff}}$. The same number of levels is used in the two quantizers to allow design reuse for the ADC. The inter-stage gain (G in Fig. 1) is chosen to be one to simplify the re-configurability of the modulator. The digital post processing (filters H_1 and H_2 in addition to an adder as shown in Fig. 1) is implemented in software off-chip. H_1 equals the STF of the modulator in the second stage, which is simply two unit delays. H_2 equals the NTF of the first stage, which is one.

The delta-sigma toolbox [18] is used to synthesize the optimized third-order NTF with maximum out-of-band gain and an OSR of 8. Next, dynamic range scaling is performed to optimize the signal range of the integrators. The coefficients are then approximated to allow the usage of a practical unit size capacitor. The approximation modifies the NTF and results in a 1.5 dB reduction of the achievable SQNR since the zeros are not in their optimum location. However, practical considerations justify the small reduction in the SQNR. Another factor that is considered in the approximation process is to maintain the sum of coefficients b and g equal to two (b and g are shown in Fig. 7). If the sum is not maintained, the STF of the $\Delta\Sigma$ modulator will change, as described by

$$\mathrm{STF} = \frac{z^{-2}}{1 + (b+g-2)\ z^{-1} - (b+g-2)\ z^{-2}}. \qquad (16)$$

The STF change will result in high frequency boost which is undesirable from a stability standpoint. In addition, since the digital filter must match the STF, it is more efficient for the digital filter to be simple delay elements instead of a more complicated filter.

The modulator is simulated in MATLAB taking into account the effects of finite gain and bandwidth in the opamps to determine the circuit design specifications [5]. From simulations, it is found that the opamp gain must be larger than 60 dB, and the closed-loop -3 dB bandwidth must be larger than twice the sampling frequency. The coefficient matching requirement for the 0–3 MASH is determined using a 100 points Monte Carlo simulation in MATLAB with normally distributed random mismatch. Simulations indicate that a 0.1% coefficient mismatch results in less than 1 dB degradation in SQNR. Since 0.1% capacitor matching is possible with a careful layout, the matching requirements are achievable with good reliability.

B. Structural Level Design

The system model in Fig. 7 is mapped into the equivalent switched-capacitor circuit as shown in Fig. 8 in the single-ended form for simplicity (the actual implementation is fully differential). NMOS switches are used wherever the gate-source voltage is fixed. Bootstrapped switches [19], [20] are used for all the floating switches at the input of the integrators. Finally, transmission gates are used for the remaining switches.

The analog addition (two separate DACs) is chosen at the front-end to keep the configurability feature simple and because the desired resolution is moderate. Since linearity of the two DACs feeding into the first integrator is important to ensure the performance of the modulator, data weighted averaging (DWA) [21] is used for both front-end DACs. However, linearity is less important for the DACs in the second and third integrators since nonlinearities are noise shaped when referred back to the input. Therefore, DWA was omitted from the second integrator to allow more time for the operation of the DWA block.

The first integrator uses the double sampled input technique [16], [17] to mitigate the timing constraint introduced at the input of the 0-$\Delta\Sigma$ MASH topology. The constraint is due to the delay free path from the input through ADC_1, DWA_1, and DAC_1 to the integrator input as shown in Fig. 8. The front-end sampling capacitor is 1 pF to achieve the desired resolution of

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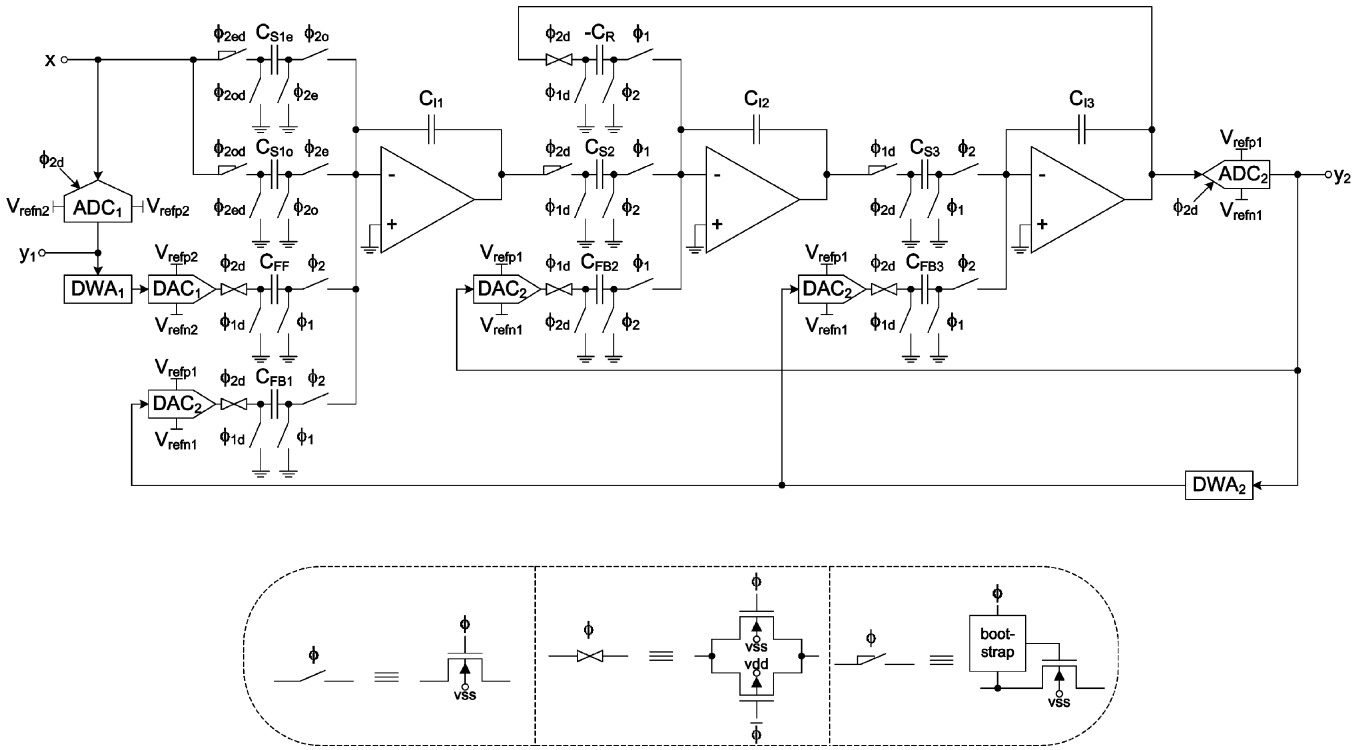

Fig. 8. $\Delta\Sigma$ modulator structural level shows the switched-capacitor circuit implementation of the 0–3 MASH.

12 bits for the 0–3 MASH topology. The capacitors in the following stages of the modulator are scaled down since their noise contribution is negligible in the noise-budget.

The quantizers are latched at the falling edge of the delayed phase 2, while the sampling capacitors sample their signal at the falling edge of phase 2. This clocking arrangement introduces a small skew at the input, which is insignificant for the operation of the modulator as discussed in Section III. It is done to ensure that any kickback from ADC_1 does not affect the sampled input-signal.

The modulator in Fig. 8 can operate in single-loop feedback mode by simply turning off ADC_1, DWA_1, and DAC_1. Furthermore, the feedforward capacitor from the first to the second stage C_{FF} (as shown in Fig. 8) is not switched in single-loop mode to eliminate its noise contribution to the modulator.

C. Circuit Level Design

The next step is to implement each of the building blocks at the transistor level. The telescopic opamp architecture was chosen for implementation and is shown in Fig. 9. Telescopic opamps with NMOS inputs have the advantage of high-speed operation because of the all NMOS signal path. The output common-mode voltage is set using a typical switched-capacitor common-mode feedback circuit where the control voltage vcm is fed back to the tail transistor. The DC gain from the telescopic opamp is not sufficient to achieve the analog-digital matching required for noise cancellation, therefore, gain boosters are used to enhance the opamps gain. All the biasing voltages for the opamps and their gain boosters are generated using typical wide-swing cascode current mirrors. The bias voltage for the NMOS cascode gain booster however, is generated as shown in Fig. 9. This biasing scheme improves the common-mode rejection.

The quantizers ADC_1 and ADC_2 are implemented as 17-level flash. Each ADC has 16 parallel comparators and each comparator is a cascade of a preamplifier, regenerative latch, and RS latch. The total input capacitance of the flash is 0.24 pF which is about one-fourth the input sampling capacitor (1 pF). Therefore, the extra load at the input due to ADC_1 is small.

The preamplifier, shown in Fig. 10, compares the differential input and differential reference and amplifies the difference. The difference is then processed by the dynamic regenerative latch shown in Fig. 10 [22]. The gain of the preamplifier is important to reduce the offset and kick-back from the regenerative latch. The latch is reset when ϕ_{2d} is low, therefore, a simple RS-latch is used to hold the output of the dynamic latch for the remainder of the period.

V. Measured Performance

The $\Delta\Sigma$ modulator is implemented in a 0.18 μm one-poly six-metal (1P6M) CMOS process with the MIM capacitor option. The active area is 1.8 mm^2 as shown in Fig. 11. The die is packaged in a 44-pin CQFP package.

The measured performance of the $\Delta\Sigma$ modulator is summarized in Table I. The improvement in the performance of the MASH modulator is reflected in its figure of merit (FOM) which is less than half of that achieved by the feedback topology. Decimation filters are not implemented in the test-chip, therefore, their power consumption is not included for either configuration. Furthermore, the digital post processing components, two unit-delay elements and an adder, are implemented in software and their power consumption is not included for the 0–3 MASH.

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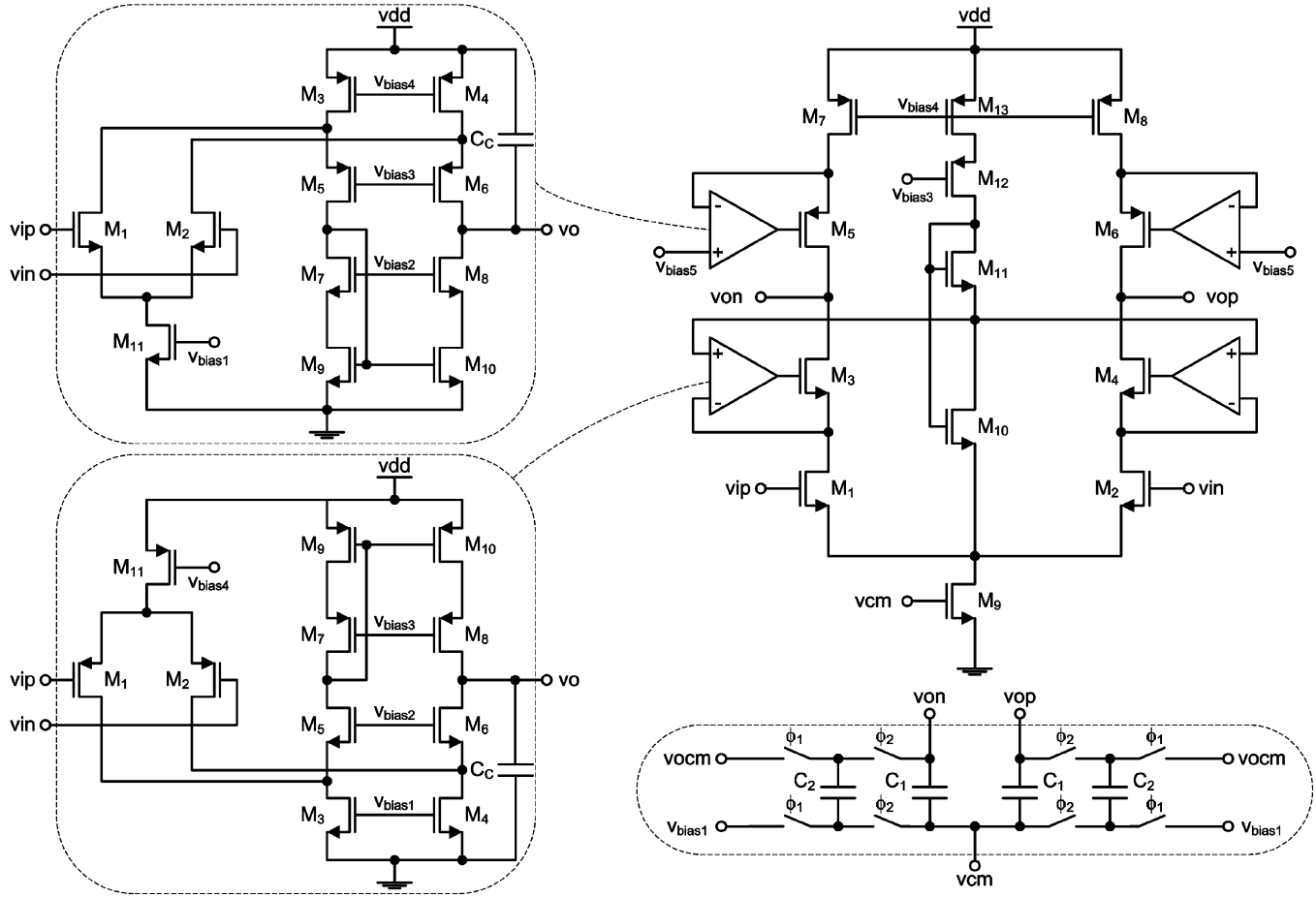

Fig. 9. Gain-boosted telescopic opamp using a switched capacitor common-mode feedback circuit.

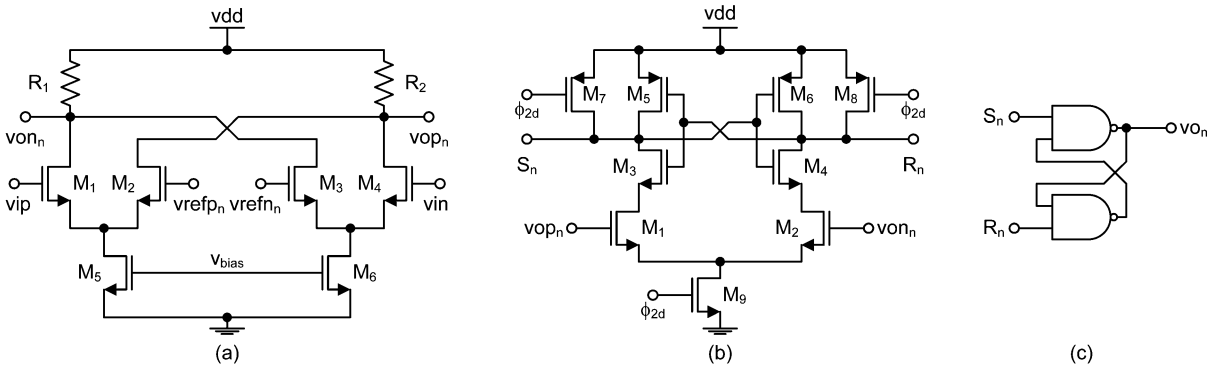

Fig. 10. Each comparator in the flash ADC contains a cascade of three stages: (a) differential difference preamplifier (b) dynamic regenerative latch (c) RS latch.

The main advantage of the 0-$\Delta\Sigma$ MASH topology is allowing a larger input-signal which results in an improvement in the achievable SNR and SNDR as illustrated in Fig. 12. The input-signal is expressed in dBFS where dBFS is decibel with respect to the full-scale. The full-scale is defined to be the reference voltage of the second-stage $(\pm 0.5\ \mathrm{V_{diff}})$ for both the 0–3 MASH and the feedback modulator. The full-scale for the 0–3 MASH can be defined differently. For example, the first stage reference $\pm(1.0\ \mathrm{V_{diff}})$. However, the definition of the full-scale does not affect the SNR/SNDR performance achieved by each modulator. At -3 dBFS, the traditional feedback modulator achieves its peak SNDR of 64.5 dB (66.3 dB peak SNR) and overloads soon after. The 0–3 MASH achieves a peak SNDR of 73.9 dB (77.2 dB peak SNR) at an input-level of 8 dBFS.

The output spectrum for the two configurations at their maximum SNDR is shown in Fig. 13. The input frequency is at 780 kHz and with amplitude of -3 dBFS for the feedback modulator and 8 dBFS for the 0-$\Delta\Sigma$ MASH modulator.

The internal nodes of the 0–3 MASH modulator contain quantization noise only before overloading the first quantizer. Although this feature is difficult to measure for all three opamps in the modulator, it can be confirmed for the third

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TABLE I
SUMMARY OF THE MEASURED PERFORMANCE

	0-3 MASH	Feedback ΔΣ
Supply	1.8 V	
$f_{sampling}$	50 MHz	
OSR	8	
BW_{signal}	3.125 MHz	
Analog Power	19 mW	18 mW
Digital Power	5 mW	4 mW
Total Power	24 mW	22 mW
Peak SNR	77.2 dB	66.3 dB
Peak SNDR	73.9 dB	64.5 dB
FOM*	0.95 pJ/step	2.57 pJ/step

*FOM=Power/(2BW_{signal} 2^((SNDR-1.76)/6.02))

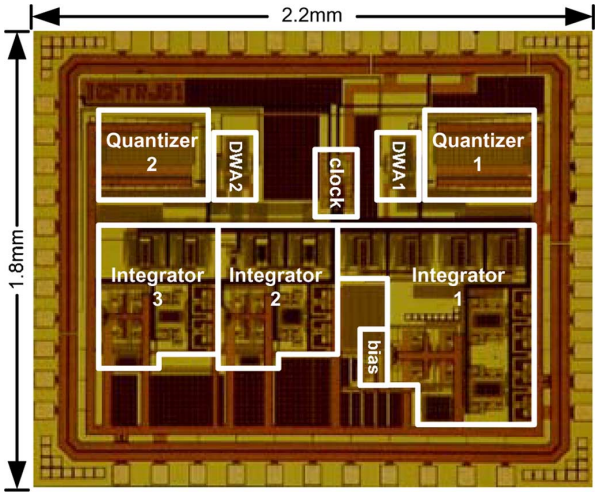

Fig. 11. Micrograph of prototype fabricated in a 0.18 μm 1P6M CMOS process.

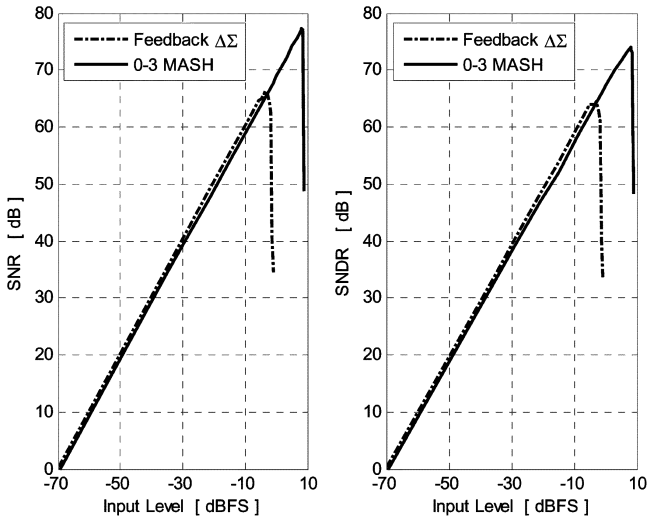

Fig. 12. Measured SNR and SNDR versus input-signal level.

opamp. This is because the third opamp output is quantized and processed off-chip, therefore, its distribution can be analyzed.

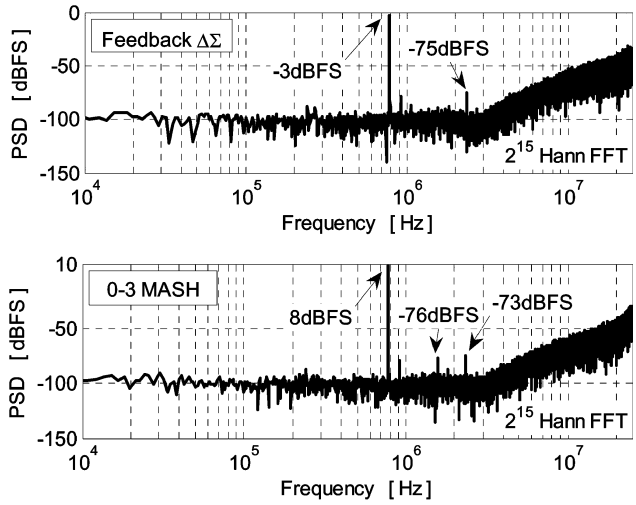

Fig. 13. Sample output spectrum at peak SNDR for the feedback and the 0–3 MASH ΔΣ modulators.

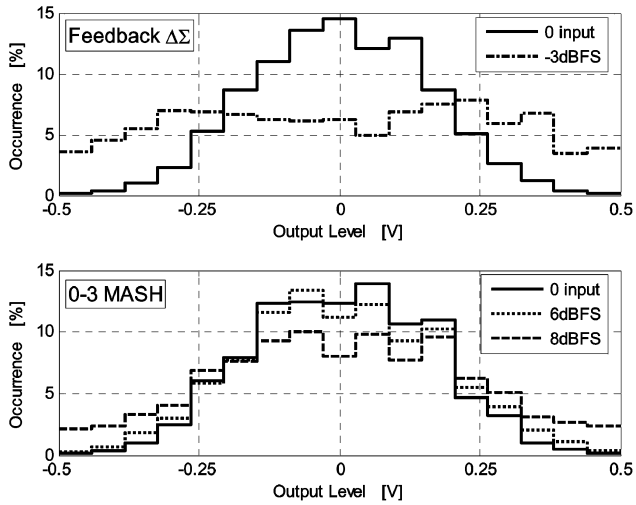

Fig. 14. Measured output level distribution.

By confirming the output of the third opamp, we can deduce the validity of the quantization noise only feature for the other opamps.

The 17-level outputs of the third opamp are shown in Fig. 14. For a zero input-signal, the outputs from both configurations are normally distributed since the input is thermal noise. The 0–3 MASH topology maintains a similar distribution up to 6 dBFS (the maximum point before ADC_1 overloads). However, at an input of -3 dBFS (the maximum SNDR point for the feedback modulator), the feedback modulator distribution shows more occurrences at the reference limit, which indicates that the modulator is getting closer to overloading. At 8 dBFS, the 0–3 MASH shows more occurrences at the reference limit. The increase in occurrences is not as large as the feedback topology, however, its impact on stability is as significant. This is because the 0–3 MASH spends most of the time processing quantization noise and large-signals appear when the input level exceeds $V_{\mathrm{ref,Q1}}$.

The 0–3 MASH performance can be compared to a recent ΔΣ-0 MASH modulator implemented in a 0.18 μm 1P6M

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CMOS process with similar resolution [23]. The first stage is a second-order feedback topology with a 4-bit internal quantizer and the second stage is a 9-bit pipeline ADC. The modulator is clocked at 80 MHz with an OSR of 4 and achieves a peak SNDR of 73 dB while consuming 240 mW, therefore, it has a FOM of 3.29 pJ/step.

VI. Conclusion

The concept of the 0-$\Delta\Sigma$ MASH architecture was presented and analyzed. The main advantage of the 0-$\Delta\Sigma$ MASH topology is allowing a larger input-signal which results in an improvement in the achievable performance and an enhancement in the modulator efficiency. In addition, its ability to process quantization noise only, relaxes the headroom and linearity requirements of the opamps.

A configurable $\Delta\Sigma$ modulator is implemented in a 0.18 μm CMOS technology to evaluate the 0-$\Delta\Sigma$ MASH concept and compare it to the single-loop feedback modulator. Both topologies are tested at 50 MHz with an OSR of 8 and powered from a 1.8 V supply. The 0–3 MASH modulator achieves 77.2 dB peak SNR (73.9 dB peak SNDR) which is 10.9 dB (9.4 dB) better than the feedback modulator at the expense of 9% increase in power consumption. The energy required per conversion step for the 0–3 MASH architecture is 37% of that required by the feedback architecture.

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Ahmed Gharbiya (S'99–M'08) received the B.E. degree from Dalhousie University, NS, Canada, in 1999, the M.A.Sc. degree from Simon Fraser University, BC, Canada, in 2002, and the Ph.D. degree from the University of Toronto, ON, Canada, in 2008.

In 2008, he joined MaxLinear Inc., Carlsbad, CA, where he has been involved with the development of low-power mixed-signal integrated circuits.

David A. Johns (S'81–M'89–SM'94–F'01) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Toronto, ON, Canada, in 1980, 1983 and 1989, respectively.

In 1988, he began working at the University of Toronto, where he is currently a full Professor. He has ongoing research programs in the general area of analog integrated circuits. His research work has resulted in more than 80 publications as well as the 1999 IEEE Darlington Award. Together with academic experience, he also has spent a number of years in the semiconductor industry and was a co-founder of a successful IP company called Snowbush Microelectronics.

Prof. Johns has served as a guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and an associate editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and was a member of the SSCS Adcom from 2002 to 2008. His homepage is http://www.eecg.toronto.edu/~johns.

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