# A 12 Bit Third Order Continuous Time Low Pass Sigma Delta Modulator for Audio Applications

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**Abstract**
We present design considerations for low pass sigma delta modulators for audio applications. A third order system is chosen to establish stable operation over 24KHz Signal Bandwidth with an Oversampling Ratio of 64 and a sampling frequency of 3.72 M Hz. A binary quantizer is used to maintain linearity in the modulator. Behavioural Modeling of the system shows signal-to-noise-and-distortion-ratio (SNDR) of 84.8 dB and Dynamic Range of 81dB. A CIFB topology is used and design is implemented in 0.25 micron CMOS Technology.

**Keywords**
Data Converters, Sigma Delta modulation, Oversampling, Noise Shaping

## I. Introduction

The emergence of powerful digital signal processing for telecommunication and multimedia applications implemented in CMOS VLSI technology creates the need for high-resolution analog-to-digital converters that can be integrated in fabrication technologies optimized for digital circuits and systems. Based on the sampling frequency the ADC is of two types-Nyquist Rate Converters and Oversampling Converters. The oversampling converters are preferred for low bandwidth applications such as audio and instrumentation because they provide inherently high resolution when coupled with proper noise shaping to push noise out of signal band and thus increase SNR. Oversampling ADCs can be divided into two categories based on the point in the signal chain where sampling takes place: Discrete-time (DT), which are built using switched-capacitor filters and continuous-time (CT), which, are implemented using continuous-time filters. CT sigma-delta ADCs are becoming more popular than DT ADCs primarily because of inherent anti aliasing filter, reduced settling time and Low Power consumption. Power reduction is a key motivator for using CT-Delta Sigma Modulator (DSM) for digitizing low-frequency analog signals [1]. Several implementations targeting audio range have been reported recently where a single bit quantizer is used [2-4].

In this paper, we describe the design of a 12-bit CT-DSM for audio applications. Implemented in a 0.25 micron CMOS technology, the modulator runs on a 2.5 V supply and achieves a SNDR of 84.8dB and dynamic range of 81dB for a signal bandwidth of 24 KHz. The modulator operates with an oversampling ratio (OSR) of 64 and a sampling frequency of 3.072 MHz.

The paper is organized as follows-Section II describes the basic principles of SD ADC and basic mathematical analysis is dealt with, elaborately. In section III a detailed Behavioral Model is presented that is based on Loop Filter design using ABCD parameters and a third order DSM is modeled in simulink. In section IV, the subsystem design of the DSM is described, providing transistor level design and circuit simulations of Two stage CMOS OPAMP, Comparator, Adder, D flip flop and DAC. The complete design of third order system and its sinusoidal response is presented in section V. The conclusion and future work is discussed in section VI.

## II. Principles of Sigma Delta ADC

The process of sampling and quantization is standard approach for conversion of analog signals to digital. Normally sampling is performed at nyquist rate i.e. at fs=2fm and then quantization is done. The quantizer being a non linear device will introduce a quantization noise. The SQNR (Signal to Quantization Noise) of such an ADC for an N bit quantizer with a sine wave input is modeled as follows

SQNR= 6.02N + 1.76 dB (1)

This is commonly known as the 6-dB rule for delta modulation. In SDADC, effort is made to reduce the quantization noise by sampling the signal very closely. Sampling is done at a much higher rate than the nyquist rate (fs>>2fm) and OSR = fs/2fm. This is typically between 16-512 times the nyquist rate and hence is suitable for audio applications. It improves the SQNR by a great amount as shown below.

SQNR = 6.02N + 10 Log (OSR) +1.76 dB (2)

The performance is improved more by doing noise shaping by introducing a loop filter wherein the quantization error is moved out to the filter stop band, thus reducing the in band noise, thus increasing the SQNR as shown in fig 1. Further, the SQNR can be increased by increasing the order of the modulator to get a sharp cutoff [3]. The effect of noise shaping is clear from the following equation wherin L stands for the order of the filter.

SQNR=6.02N+ 10(2L+1)Log (OSR)+1.76dB (3)

Higher order modulators will lead to instability of the circuit and hence a feedback path is introduced to keep the system stable. It is here we observe that a difference and summation (loop filter) is being performed together and hence the name Sigma Delta ADC.

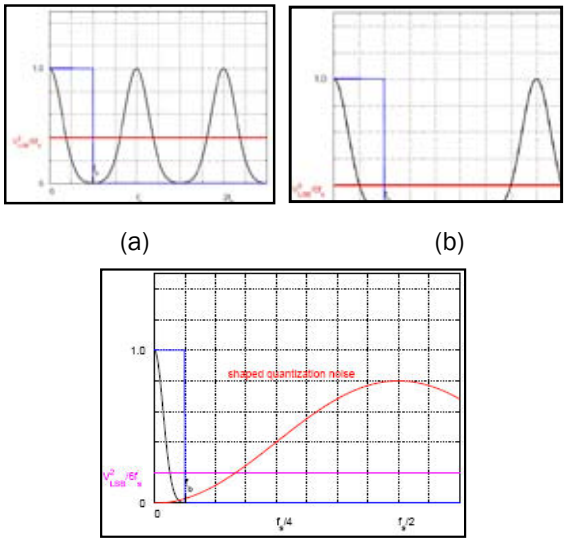



Fig. 1: (a). SQNR for Nyquist Rate ADC (b). SQNR with Oversampling (c). SQNR with Oversampling and Noise shaping

A simple block diagram of a first order sigma-delta modulator is shown in fig. 2, in which the quantizer is modeled as a source of additive noise.

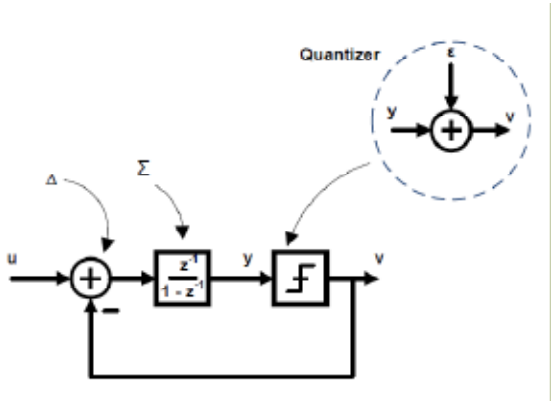



Fig. 2: First Order Sigma Delta Modulator

The model in fig. 2, is of a linear system with 2 inputs and 1 output. The output can hence be expressed as,

$$v = STF.u + NTF.\varepsilon \quad (4)$$

where, STF and NTF refer to the signal transfer function and noise transfer function respectively and are given by,

$$STF = \frac{V(z)}{U(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \quad (5)$$

$$NTF = \frac{V(z)}{E(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \quad (6)$$

As seen in equations (5) & (6), the signal and quantization noise have different transfer functions to the output. While the signal appears unchanged at the output with just a delay, the noise is differentiated and shaped such that it is pushed out of signal band.

In the above example, NTF of a first order transfer function is shown. We can obtain further improvements in resolution by using higher orders of noise shaping. Using an L th order modulator, the NTF will get modified as shown in (7).

$$NTF = (1 - z^{-1})^L \quad (7)$$

The SQNR will improve at the rate of (L+0.5) bits/octave of oversampling in the case of an Lth order sigma-delta modulator. In this paper design a third order SDADC i.e. of L=3 is discussed.

## III. Behavioral Model of SDADC

In the last decade, sigma-delta modulators were primarily discrete-time in nature and hence were implemented using switched-capacitor techniques. Only in the recent past, with the push towards higher bandwidths together with higher power efficiency, have continuous-time modulators become more prominent. Because of the wide usage of switched-capacitor modulators, design methodologies for DT modulators have been very well studied and many tools geared for the same have also been developed, e.g. the ΔΣ MATLAB toolbox by Richard Schreier [6]. In this paper, sigma-delta toolbox is used to extract the modulator coefficients using ABCD parameters.

### A. Design Considerations

The target in this paper is to realize a continuous-time sigma-delta low-pass modulator with the specifications shown in Table 1.

Table 1: Design Specifications

| Performance Parameter | Targeted Specifications |
|---|---|
| Order | 3 |
| Bandwidth | 24 KHz |
| Resolution | 12 bits |

Based on extensive simulations in MATLAB using the ΣΔ toolbox, the values in Table 2, were arrived at, to obtain the best SQNR performance.

Table 2: Noise Transfer Function Parameters

| Parameter | Value |
|---|---|
| OSR | 64 |
| Order | 3 |
| Number of levels in Quantizer | 2 |
| $NTF_{max}$ | 1.5 |
| SQNR | 84.8 dB |

The NTF used in the design is obtained using MATLAB as shown in fig. 3.

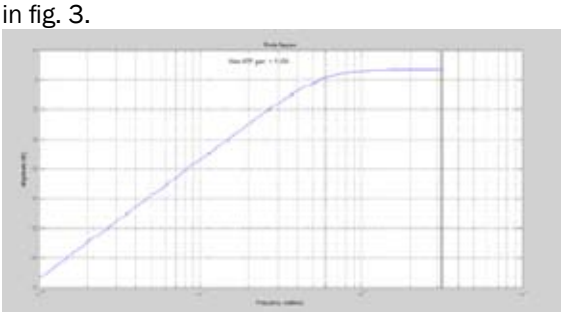


Fig. 3: Noise Transfer Function

A plot of the SQNR of the discrete-time system as a function of the input amplitude is shown in fig. 4. From the fig. we can see that the modulator can provide a maximum SQNR of 84.8dB at input amplitude of -3dBFS.

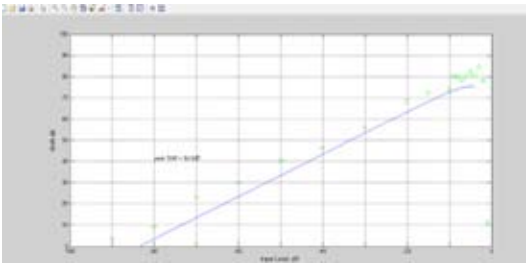


Fig. 4: SNR vs Input Amplitude

### B. Loop Filter Design

Once the NTF is known, the Loop filter that implements this NTF has to be designed. Initially the topology is decided. This paper implements the sigma-delta modulator using CIFB (Cascade-of-integrators, feedback form) topology as shown in fig. 3. The loop filter is described in the state space model by an ABCD matrix which is a conglomeration of four matrices namely matrix A, B, C and D. For single-quantizer systems, the loop filter is a two-input, one-output linear system and ABCD is an (n1x n+2) matrix, partitioned into A (nxn), B (nx2), C (1xn) and D (1x2) sub-matrices as shown in eqn. 1

$$ABCD = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (1)$$

Matrix A is of the order n and describes interconnections within the loop filter. The matrix B describes how the input u(n) and feedback output v(n) are applied to the loop filter. Matrices C and D describe how the output of the loop filter y(n) is computed from x(n), u(n) and v(n).The equations for updating the state and computing the output of the loop filter are

$$x(n+1) = Ax(n) + B\begin{bmatrix} u(n) \\ v(n) \end{bmatrix} \quad (2)$$

$$y(n) = Cx(n) + D\begin{bmatrix} u(n) \\ v(n) \end{bmatrix} \quad (3)$$

This formulation is sufficiently general to encompass all single-quantizer modulators which employ linear loop filters [8]. The sigma-delta toolbox supports translation to/from an ABCD description and coefficients for CIFF (Cascade-of-integrators feed forward form. In a Continuous Time modulator the integrator block will be replaced with 1/s

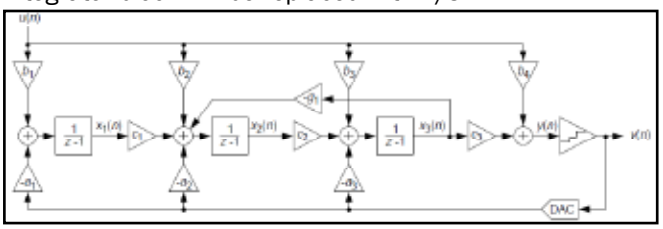



Fig. 5: CIFB structure for third order modulator

The ABCD matrix obtained is shown in eqn. 4. and the state space representation is for 3rd order modulator is shown in eqn. 5

$$ABCD = \begin{bmatrix} 0 & 0 & 0 & 0.044 & -0.044 \\ 1 & 0 & 0 & 0 & -0.2442 \\ 0 & 1 & 0 & 0 & -0.6703 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} x_1(n+1) \\ x_2(n+1) \\ x_3(n+1) \\ y(n) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & b_1 & -a_1 \\ c_1 & 0 & 0 & 0 & -a_2 \\ 0 & c_2 & 0 & 0 & -a_3 \\ 0 & 0 & c_3 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1(n) \\ x_2(n) \\ x_3(n) \\ u(n) \\ v(n) \end{bmatrix} \quad (5)$$

Comparing the first matrix on RHS with the ABCD matrix obtained from sigma-delta toolbox, we get

$$b_1 = 0.044, a_1 = -0.044, a_2 = 0.2442, a_3 = 0.6703, c_1 = c_2 = c_3 = 1$$

These coefficients are used in the detailed design of the sub-modules i.e. summing/differencing blocks at each stage. The ideal simulations of the sigma-delta modulator can be carried out using MATLAB Simulink. The Simulink model for the third order modulator is shown in fig. 6, and its input output waveforms u(t), and v(t) are shown in fig. 7. The loop filter coefficients obtained from ABCD matrix are used in the following model.

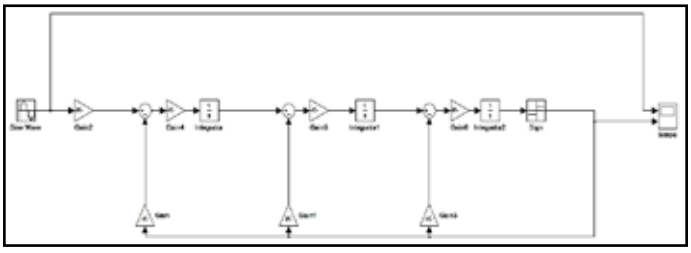


Fig. 6: Simulink Model for 3rd Order ∑Δ modulator

It can be observed that the output waveform has levels +1 and -1. When the input signal is positive the output waveform shows large number of +1 levels and when the input is negative output waveform shows large number of -1 levels and for input close to zero the output waveform has equal number of +1 and -1 levels which cancel out when a moving average is taken to give result as zero.

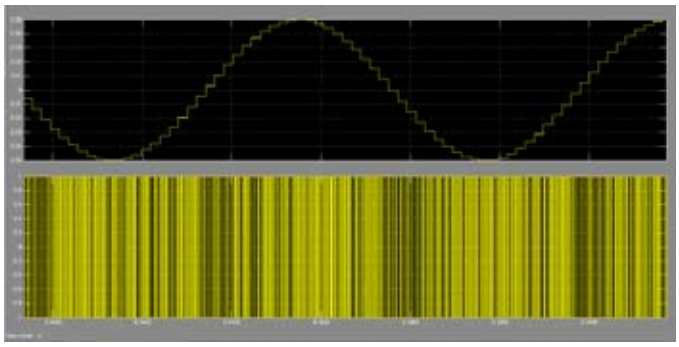


Fig. 7: Modulator Input and Output Waveforms

## IV. Subsystem Design

As seen in fig. 6, the various blocks of a delta sigma modulator are summer, integrator, comparator and DAC. The basic building block of all these modules is the Operation Amplifier. A Two Stage CMOS Op Amp is selected as it provides sufficient gain required by the ADC and is simple to design and is used to drive a resistive load.

### A. Design of Two Stage CMOS Op Amp

Two-stage circuit architecture has historically been the most popular approach for both bipolar and CMOS op-amps, where a complementary process that has reasonable n-type and p-type devices is available. When properly designed, the two-stage op-amp has a performance very close to more modern designs and is somewhat more suitable when resistive loads need to be driven. A block diagram of the typical two stage op-amp is shown in the fig. 8, "Two stages" refer to the number of gain stages in the op-amp. Fig. 8, actually shows three stages–two gain stages and one unity gain output stage. The output buffer is normally present only when resistive loads need to be driven. If the load is purely capacitive, then it is not included. The first gain stage is a differential input single ended output stage. The second gain stage is normally a common source gain stage that has an active load. Capacitor $C_c$ is included to ensure stability when the op-amp is used with feedback. Because $C_c$ is between the input and the output of the high gain second stage, it is often called a Miller capacitance since its effective capacitance load on the first stage is larger than its physical value. It should be noted that the first stage has a p-channel differential input pair with an n-channel current mirror active load.

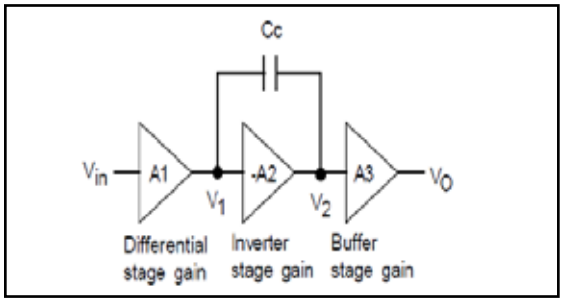



Fig. 8: Op-amp General Block Diagram

The op amp has been designed with the following specifications

Table 3: OP AMP Design Specifications

| Parameter | Value |
|---|---|
| Supply Voltages | $V_{DD}$ = + 2.5V, $V_{SS}$ = -2.5V |
| Open-loop gain | 15000 (84db) |
| Unity Gain Frequency ($w_{GB}$) | $2\pi \times 5 \times 10^6$ (5 MHz) |
| Slew Rate, SR | 10 V/µSec |
| Output Resistance, Ro | 1.5KΩ |
| Common Mode input Range | -2V to 1.5V |
| Phase Margin | > 60° |
| Technology Size | 0.25 Micrometer |

The transistor version of the two stage CMOS Op Amp is shown in the fig. 9.There are total 10 transistors in the design and using the above design values and standard design equations [7] the size of each transistor is calculated. The design is implemented in 0.25µm CMOS technology. For each transistor length is taken as 1µm and width is calculated according to the W/L ratio. The Table 4, summarizes W/L ratios for each transistor

Table 4. Design Summary of Op Amp

| Parameter | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | M10 |
|---|---|---|---|---|---|---|---|---|---|---|
| I (µA) | 5 | 5 | 5 | 5 | 10 | 15 | 15 | 50 | 50 | 50 |
| Type | P | P | N | N | P | N | P | P | P | P |
| W/L | 2.54 | 2.54 | 1 | 1 | 5.1 | 3 | 7.2 | 70.5 | 25.4 | 25.4 |
| L (µm) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $L_{effective}$ | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 |
| W (µm) | 2.125 | 2.125 | 0.875 | 0.875 | 4.125 | 4.125 | 5.875 | 57 | 21 | 21 |

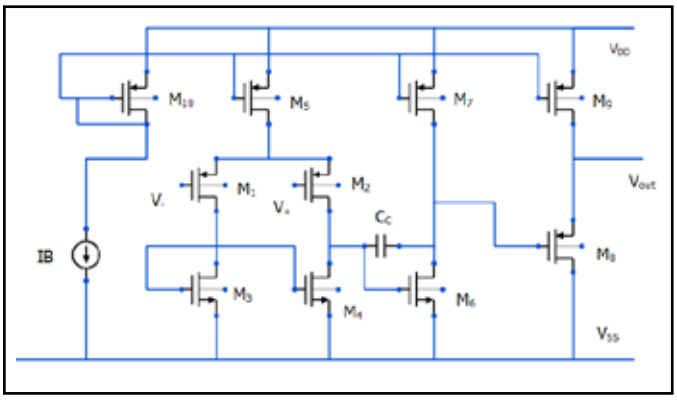



Fig. 9: Transistor version of Op-Amp

The output of the Op Amp is summarized by obtaining the gain and phase Plot through AC Analysis over a range of 0 Hz to 10MHz. The response is shown in fig. 9, It can be seen that, the gain of the Op-Amp becomes 0 dB much before the -180 degrees point. The compensation was designed for a Phase Margin of 60 degrees but a practical Phase Margin of 50 degrees is achieved. Results also show a maximum gain of 70 dB, Unity gain frequency = 6MHz and a Slew Rate of 5.65 is achieved.

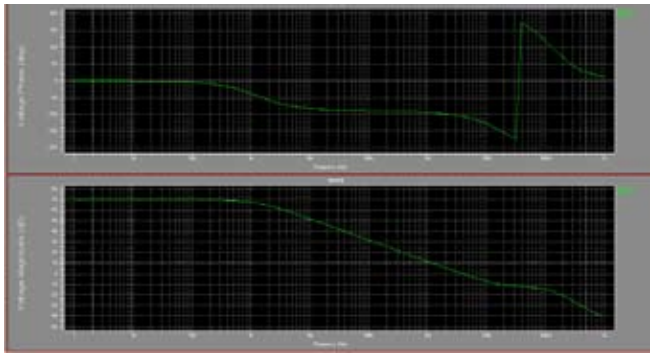


Fig. 10: Magnitude and Phase plot of Op-Amp

### B. CMOS Comparator Design

A comparator is a device which compares two voltages or currents and switches its output to indicate which is larger. A comparator is a circuit that has binary output. Ideally its output is defined as follows:

$$V_o = \begin{cases} V_{OH} \text{ if } V_{in+} - V_{in-} > 0 \\ V_{OL} \text{ if } V_{in+} - V_{in-} < 0 \end{cases}$$

In the current paper, a 10mV signal must be resolved using the comparator. The power supply rails are $V_{DD}$=2.5V and $V_{SS}$=-2.5V. That is, the output will swing by 5V ( from –2.5V to 2.5V) when the input signal swing by 10mV( from –5mV to 5mV). The comparator gain must be at least 10,000.

Table 5: Comparator Design specifications

| Parameter | Desired value |
|---|---|
| Supply Voltages | $V_{DD}$=2.5V and $V_{SS}$=-2.5V |
| Comparator Gain | 10000 |
| Common Mode input Range | -1.5V to 1.5V |
| Slew Rate, SR | 10V/µSec |
| Output voltage Swing | -2.25 V to 2.25 V |

The transistor version of the CMOS comparator implemented with PMOS input drivers and input biasing resistor is as shown in fig. 11.

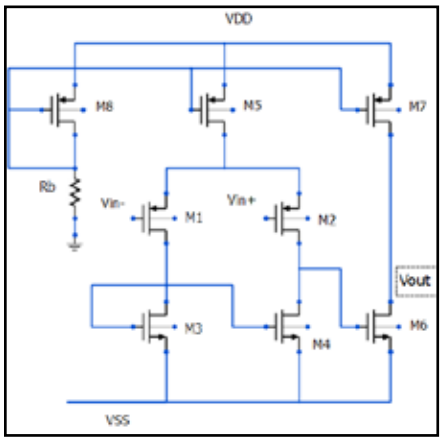



Fig. 11: Circuit Diagram of CMOS comparator

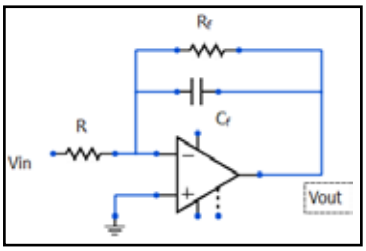
There are 8 transistors and one resistor in the comparator design and using the above design values and standard design equations the size of each transistor is calculated.

Table 6: Comparator Design Summary

| Parameter | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 |
|---|---|---|---|---|---|---|---|---|
| I (μA) | 5.5 | 5.5 | 5.5 | 5.5 | 11 | 20 | 20 | 20 |
| Type | P | P | N | N | P | N | P | P |
| W/L | 2 | 2 | 1 | 1 | 8 | 3.6 | 10.15 | 10.15 |
| L (μm) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $L_{eff}$ (μm) | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 |
| W (μm) | 1.625 | 1.625 | 0.875 | 0.875 | 6.5 | 3 | 8.125 | 8.125 |

### C. Integrator Design

A simple op-amp based integrator which will be used in the loop filter of the modulator is shown in fig. 12. The design of Integrator is done with unity gain frequency is $f_a$=3.072 M Hz and 3dB frequency is $f_b$=30.72 M Hz.

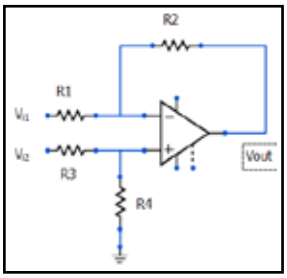



**Designed Values:**
C = 1 PF
R=5.18KOhms
$R_f$=51.8 KOhms

Fig. 12: Circuit Diagram of Integrator

### D. Summer Design

The summer is a very important block of SD ADC as its design is purely dependent on the filter coefficients extracted using MATLAB. For a third order modulator three summers as required, all of them will have the same circuit as shown in fig. 13.




| Stage | I | II | III |
|---|---|---|---|
| Coeff | 0.044 | 0.2442 | 0.6703 |
| R1 | 50k | 10k | 10k |
| R2 | 2.2k | 2.5k | 6.67k |
| R3 | 50K | 10k | 10k |
| R4 | 2.2K | 40k | 15k |

Fig. 13: Circuit Diagram of Summer block with Resistance values

### E. D Flip Flop

In order to clock the Non return-to-zero (NRZ) output of the comparator to a RZ output, a D flip-flop is added after the comparator. Fig. 14, shows the schematic design of the D flip-flop [5].

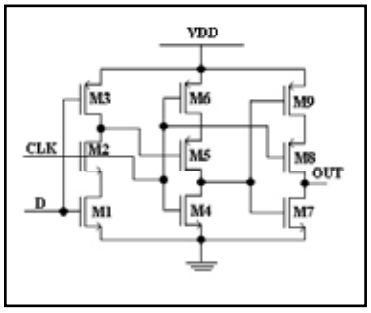



Fig. 14: Circuit Diagram of D Flip Flop

### F. One Bit DAC

The most important component of feeback path is the 1 bit DAC that converts the output digital bit stream to analog value based on a reference voltage [9]. The DAC is a simple multiplexer based design in which if the input(output of modulator) is logic 1 a voltage of +Vref/2 is fed back and if the input is logic 0 a voltage of–Vref/2 is fed back to the summer of first stage.

## V. System Design of Third order Delta Sigma Modulator

The sub blocks designed in step IV are combined to form the CIFB structure of third order modulator as shown in fig. 15 below.

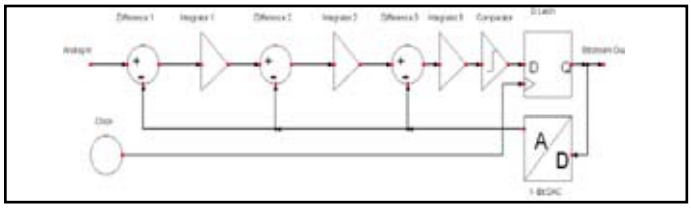



Fig. 15: Block Diagram of 3rd Order Sigma Delta Modulator

The clock signal is provided to the D flip flop which converts the Bipolar output of the comparator to unipolar. The third order modulator is simulated by giving a sinusoidal input of 50mV peak value, 50mV offset voltage and frequency 20KHz and a sampling clock signal of frequency 3.072MHz is used. The output of the modulator as shown in fig 5.2 contains more number of ones when the input approaches 100mV and more number of zeroes when the input approaches zero [10].

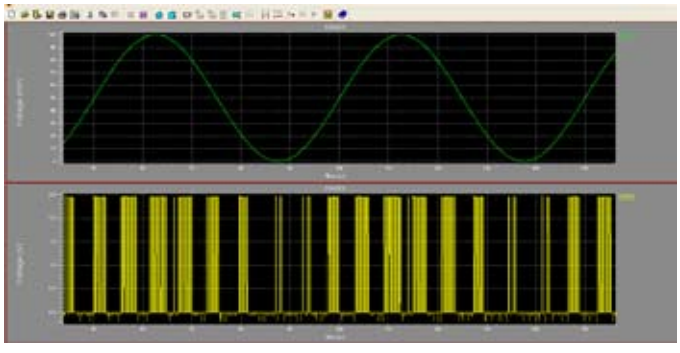


Fig. 16: Response of 3rd order SDADC to sinusoidal input

The output bitstream is analysed by obtaining FFT and plotting the spectrum. We clearly see the impulse at 20 KHz in fig. 17. The plot of SNR as a function of input amplitude is shown in fig. 18, It can be seen from this plot that peak SNR of 84.1dB is achieved with a dynamic range of 81 dB. If 10% degradation is assumed in the SNR then this modulator provides a resolution of 12 bits.

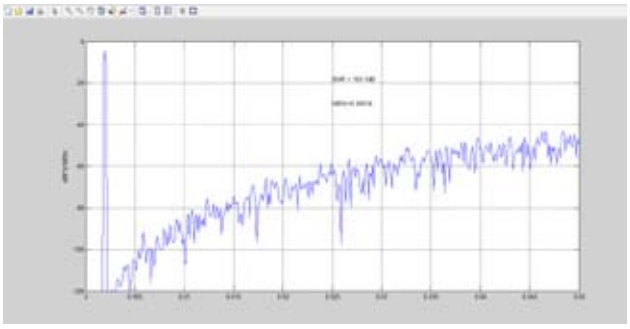


Fig. 17: Output versus normalized frequency plot

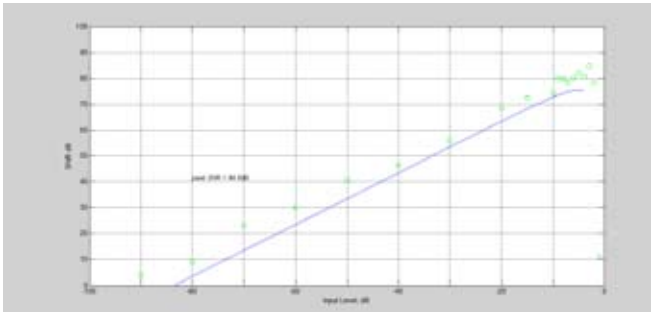


Fig. 18: SNR versus Input plot

## VI. Conclusion and Future Scope

A third order continuous time sigma delta modulator is designed in 0.25 micron CMOS. It targets low pass signals for audio frequency range at a signal bandwidth of 24 K Hz with an Oversampling Ratio of 64 and a sampling frequency of 3.072 MHz. A signal to noise ratio of 84.1 dB is achieved which provides a 12 bit resolution. The design of a modulator is proposed in this paper that provides a single output bit stream. This bit stream has to be converted into 12 bit digital data by passing through a decimation filter. The future work aims at designing this decimation filter which is purely a digital FIR filter and is essentially a moving average filter. A complete ADC is a sigma delta modulator followed by a decimation filter integrated on a single chip. Even though the SDADC provides High Resolution it is plagued by inherent delay in the output path. This Excess loop delay (ELD) can be cancelled using various delay cancellation techniques.

## References

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