A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13µm CMOS Technology

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Abstract

A novel 12-bit Vernier ring time-to-digital converter (TDC) with 8ps of time resolution for digital-phase-locked-loop applications is presented. The TDC achieves a large detectable range of 32ns. The core of the TDC occupies 0.75 x 0.35 mm^2 in a 0.13um CMOS technology. The total power consumption for the entire TDC chip is only 7.5mW with a 1.5V power supply at a sample rate of 15MSps.

Introduction

Time-to-digital converter (TDC) is a critical building block for digital-phase-locked-loop (DPLL) designs. An inverter-chain based TDC was implemented in the first DPLL for a blue-tooth radio application [1]. Recently several topologies have been explored to shrink the TDC time resolution to several picoseconds. A time amplifier based TDC greatly improves the resolution and detectable range by amplifying the time residue left in a coarse TDC before quantizing it using a fine TDC [2]. A gated ring oscillator based TDC was reported with a time resolution of 6ps, detectable range of 11-bit and up to 21mW power consumption [3]. The Vernier delay line based TDC is well known for its fine time resolution, yet it struggles with the efficiency in measuring large time intervals. In this paper, a *Vernier ring TDC* (VRTDC) is presented for the first time that leverages the time difference between two rings of delay cells to achieve a fine time resolution of 8ps and a large detectable range up to 12 bits. We propose a novel TDC architecture that places the Vernier delay cells in a ring format such that the delay chains can be reused for measuring large time intervals. Proper logics are designed to monitor the number of laps the signals propagate along the rings. Arbiters are used to record the location where the lag signal catches up the lead signal. The reuse of Vernier delay cells in a ring configuration achieves fine resolution and large detectable range simultaneously with small area and low power consumption.

Circuit Implementation

The proposed 12-bit VRTDC chip is composed of a VRTDC core, a pre-logic, a control logic, a thermometer decoder, a 6-bit fine counter (N_F) and a 6-bit coarse counter (N_C). Fig. 1 illustrates the concept of the proposed VRTDC. Two rings of inverters with slightly different delays are used to quantize the input time interval. The VRTDC consists of two chains of arbiters, which operate in odd laps and even laps, respectively. Two types of arbiters are placed alternatively along the rings to compare the rising and falling edges, respectively. The VRTDC core consists of a fast ring with smaller delay, a slow ring with larger delay and 30 arbiters as shown in Fig. 2. Each ring has 15 stages of inverters with delays adjustable by external bias voltages.

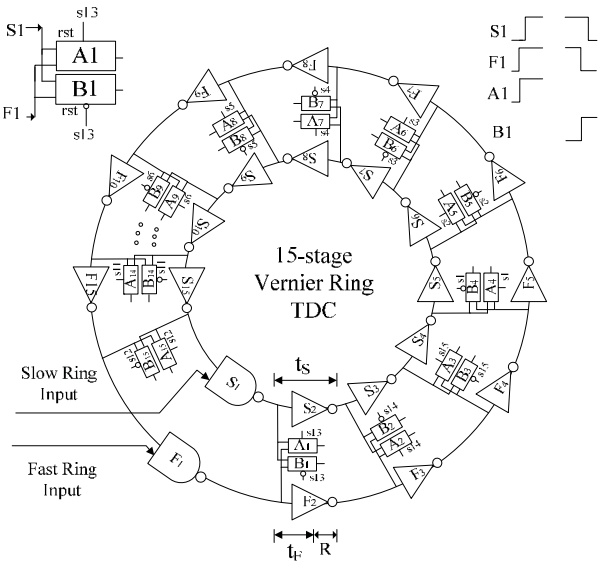

Fig. 1 Block diagram of the VRTDC core with 15 stages.

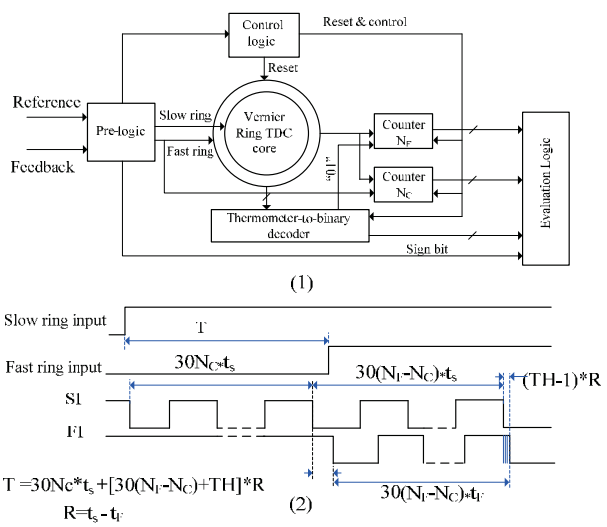

Fig. 2 (1) VRTDC architecture and (2) illustration of timing diagram.

The reference signal and the oscillator feedback signal in a DPLL are fed into the pre-logic cell, where an arbiter judges whether the reference leads the feedback or vice versa, which determines the sign bit of the TDC output. As shown in Fig. 3(1), the lead signal is steered to the slow ring by the output of the arbiter, while the lag signal is fed to the fast ring. The lag signal chases the lead signal along the ring and eventually passes it after a certain amount of propagation. The propagation delays of the inverters in the fast and slow rings are set to t_F and t_S, respectively. Thus the time resolution of the TDC is given by $R=t_S-t_F$. Fig. 3(2) shows the schematics of two types of arbiters. Arbiter *A* and *B* are triggered by rising

and falling edges, respectively. They are reset every other lap. The edge detector in both of arbiters outputs a negative pulse to set the arbiters and then release the control to the reset signals. The arbiter outputs *0* when the signal in the slow ring arrives first, namely, the lag signal has not caught up the lead signal yet. The arbiter outputs *1* when the signal in the fast ring arrives first, namely, the lag signal catches up the lead signal. The first transition from zero to one at the arbiter output will be detected and used to latch the fine counter. The outputs of 30 arbiters are combined to output a 30-bit thermometer code *TH*, which are translated into 5-bit binary code by a thermometer decoder. *TH* records the location (number of delay cells) where the lag signal passes the lead signal. The fine counter (N_F) records the number of laps that the lead signal has propagated before the lag signal catches up the lead signal. The coarse counter (N_C) records the number of laps that the lead signal has propagated when the lag signal arrives at the input of the TDC. Therefore the total amount of delay N consists of three elements: N_C, N_F and the thermometer code TH. The TDC output is thus given by,

$$N = \pm 30(N_F - N_C) + TH + 30N_C t_S / R \qquad (1)$$

where the polarity of N, the sign bit of TDC output, is determined by the pre-logic as described above.

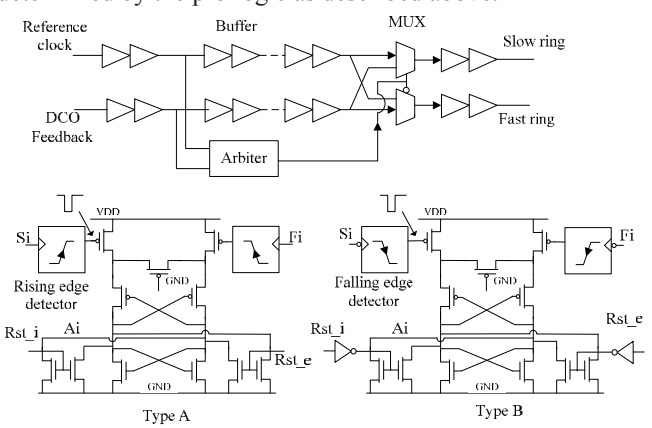

Fig. 3 Simplified circuits of (1) pre-logic unit and (2) arbiters.

Measurement

Fig. 4 (left) shows the TDC output measured with two inputs that has a fixed phase difference of 2.05ns plus a sinusoidally time-varying phase difference of 20ps peak-to-peak. Sixty sequentially measured output codes were averaged to obtain the TDC output in the time domain. The measured TDC output correctly follows the input sinusoidal phase sweep when the time resolution was set to 10.2ps. Fig. 4 (right) demonstrates that the TDC works well at a time resolution of 7.6ps, which was achieved by adjusting the delay difference between two rings. Two input signals with 2Hz frequency difference at 15MHz are applied to generate a ramp of time interval for the measurement of the TDC transfer curve, INL and DNL. The slope of the transfer curve indicates an average measured time resolution of 8ps. The measured time resolution of 8ps was limited by the available test equipment and test setup. Noise coupling from PCB/power supply and the frequency variation of the signal generators can affect the TDC test. The simulated TDC performance achieves better than 2ps resolution. Fig. 5 shows the measured TDC output after a median filter with 30x averaging. Fig. 6 gives the measured code distribution with a constant input time interval. It indicates that the standard deviation of the TDC output is less than 1-LSB under 256000 tests. The core of the TDC circuit occupies 0.75 x 0.35 mm^2. The entire TDC chip consumes 7.5mW from a 1.5V power supply while operating at 15 MSps.

References

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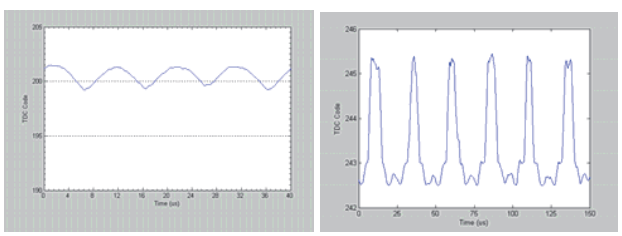


Fig. 4 Measured TDC output with sinusoidal delay sweep 20 ps(p-p), (left) 100kHz with 2.05ns fixed delay and (right) 40kHz with 1.95ns fixed delay.

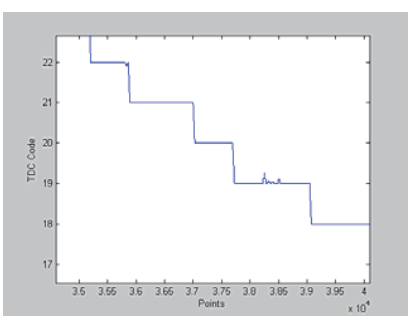
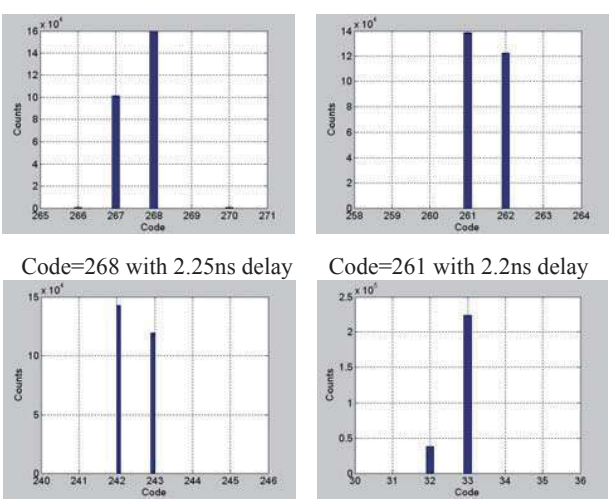


Fig. 5 Measured TDC output after median filter with 30X averaging.



Code=268 with 2.25ns delay Code=261 with 2.2ns delay

Code=242 with 1.99ns delay Code=33 with 0.35ns delay

Fig. 6 Measured TDC code distributions at 4 constant delays.